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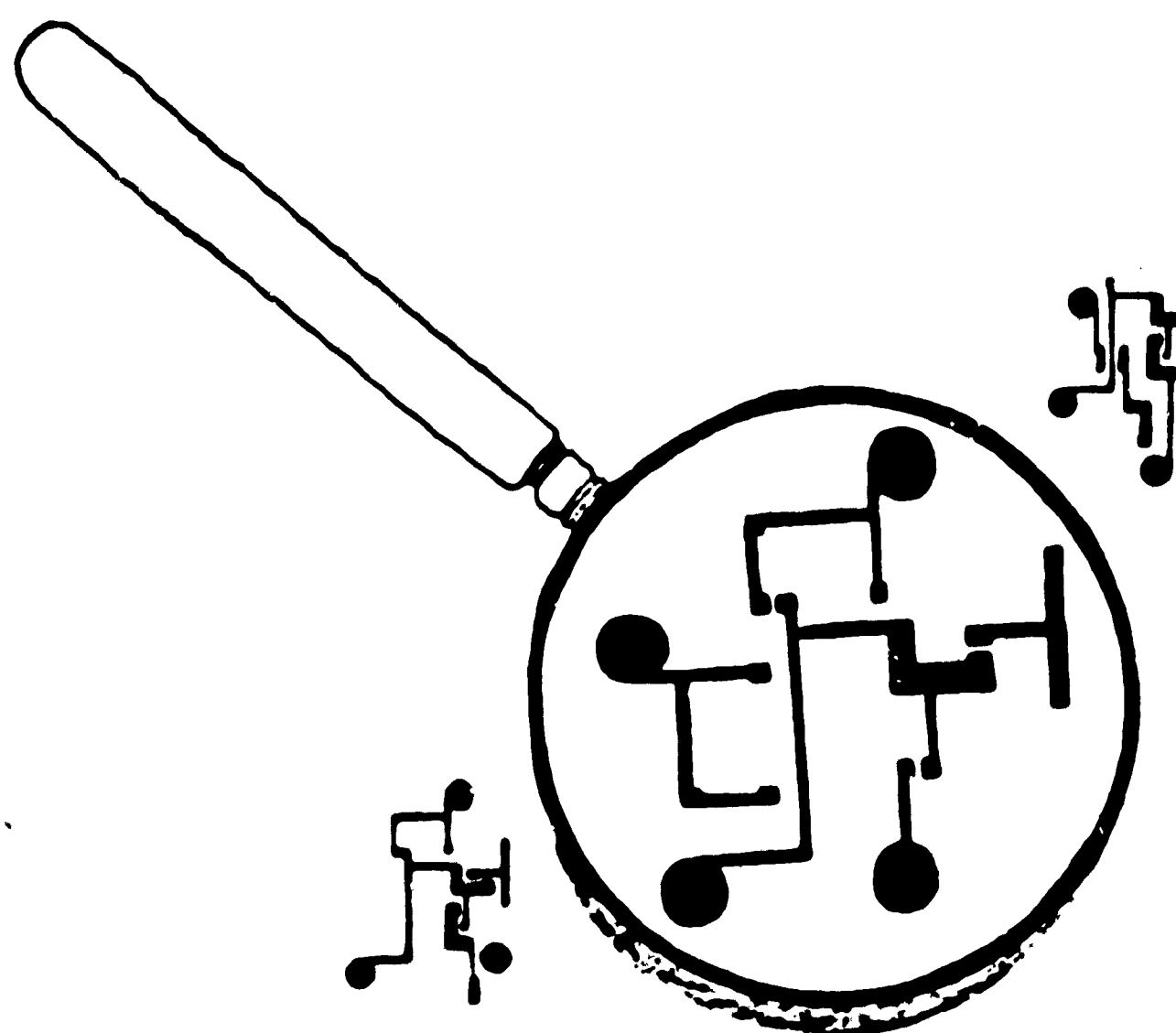
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μ-Notes

INFORMATION ON MICROELECTRONICS
FOR NAVY AVIONICS EQUIPMENT

μ-NOTES NO. 9

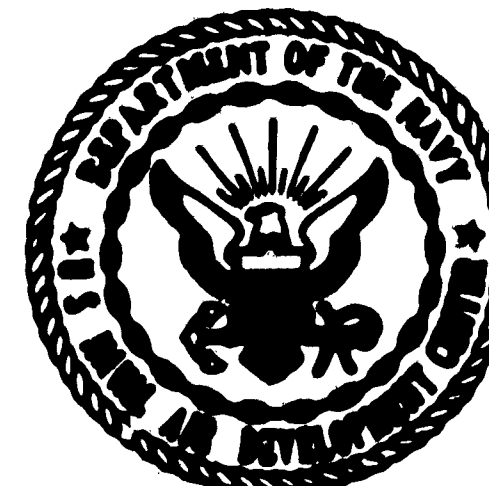
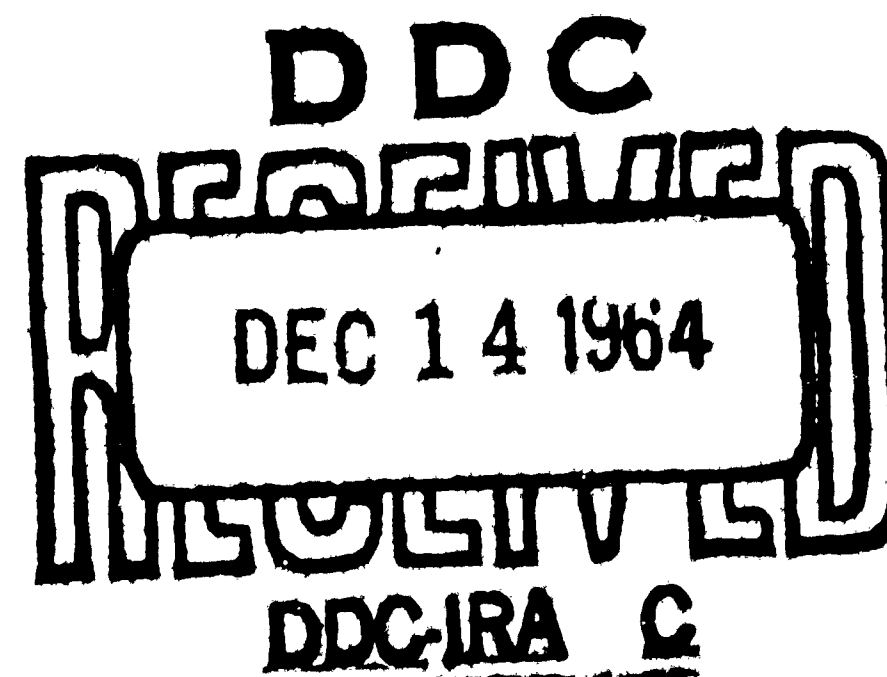
1 DECEMBER 1964



PREPARED BY

U. S. NAVAL AMMUNITION DEPOT
CRANE, INDIANA

U. S. NAVAL AIR DEVELOPMENT CENTER
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NAD Crane NADC Johnsville
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μ - NOTES NO. 9

1 DECEMBER 1964

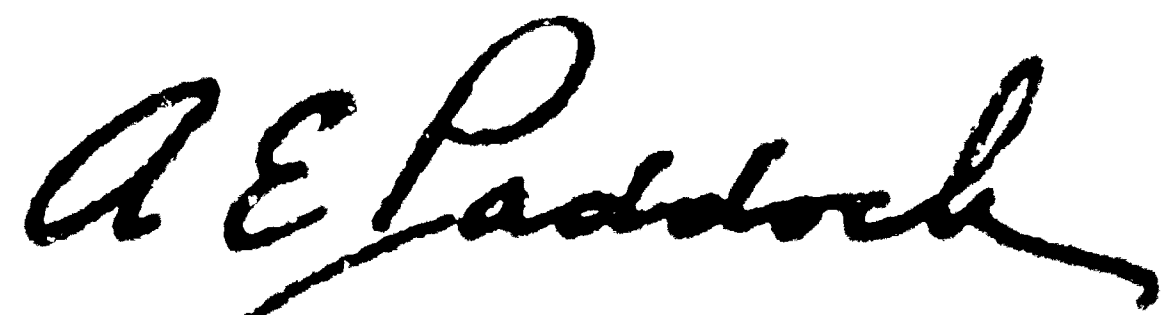
The Avionics Division of the Bureau of Naval Weapons has embarked upon a program utilizing microelectronics in Airborne electronic equipment. Two BUWEPS field stations, U. S. Naval Ammunition Depot, Crane and U. S. Naval Air Development Center Johnsville, have been assigned tasks implementing the BUWEPS program. The two activities were directed to make information on microelectronics available to Avionics equipment and systems manufacturers by distributing a periodic newsletter.

The purpose of the newsletter, μ-NOTES, is to provide information on evaluation, application, availability, research and development, and standardization activity pertaining to state-of-the-art circuits, devices and materials. Inquiries, comments, or suggestions are invited and should be addressed to the Commanding Officer, U. S. Naval Ammunition Depot, (Code QECA) Crane, Indiana 47522

Approved by:



E. R. PETTEBONE
Commanding Officer
U. S. Naval Ammunition Depot
Crane, Indiana



A. E. PADDOCK
Commanding Officer
U.S. Naval Air Development Center
Johnsville, Pennsylvania

P R E F A C E

The newsletter, *μ*-NOTES, is divided into topic sections (Research and Development, Standardization, Evaluation, Application, Availability) containing information of similar nature, in order to provide logical grouping and easy location of articles.

Each article, *μ*-NOTE, is numbered in the following manner:

First digit - "*μ*-NOTES" issue number

Second digit - Section number

Third digit - Consecutive number in the section. This will provide easy referral to articles and retain continuity when adding information to previous articles on the same topic.

The contents of this publication have been prepared by the Aeronautical Electronic and Electrical Laboratory, NAVAIRDEVCON and the Quality Evaluation Laboratory, NAD, under the direction of:

J. H. NAMAROFF, Development Support Division, AEEL,
NAVAIRDEVCON Johnsville

M. R. BUFFINGTON, Aircraft Equipment Branch, QEL,
NAD Crane

N O T I C E

Publication of data in the *U*-NOTES or comments regarding the products of any manufacturer does not constitute exclusive acceptance, approval or disapproval by the Government of the vendors products.

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Section 1
RESEARCH AND DEVELOPMENT

1.0.0

Section 1 - Research and Development

μ-Note 911

Microelectronic Power Supply Program

The objective of this program, under contract NOW 63-0749-di, and described briefly in *μ*-Note 811, was to standardize regulated voltage power supplies to be used in conjunction with microelectronic circuitry, a reduction in size and weight, and an improvement in efficiency and MTBF over available hardware.

Voltages and their regulation for the six different modules were also contained in *μ*-Note 811.

The modules were packaged in sizes ranging from 7 to 15 cubic inches for power ratings from 6 to 60 watts. Figures 1 through 4 show the final version of the experimental models, the first of three developmental stages of this contract. The final versions of the succeeding developmental models will contain simplified circuitry and will use greater efficiency in packaging.

No forced air cooling or external means, other than a heat sink, is necessary. The specified cooling requirements indicate meeting the requirements of MIL-E-5400 for Class 3 equipment except that the maximum temperature of the supply mounting plate will be +55°C, and the maximum temperature of the surrounding ambient air will be +85°C. Internal cooling is provided by conduction paths to the base plate of the power supply.

Figures 5 and 6 show the final production version of the power supply developed for the one-way Data Link equipment, AN/ASW-25(XN-1), under a NAVAIRDEVCON contract.



FIGURE 1 - Experimental Models -
6W to 60W

1.1.1

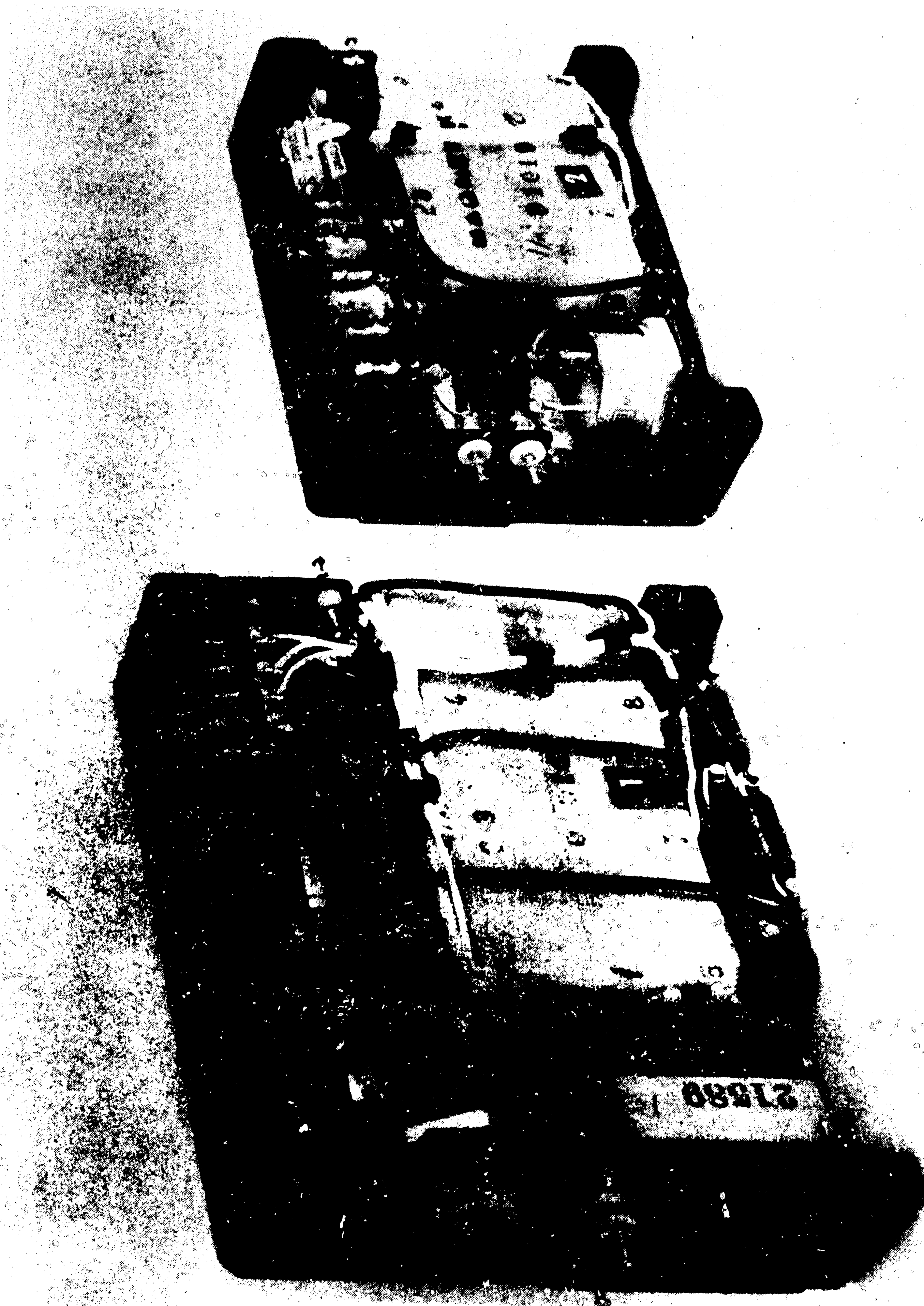


FIGURE 2 - Comparison of GON to GON



FIGURE 3 - Size Portrayal of 60W
Module

1.1.3

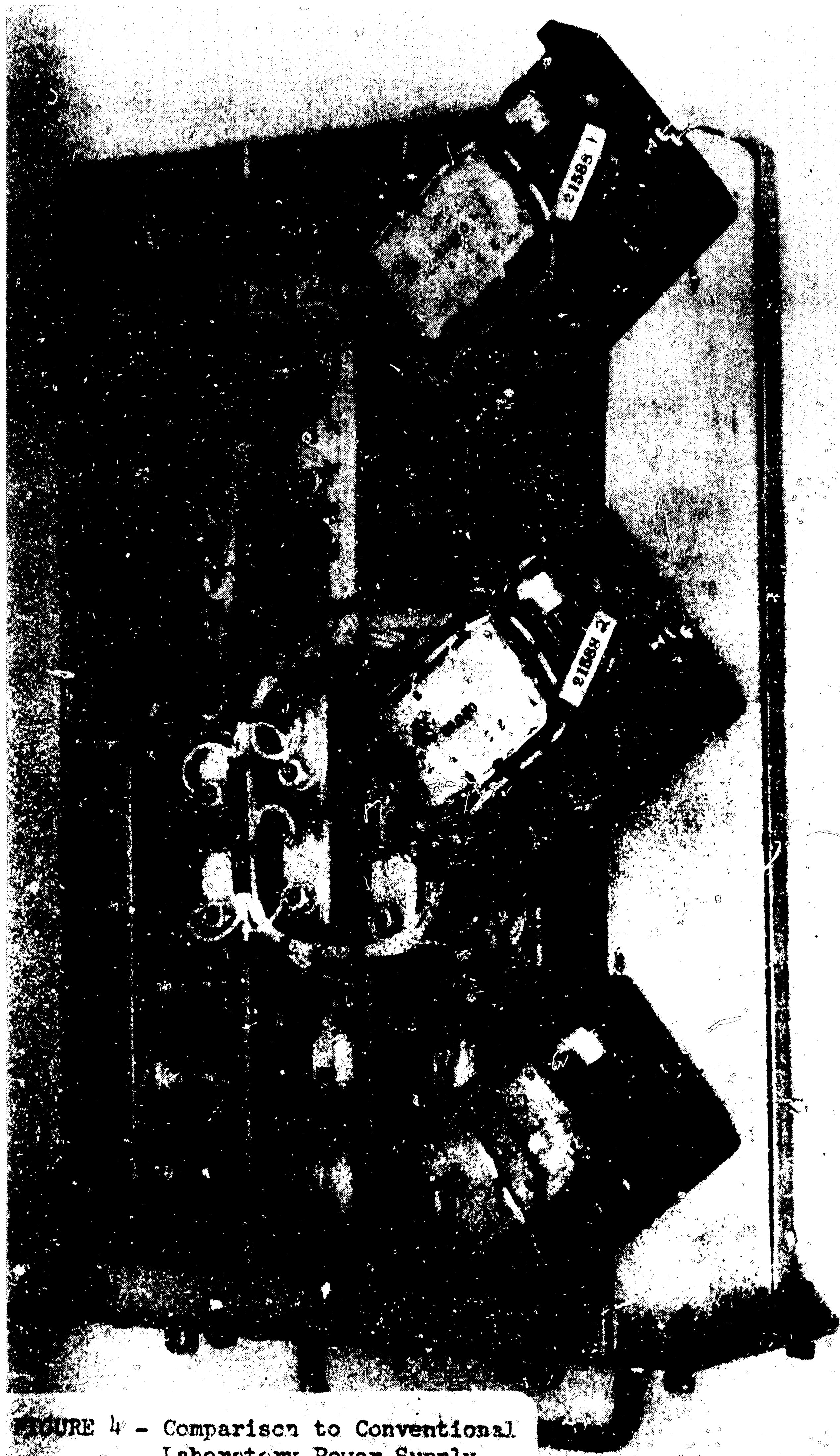


FIGURE 4 - Comparison to Conventional
Laboratory Power Supply

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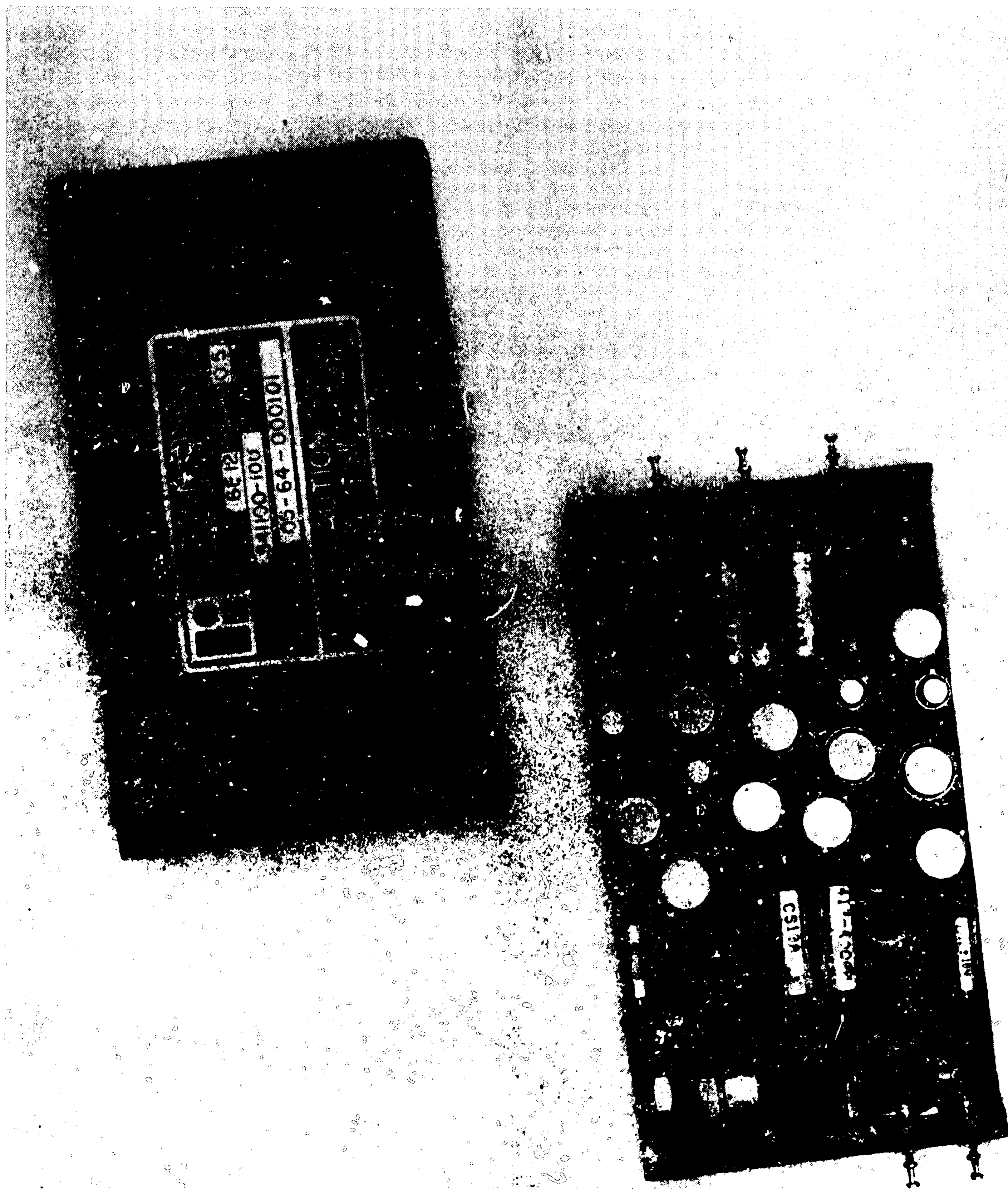


FIGURE 5 - Data Link Version Module

1.1.5



FIGURE 6 - Size Portrayal of D-L Module

1.1.6

Resume of Epitaxial Studies Report - Part I

Battelle Memorial Institute under NAVAIRDEVCON Contract N62269-2470 prepared a Special Report on Microelectronic Studies entitled Epitaxial Studies. This report consists of a summary of the many articles which have appeared in the literature on epitaxial films on semiconductors in recent years and describes the bibliography covering different aspects of epitaxy.

This *M*-Note will present the first part of this report and will consist of the Introduction, Summary and Background.

Introduction

The semiconductor industry is one in which the technologies used are subject to refinement and change continuously. The introduction of epitaxial technology for fabrication of semiconductor devices in the early 1960's represents a step forward for the industry because of the additional possibilities for devices that the technology offers. However, as with any new technology, there are many aspects and variations to be explored; consequently a considerable number of papers on the subject have appeared in the literature during the last four years. It was decided that this would be an opportune time to review the state-of-the-art. In this report, more than 100 papers have been reviewed and classified as to subject matter in a bibliography. The opportunity was taken to assess the state-of-the-art for different aspects of epitaxy which have potential semiconductor device applications. The state-of-the-art assessment forms the major part of this report, and the bibliography forms the supporting part.

Summary

The process of epitaxial growth has permitted production of transistors and microcircuits of superior characteristics compared to those which had been made before the development of this process. It makes possible devices such as heterojunctions and retrograde junctions which cannot be formed by other methods. It permits the growth of thin single crystalline semiconductor films which are of controlled resistivity and thickness and relatively free of lattice imperfections.

There are many techniques which can be used to deposit epitaxial films. The most important at the present time appears to be the hydrogen reduction of silicon tetrachloride. The hydrogen reduction of trichlorosilane and decomposition of silane have been used to a lesser extent. Germanium can be deposited by hydrogen reduction of germanium tetrachloride or disproportionation of germanium di-iodide. It is also possible that vacuum evaporation of silicon and germanium on single-crystal substrate will prove to be a useful technique, especially since vacuum evaporation is already widely used in micro-circuit fabrication.

There are still many unknown factors involved in the epitaxial deposition of thin films of silicon on silicon substrates. The cause of these stacking faults is not yet established. The actual reaction taking place at the gas substrate interface has not been well defined. The control of thin film resistivity and thickness is not as good as desired. Therefore, it seems likely that epitaxial growth will be a subject of continued research for some time in the future.

Background

The term epitaxy ("orderly arrangement on") was introduced by L. Royer in 1928 to denote the phenomenon of oriented growth of one crystal onto another. This was first found to occur naturally on certain materials; two crystals of different species had grown together with a definite unique orientation relationship between their crystal axes.

The first successful attempt to produce epitaxial growth in the laboratory was apparently made by Frankenheim in 1836 who grew sodium nitrate from a water solution in perfect orientation onto a calcite crystal. Other methods which have subsequently been successful in producing epitaxial layers are:

1. Electroplating
2. Vacuum evaporation
3. Sputtering
4. Chemical reaction - For example, if a single crystal of silver is placed in a solution of chlorine in water, an epitaxial deposit of silver chloride grows on the crystal surface.

5. Chemical vapor deposition - This is a process wherein a material is deposited onto a surface as a result of chemical reactions between gaseous reagents taking place preferentially on the surface. This process has been used almost exclusively for the epitaxial deposition of germanium and silicon onto parent substrates for electronic device fabrication.

The successful achievement of an epitaxial deposit depends on satisfying certain requirements involving the structural nature and material of the surface on which deposition is proceeding, the surface

temperature, and the rate of deposition. If these requirements are not met, the resulting deposit will be polycrystalline or amorphous. Partial orientation may also occur in which only one crystal direction in the deposit bears a unique relation to the crystal axes of the substrate, and this is termed "partial epitaxy." For complete epitaxy, all three crystal axes in the deposit should be related to the substrate crystal axes.

Isoepitaxy is a term used to denote the growth of a layer onto a substrate of the same material, and this is often done in semiconductor device fabrication, as when n-type silicon is deposited epitaxially on a p-type silicon substrate.

Rheotaxy is a term recently coined to describe the growth of a solid, single-crystal deposit on a substrate which, at the elevated temperatures used for deposition, is covered with a liquid glaze.

Future issues of *μ*-Notes will contain additional information regarding the epitaxial process.

Section 2
STANDARDIZATION

2.0.0

Section 3
EVALUATION

3.0.0

***μ*-NOTE 931**

EVALUATION OF SILICONIX INC. "A" SERIES INTEGRATED DIGITAL CIRCUITS

"A" SERIES INDEX

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INVESTIGATION OF SILICONIX INCORPORATED "A" SERIES LCDTL INTEGRATED CIRCUITS

I. Circuit Description

A. This family of circuits is designed around the basic NAND Gate shown in Figure 3.1.1. Each type is a true monolithic integrated circuit, i.e., all active and passive components in the circuit are produced integrally with, and inseparable from, the substrate. All circuits use epitaxial transistors. Multiple diffusions are used to complete the active and passive circuit components. The structures are packaged in either modified TO-5 cans or in flat pack form for higher density systems.

B. The siliconix DTL Gate has two circuit-design modifications from conventional DTL circuits. They are: (1) the addition of emitter follower Q_1 to relax gain restrictions and (2) the use of clamping diode D_3 to prevent inverter saturation. These modifications have led to the term load compensated DTL or LCDTL.

C. The Siliconix family of DTL circuits consists of the following units.

1. A02 and A07 - Dual Power Gate and Dual NAND/NOR Gate. The A02 and A07 circuits are identical except for fan-out. The A02 can drive a fan-out of 15 and the A07 can drive a fan-out of 5. See Figure 3.1.1.

2. A01 and A06 - Single Power Gate and Single NAND/NOR Gate. The A01 and A06 Single NAND/NOR Gates have the same electrical characteristics as the A02 and A07 dual gates with the addition of a fan-in expansion terminal. See Figure 3.1.1. The A01 and A06 are identical, except for fan-out. The A01 and A06 have fan-out capabilities of 15 and 5 respectively.

3. A03 - Counter, Shift-Register Circuit. The A03 is a flip-flop for use in counter and register applications. Designed for use with a single-phase clock, the A03 may be operated asynchronously or synchronously. Eight separate inputs can be connected to implement a variety of logic functions. The A03 is a monolithic array of six direct-coupled NAND Gates. See Figure 3.1.11 for a block diagram of the circuit and the truth table defining its operation.

4. A04 - Diode Array. The A04 is a diode array used to extend single gate fan-in (A01 and A06) in increments of six, to a limit depending upon input loading and circuit speed. See Figure 3.1.19.

5. A05 - Dual NAND/NOR Gate Line Driver. The A05 is identical to the A07 Dual NAND Gate with the addition of an internally connected pull-up resistor (See Figure 3.1.21) which provides a charge path for capacitive loads and increases the high output level.

6. A03 - Monostable Multivibrator. The A08 is a six-gate array connected to perform the one-shot function. Delays are implemented by connecting external capacitors from D-D' to ground. Three inputs and complimentary outputs are provided to increase the circuits' versatility. See Figure 3.1.28.

7. A20 - Dual NAND/NOR Gate. The A20 is a selected dual NAND/NOR Gate for special applications such as buffers and FET commutator drivers. Selection is based on BV_{cex} of Q2. When used with external load resistors and an external source voltage, V_s , an output voltage swing of 15 volts is possible. See Figure 3.1.35.

II. Circuit Tests.

A. The D-C characteristics of the Siliconix A series of LCDTL circuits were obtained using a transistor curve tracer. Six curves make up the family of D-C characteristics. They are as follows: (1) V_{in} vs V_{out} , (2) I_{in} vs V_{out} , (3) V_{in} vs I_{in} , (4) V_{out} vs I_{out} , (5) V_{cc} vs V_{out} and (6) V_{cc} vs I_{cc} . Temperature was used as a parameter on those curves where important variations were noted. Included in the information obtainable from these curves are: (1) the worst-case output voltage under full load, (2) maximum low or "false" output voltage, (3) minimum high or "true" output voltage, and (4) worst-case input current.

The curves plus any necessary explanation are presented with the data for each device.

Due to the identical nature of some of the devices (see the equivalent circuits, Figure 3.1.1) only the following were tested.

- (1) A02 - Dual Power Gate
- (2) A03 - Counter, Shift Register Circuit
- (3) A05 - Dual NAND/NOR Gate Line Driver
- (4) A04 - Diode Array
- (5) A08 - Monostable Multivibrator

B. Dynamic tests were performed on four of the seven designated types of circuits manufactured by Siliconix. Tests on all types would have been redundant because of the similarity noted previously. The circuits dynamically tested were the A02 Dual NAND/NOR Power Gate, Figure 3.1.1; the A03 Counter, Shift-Register Circuit, Figure 3.1.11; the A05 Dual NAND/NOR Gate Line Driver, Figure 3.1.21; and the A08 Monostable Multivibrator, Figure 3.1.28.

Tests on the gates consisted of measuring pulse amplitude, pulse width, rise time, fall time, delay time, storage time, and propagation delay. These measurements were made with fan-outs of 1, 5, and maximum, at bias voltages (V_{cc}) of 4, 5 and 6 volts, and temperatures of -55, -40, 25, 85 and 125°C. A block diagram of the test set-up is shown in Figure 3.1.5. Definition of the measured parameters (rise time etc.) is given in Figure 3.1.6.

Tests on the flip-flop consisted of measuring the same parameters as measured on the gates with the exception of set-up time which was determined instead of propagation delay. These measurements were again determined at the various values of fan-out, bias voltage, and temperature. Figure 3.1.14 shows a block diagram of the test set-up and Figure 3.1.15 defines the measured parameters.

The A08 monostable multivibrator was tested by measuring pulse amplitude, pulse width, rise time, fall time and delay time. These measurements were made with external capacitances from D-D' to ground of 113 and 226 pico-farads. Measurements for each value of capacitance were obtained at bias voltages of 4, 5, and 6 volts and temperatures of -55, -40, 25, 85 and 125°C. The minimum pulse widths at the complimentary outputs (open circuit from D-D' to ground) were measured for each condition of bias voltage and temperature. All tests were performed at a fan-out of one from each output. Figure 3.1.32 shows a block diagram of the test set-up and Figure 3.1.33 defines the measured parameters.

III. Circuit Performance.

A. General observations made while performing tests on Siliconix "A" Series LCDTL integrated circuits are listed below together with any comments.

1. From the block diagrams of the test set-ups shown in Figures 3.1.5, 3.1.14 and 3.1.32 it can be seen that the test circuitry consisted of essentially three Siliconix A type circuits in series. The first circuit is termed the driver unit, the second the test unit, and the third the load unit(s). It will be noted that all units were enclosed in the temperature chamber and hence changes noted in the test circuit performance as a function of temperature (all data was acquired from the "test circuit") were due in part to changes in the associated circuitry. This is also true for changes due to bias supply, variations, i.e., all units were connected to the same supply and were subjected to the same variations. It is felt that testing in this manner produces results more typical to system performance than if isolated circuits were tested.

2. A characteristic of the LCDTL circuits was ringing on the lower voltage level of the output pulse. See oscillographs accompanying the data sheets. This ringing, which is attributed to the diode D₃, of Figure 3.1.1, was found to increase with decreasing temperature. It was also noted to decrease with increasing fan-out or with decreasing bias supply, V_{cc}. The ringing is a noticeable characteristic of the circuits when viewed on an oscilloscope but it did not have any apparant adverse effect on circuit operation. The ringing is not propagated from one circuit to another but is generated in each individual circuit. This is shown by the fact that in a NAND Gate a low voltage input (with ringing) produces a high voltage output with no ringing.

During the discussion of the data in this report with Siliconix engineers it was learned that a mask change and a process change has been introduced to reduce the ringing noted above. The results are shown in Figure 3.1.9.

3. As has been the case in several previous issues of μ -NOTES, the definitions of the various time parameters used by this facility and those used by the manufacturer have been different. Siliconix uses definitions shown in Figure 3.1.36 for the dynamic parameters.

The waveforms used in this report are defined in Figures 3.1.6, 3.1.15 and 3.1.33. Generally speaking, the time definitions used for the gate circuits are more severe than those imposed by Siliconix and those used for the flip-flop are less severe. Comparison of data published by the manufacturer and that shown in this report should be done with the above mentioned differences in mind.

4. Data on circuit performance as a function of fan-in was not acquired. It was found that differences in circuit performance with fan-ins ranging from one to four (the A01 and A06 were not tested) was negligible.

Multiple fan-ins from circuits not utilizing pull up resistors in the output transistor collector circuits, produce the result that no output can go to its high voltage level unless all outputs connected to that particular fan-in array are also high. This is true for all DTL circuits, not only the A series of Siliconix. This fact is mentioned because of the effect noted on the performance of the flip-flop and one-shot circuits which are arrays of NAND Gates. In the case of the flip-flop, the SI logic input which was supplied by a type A02 gate would not go high until after the clock pulse went low if the clock pulse was present during the transient of the logic input from its low to its high state. See Figures 3.1.11, 3.1.14 and 3.1.18. In the case of the one-shot, the \bar{T} input, which was also supplied by an A02 gate, would not go high until after the \bar{Q} output went high. See Figures 3.1.28, 3.1.32 and 3.1.34. If any undesirable results were found because of the above mentioned characteristics they could be easily corrected by using the A05 units (with pull up resistors in the output transistor collector circuits) in place of the A02 units as driver circuits to the devices in question (A03 and A08).

**A02 Dual Power Gate
Characteristic Data and Graphs**

CIRCUIT DIAGRAMS

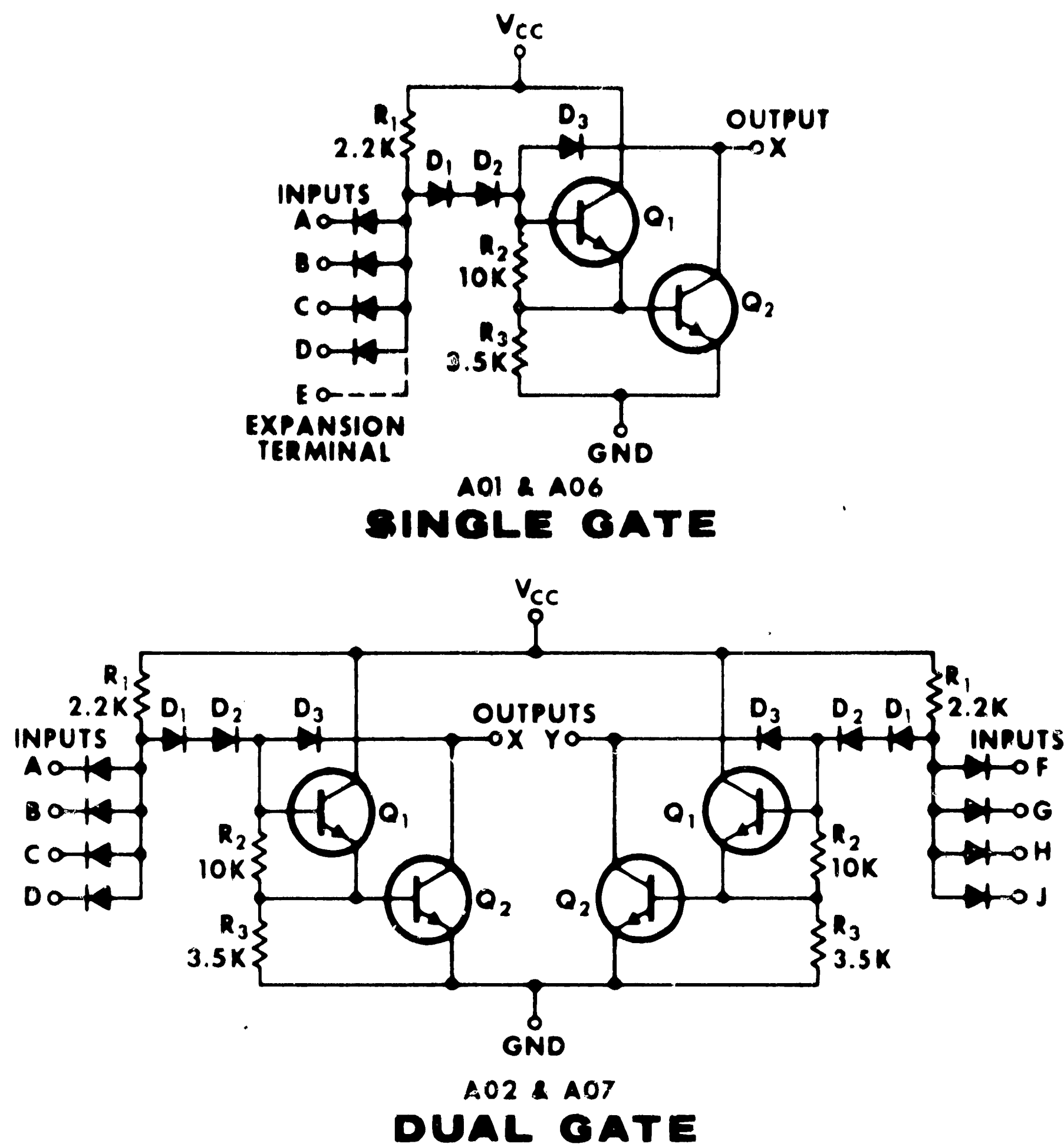
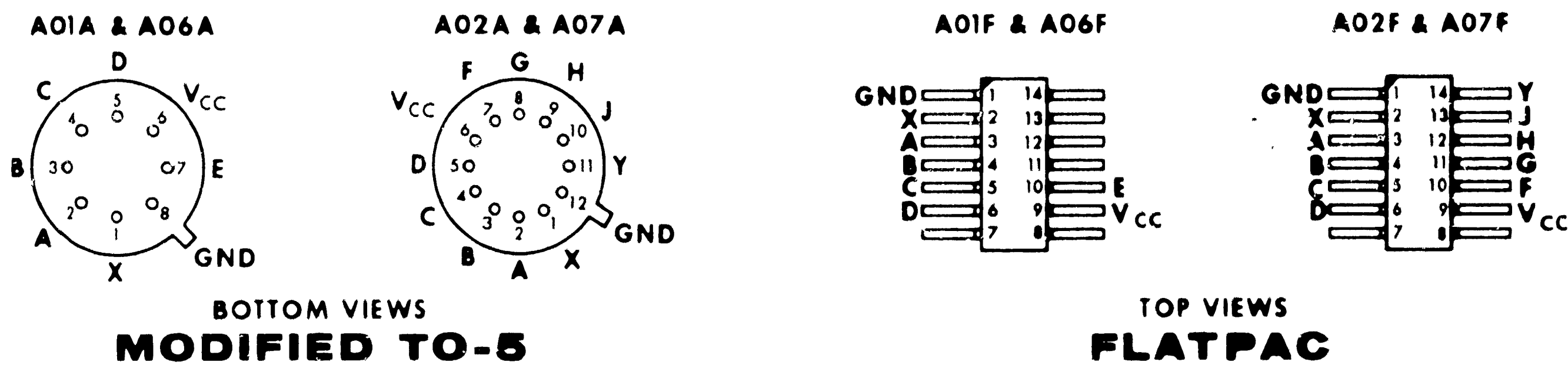
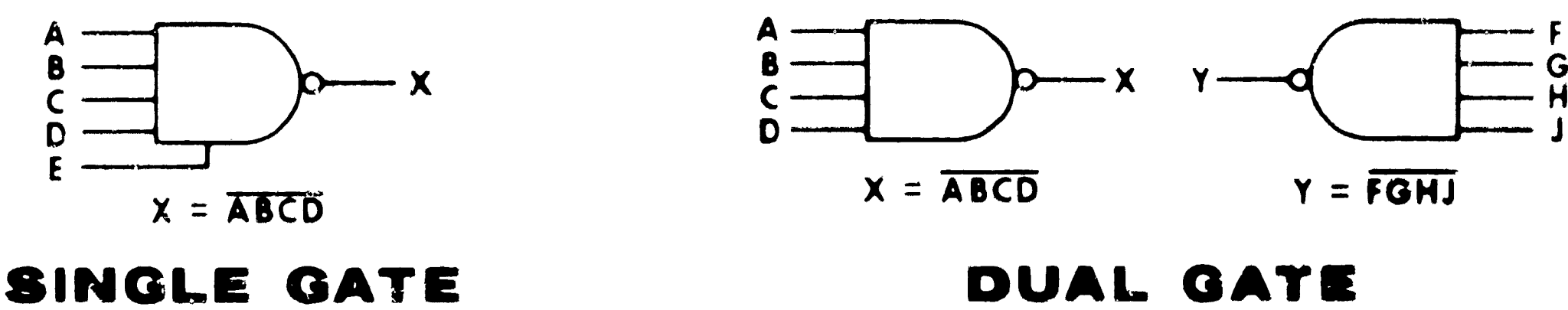


Figure 3.1.1

PIN DIAGRAMS



LOGIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS AT 25°C

Power Supply Voltage V_{CC}	6 v
Input Voltage BV_i	6 v
Output Voltage BV_o	6 v
Operating Temperature Range T_A	-55 to +125°C
Storage Temperature Range T_S	-65 to +150°C
Output Current	50 ma

Voltage at any pin must be positive with respect to the common terminal.

AO2 DUAL NAND/NOR GATE

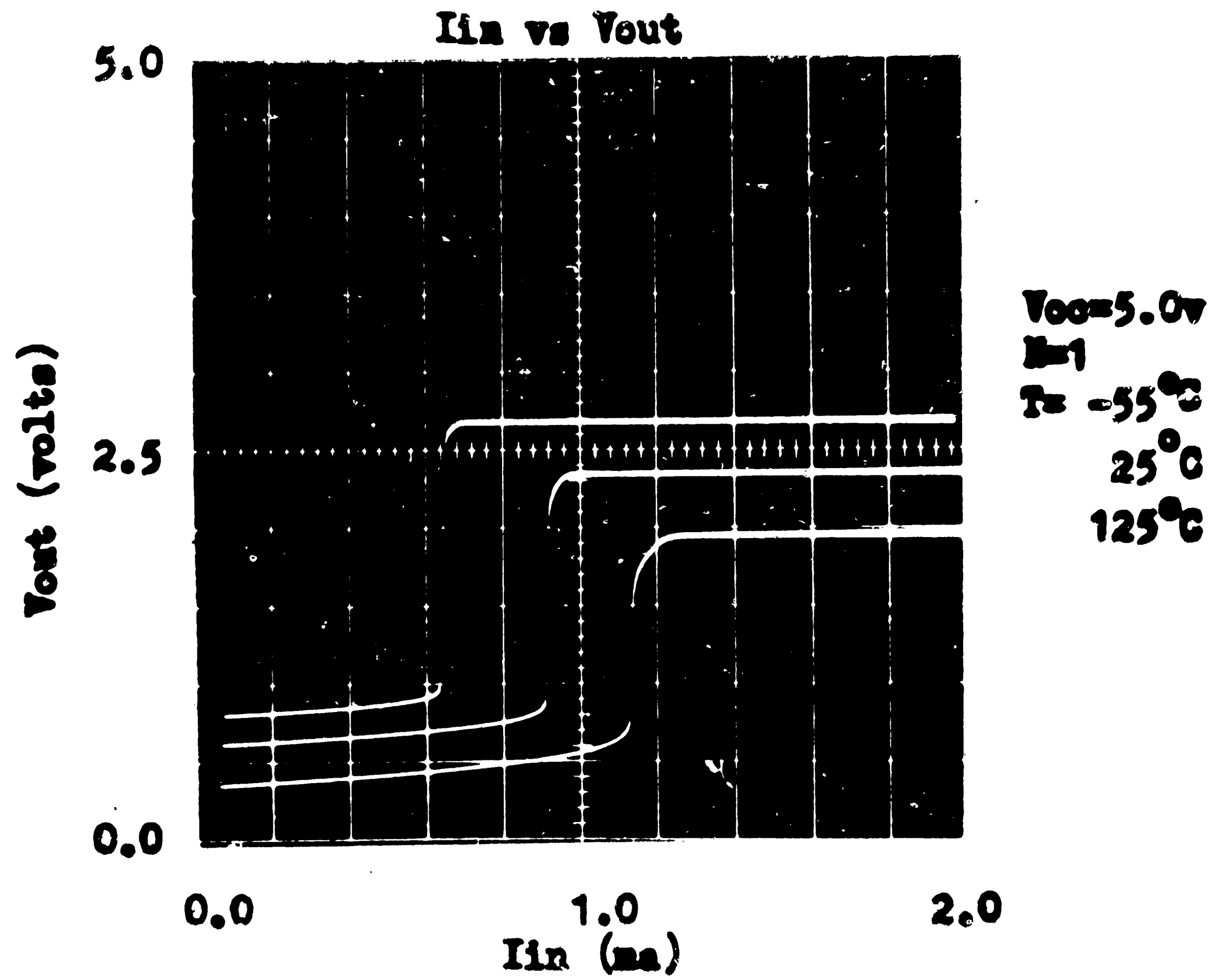
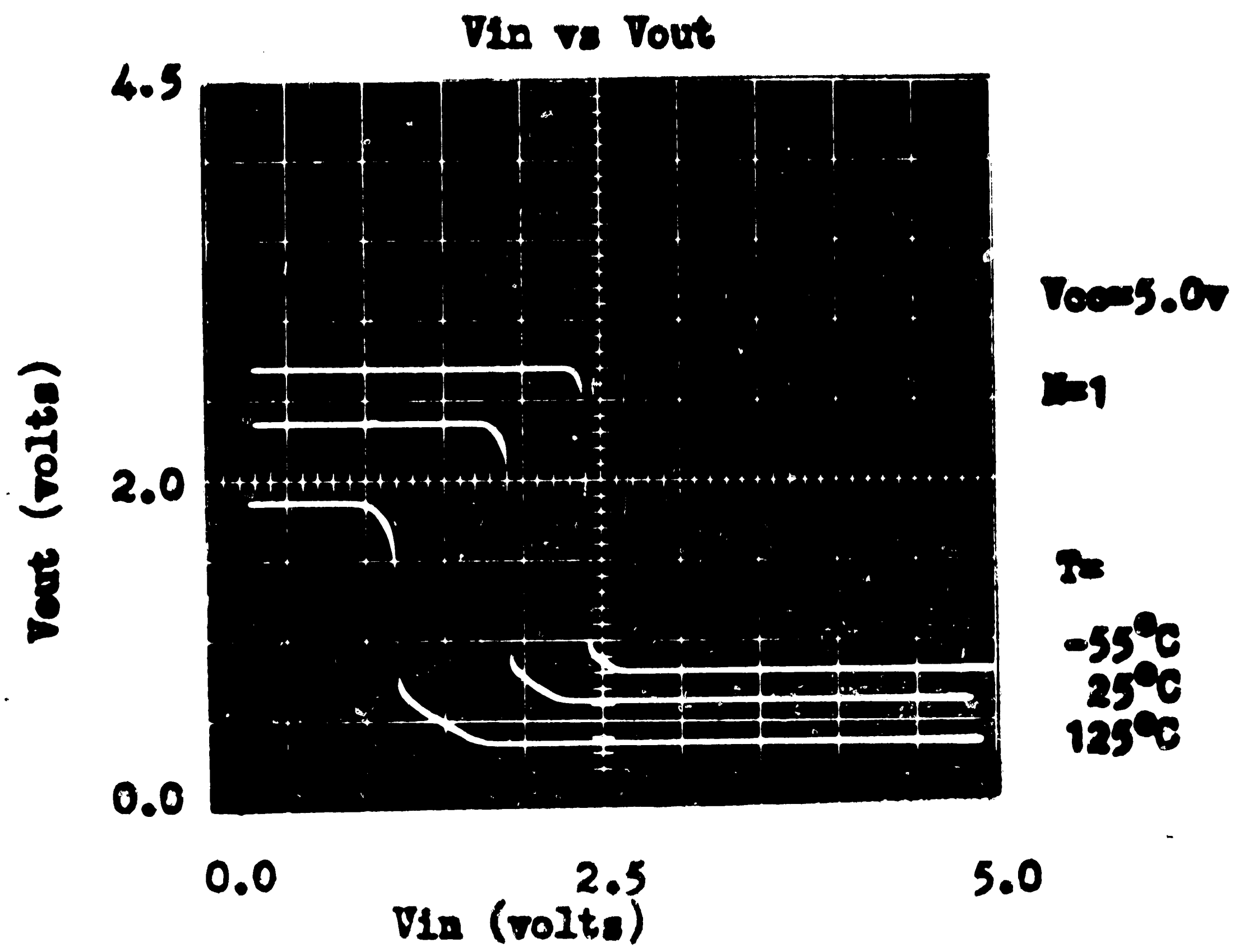
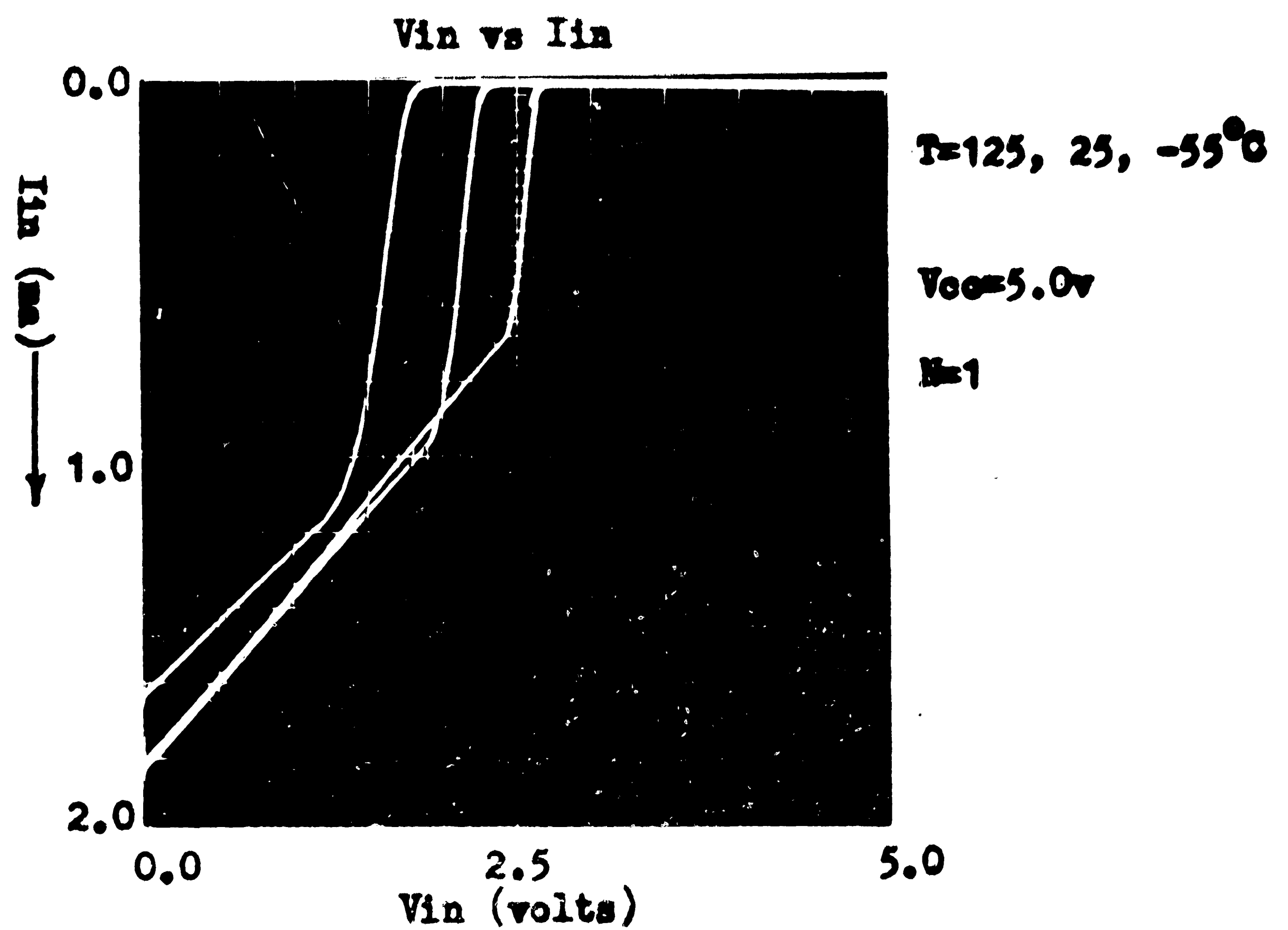


Figure 3.1.2

AO2 DUAL NAND/NOR GATE



Note: The V_{in} vs I_{in} curve also represents a V_{out} vs I_{out} characteristic for $V_{in}=0.0$ and $N>0$.

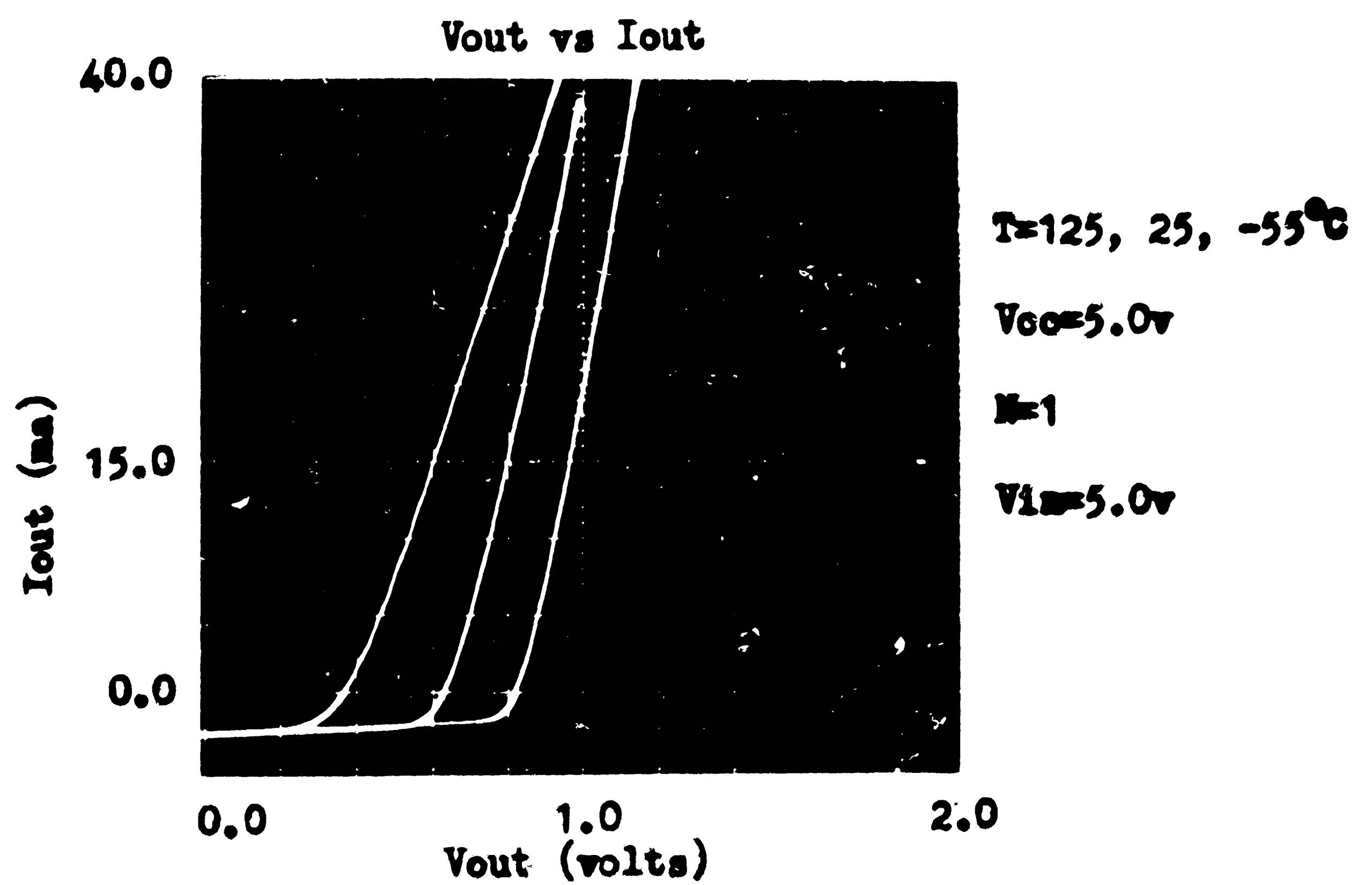
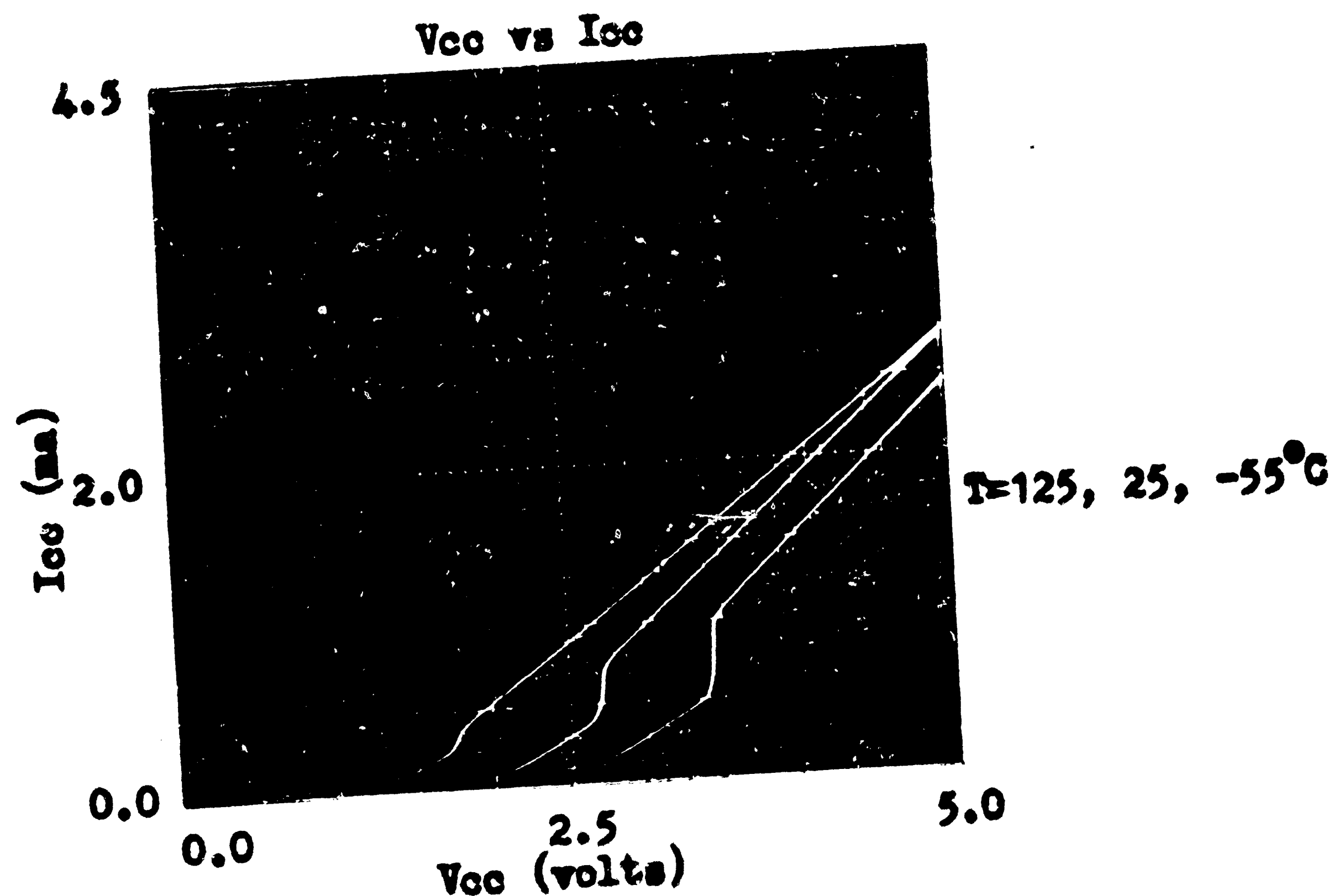
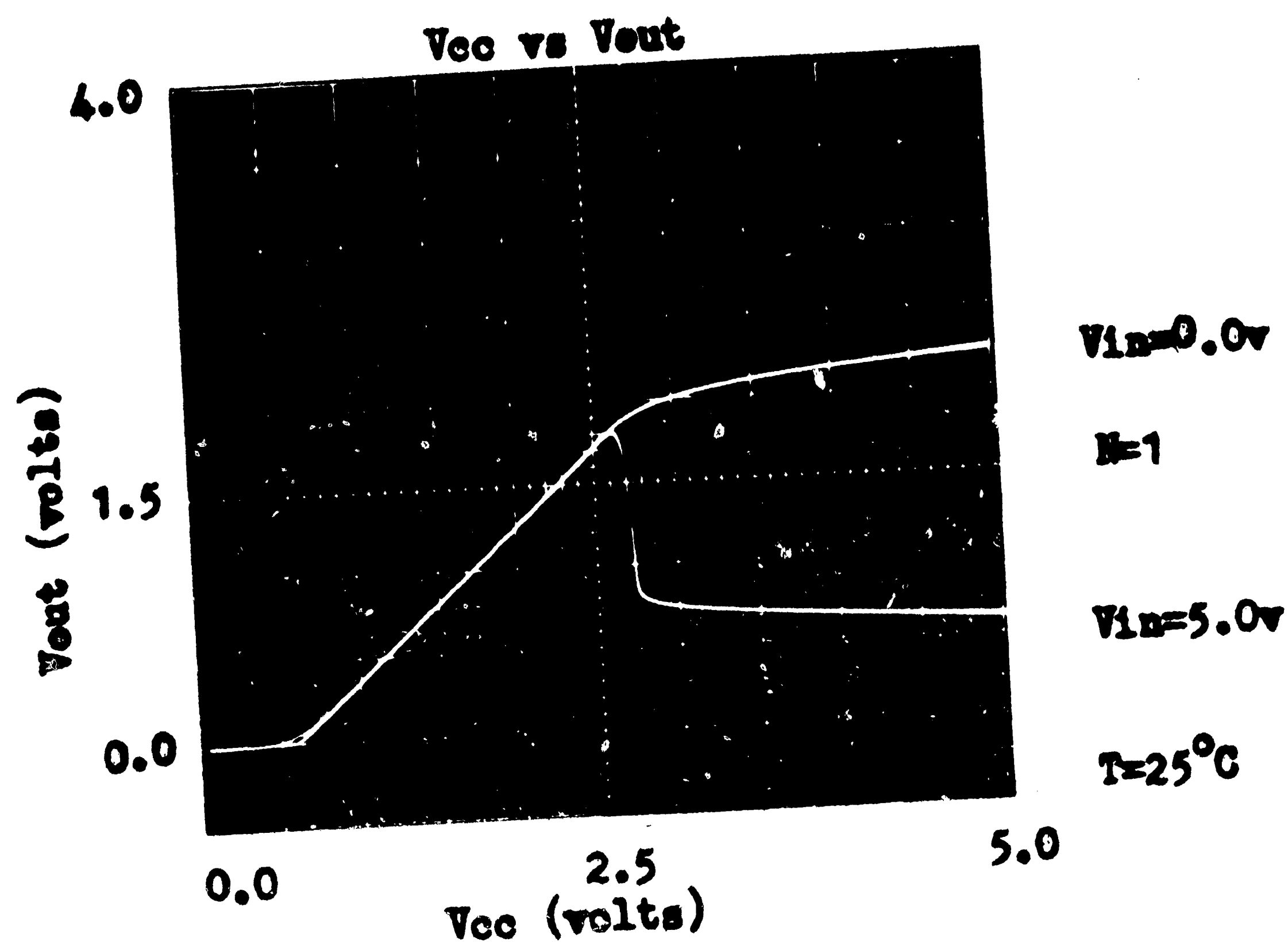


Figure 3.1.3

AO2 DUAL NAND/NOR GATE



The power dissipation curve, V_{cc} vs I_{cc}, shown above was obtained by loading one circuit of the dual NAND unit with the other. The inputs to the first circuit were left open simulating a high level input. This produced a low output which was coupled to the input of second circuit. In this manner a 50% duty cycle power dissipation curve (one circuit "on" and one circuit "off") is obtained for the complete unit. Power dissipation for one circuit is obtained by dividing the product of V_{cc} and I_{cc} shown on the above curve by two.

Figure 3.1.4

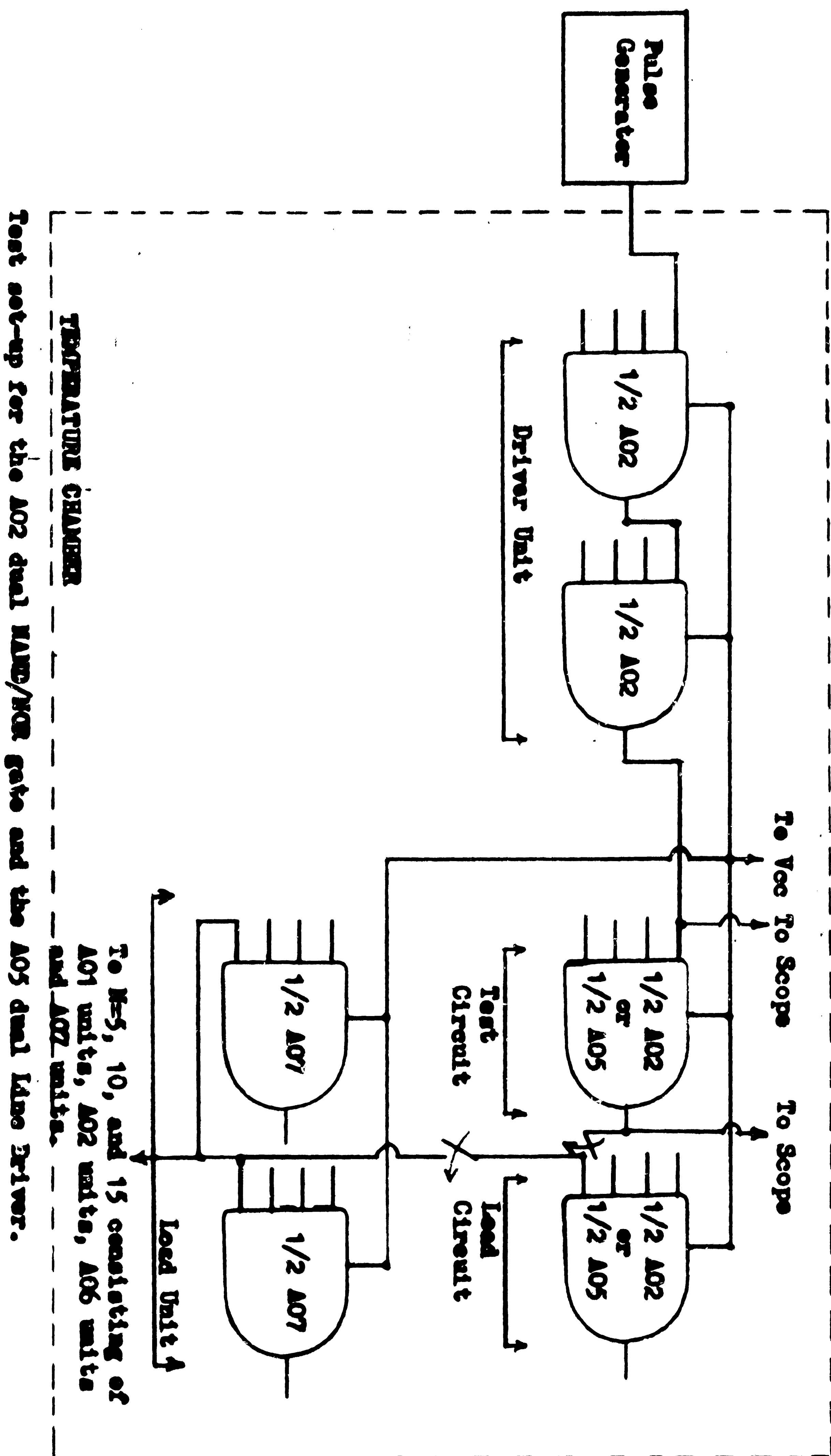
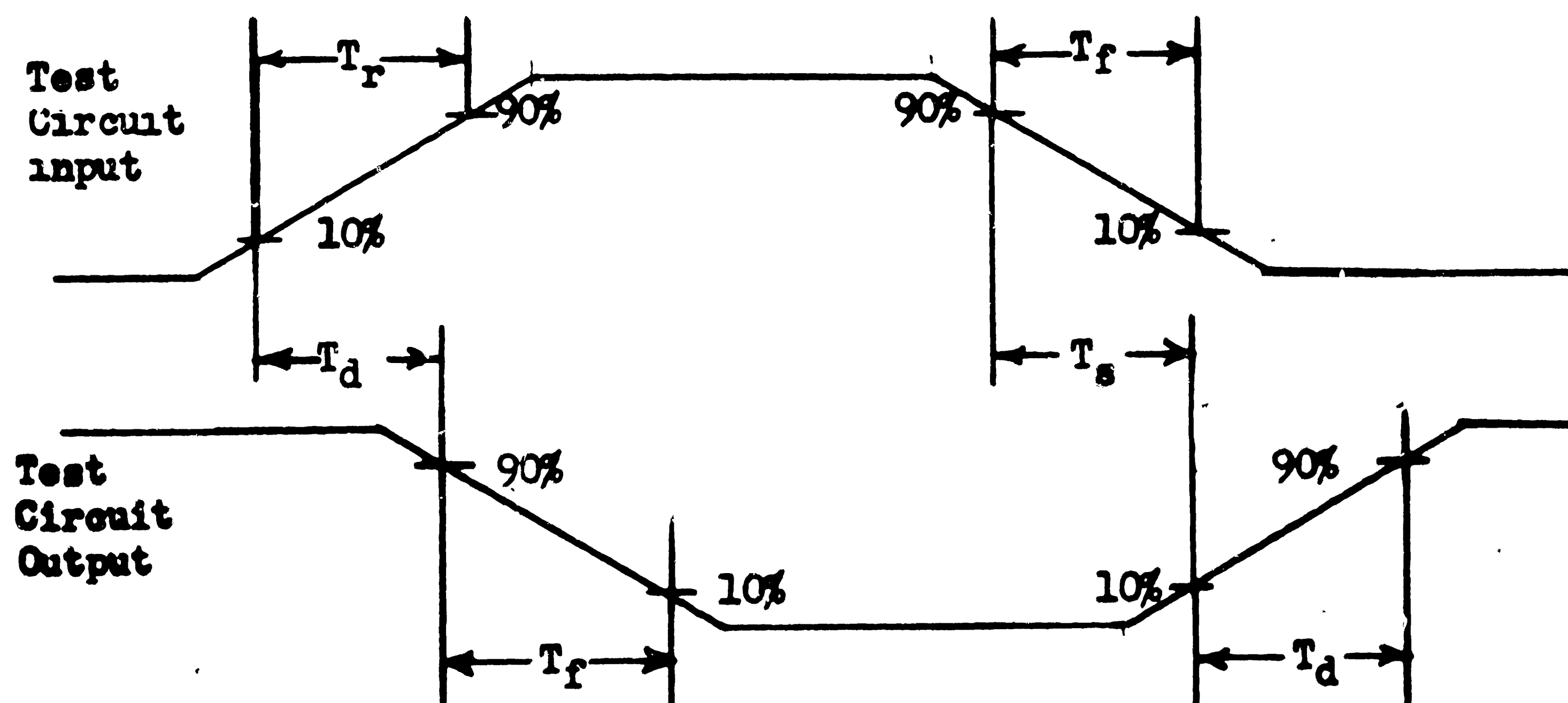
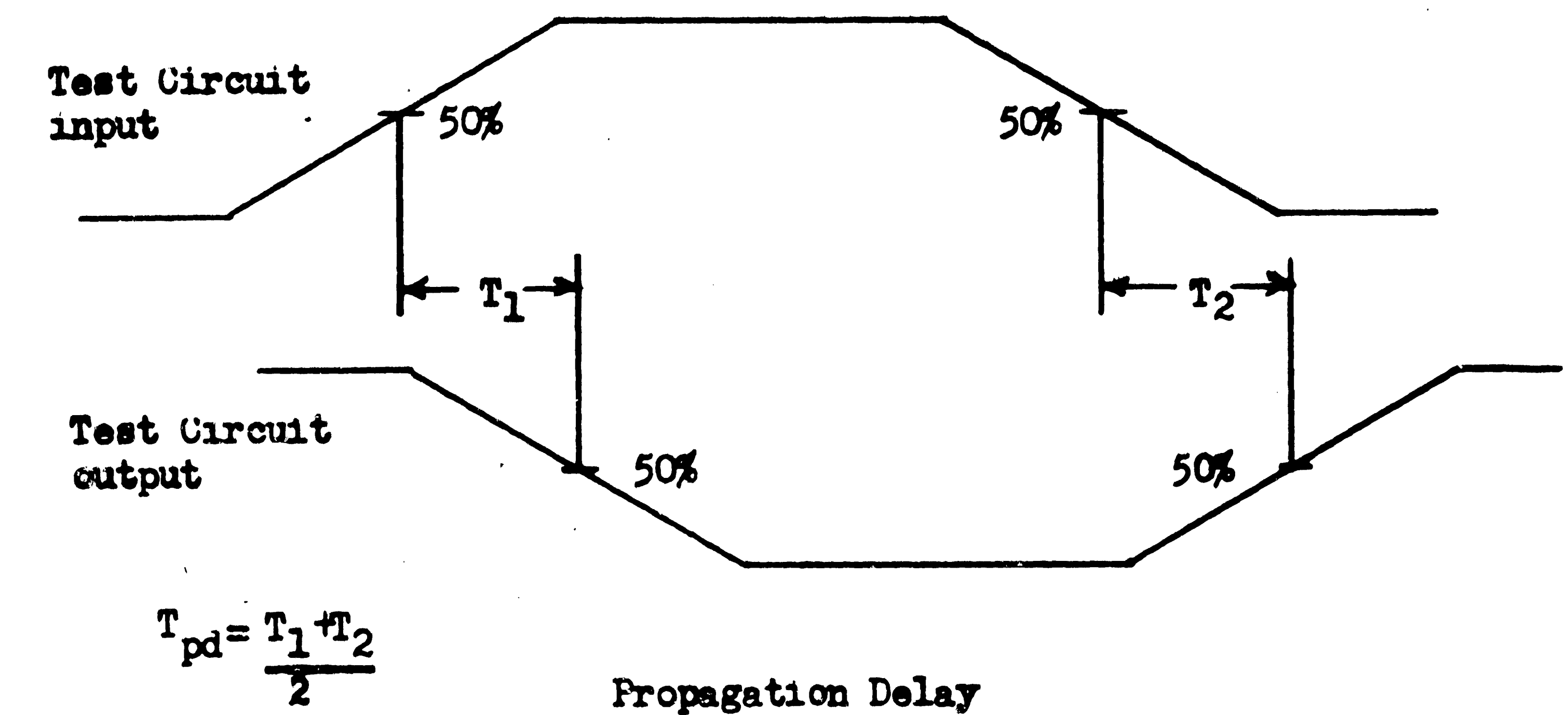


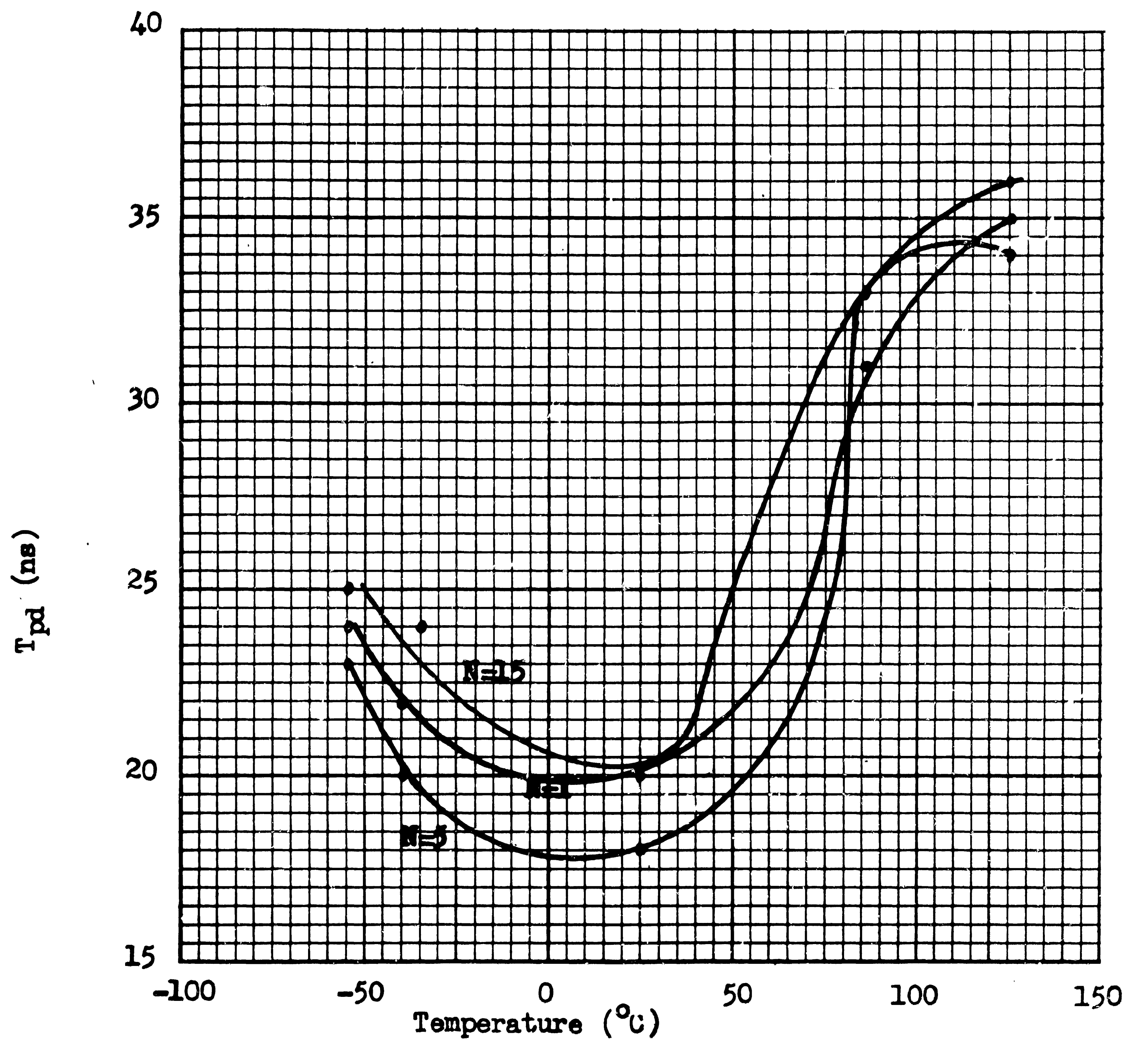
Figure 3.1.5



Rise time (T_r), Fall time (T_f), Delay time (T_d), Storage time (T_s).

A02 and A05 NAND/NOR Gate waveform definitions.

Figure 3.1.6



AO2 NAND/NOR Power Gate. Propagation delay vs temperature with the number of loads (N) as a parameter. $V_{cc}=5.0v$

Figure 3.1.7

AO2 DUAL NAND/NOR GATE

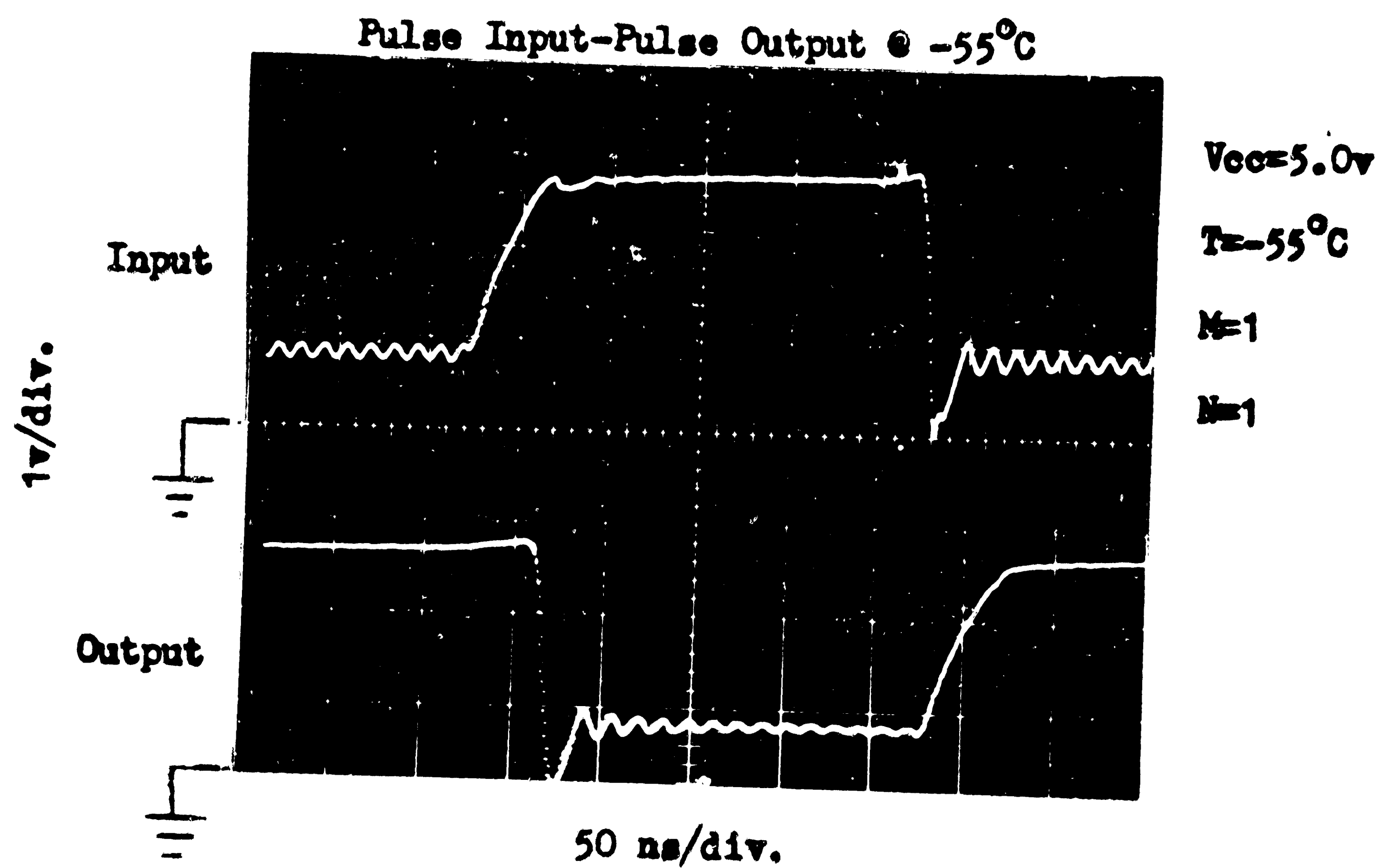
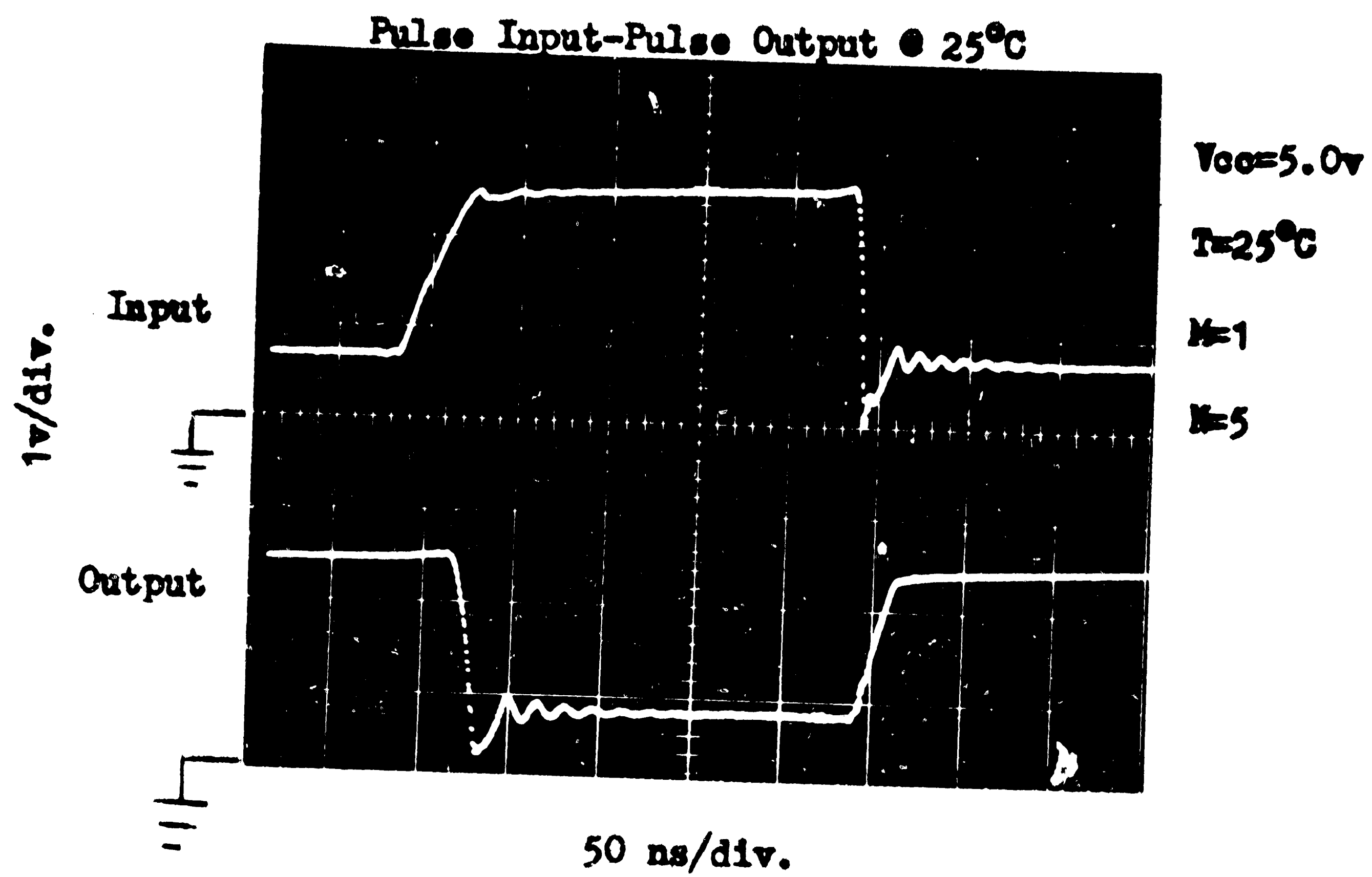
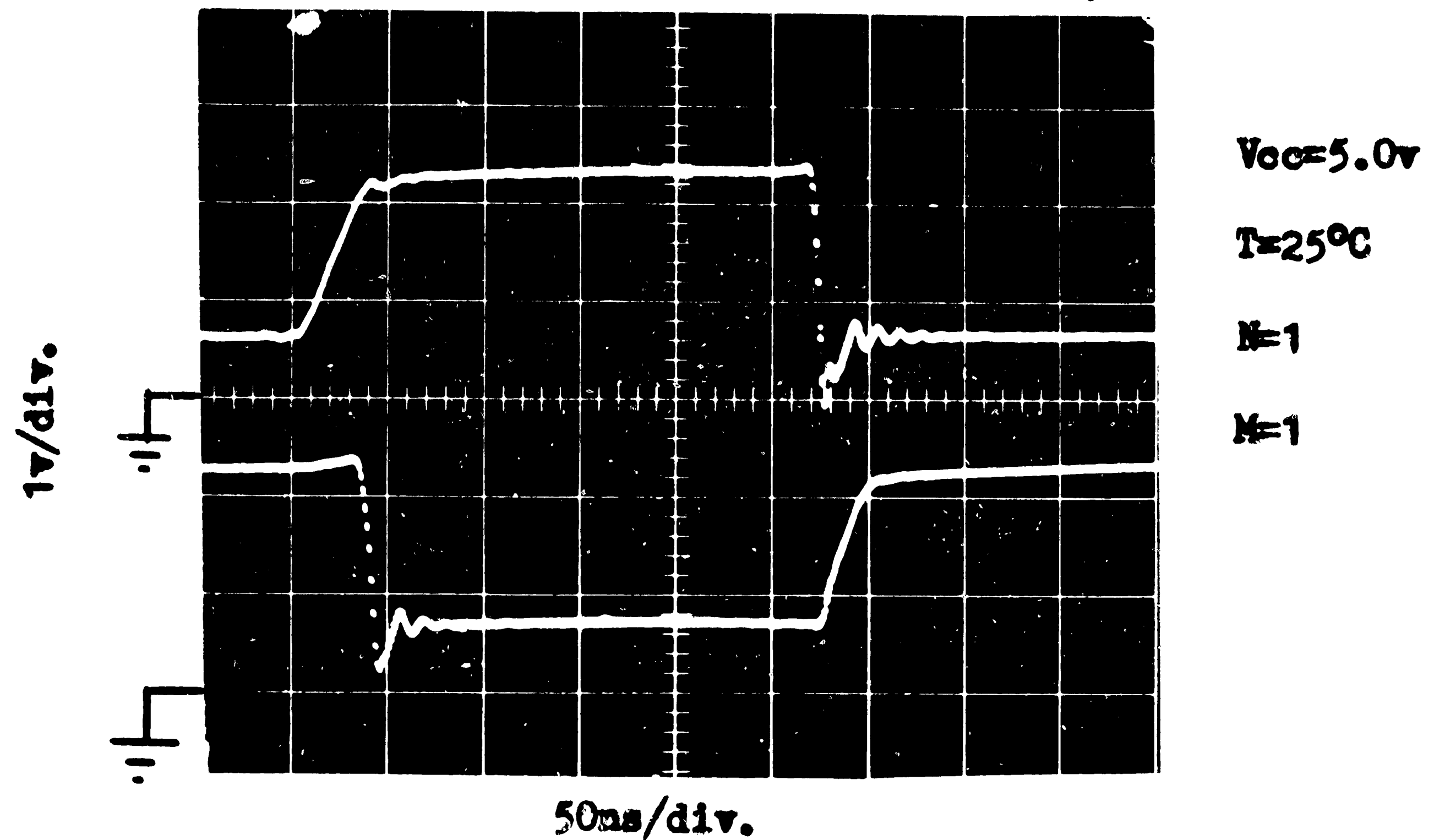


Figure 3.1.8

A02 Dual NAND/NOR Gate driving a A07 Dual NAND/NOR Gate



This oscillograph demonstrates the difference in output pulses between an "old" circuit and a "new" circuit. The top trace is the output of an A02 before changes were made in the production process. This trace is also the input to an A07 circuit which was manufactured under the new process. The output of the A07 is shown in the bottom trace. Note the reduction in the duration of the ringing as well as the peak amplitude.

Figure 3.1.9

AO2 DUAL NAND/NOR GATE

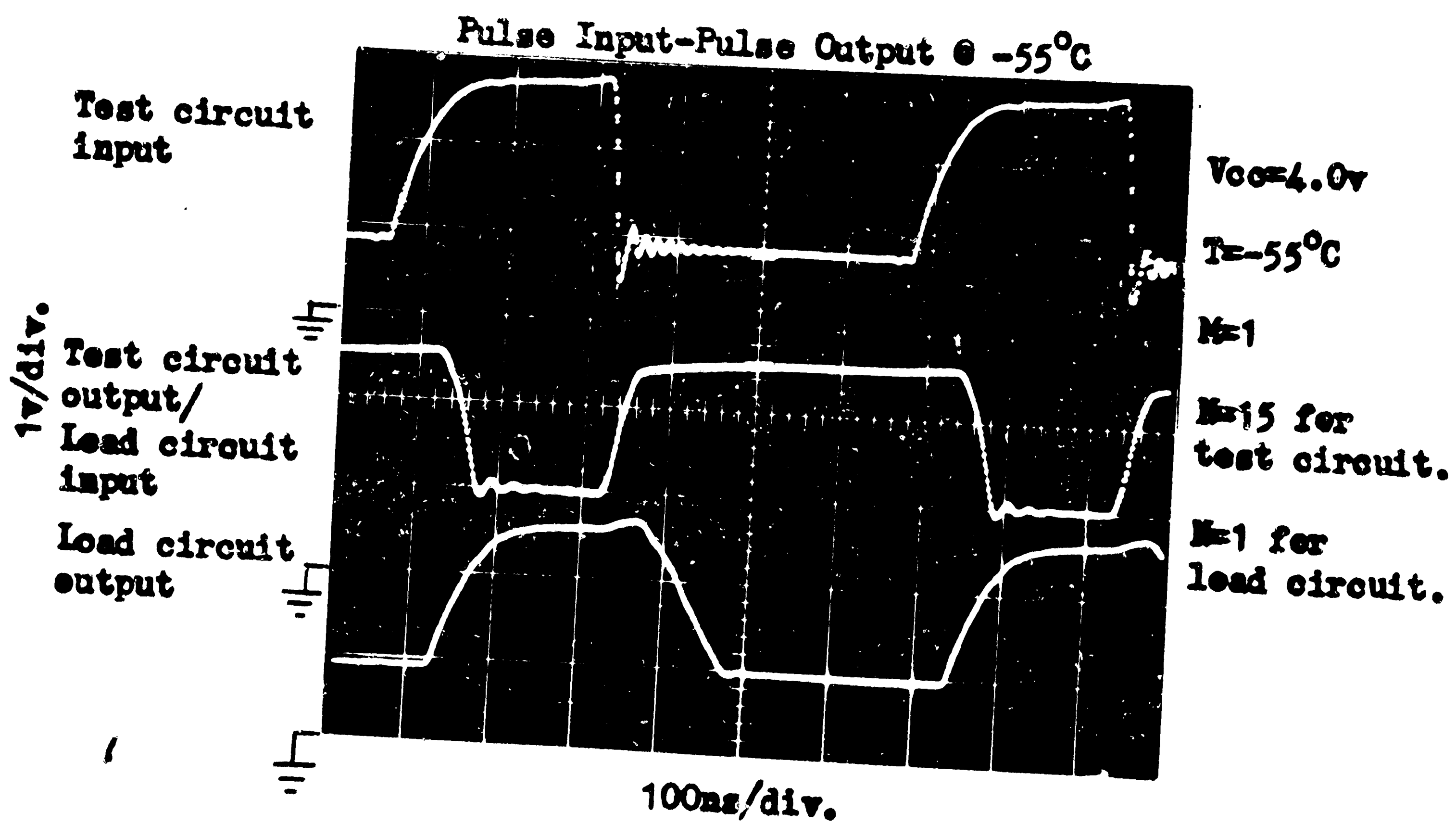
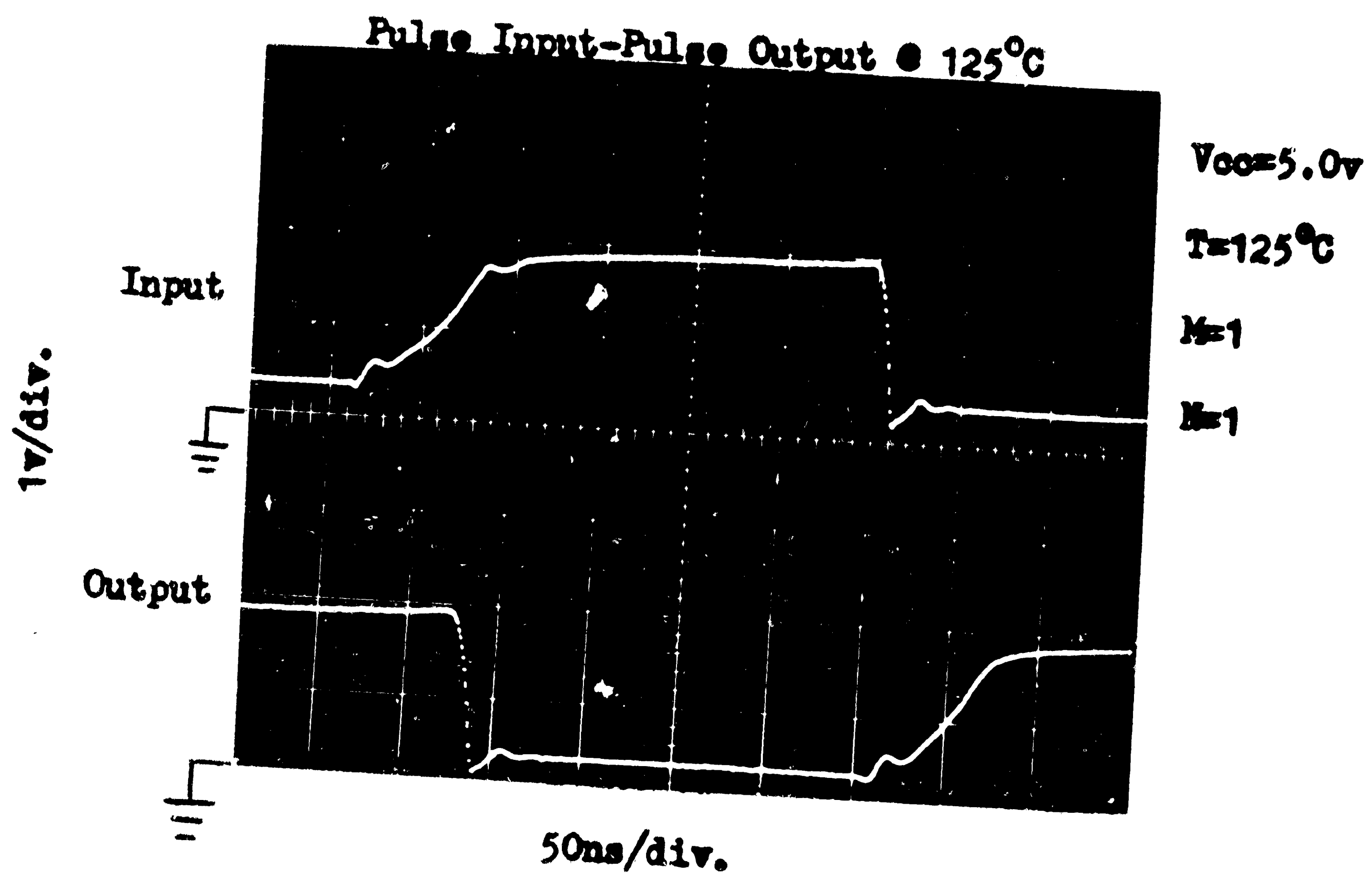


Figure 3.1.10

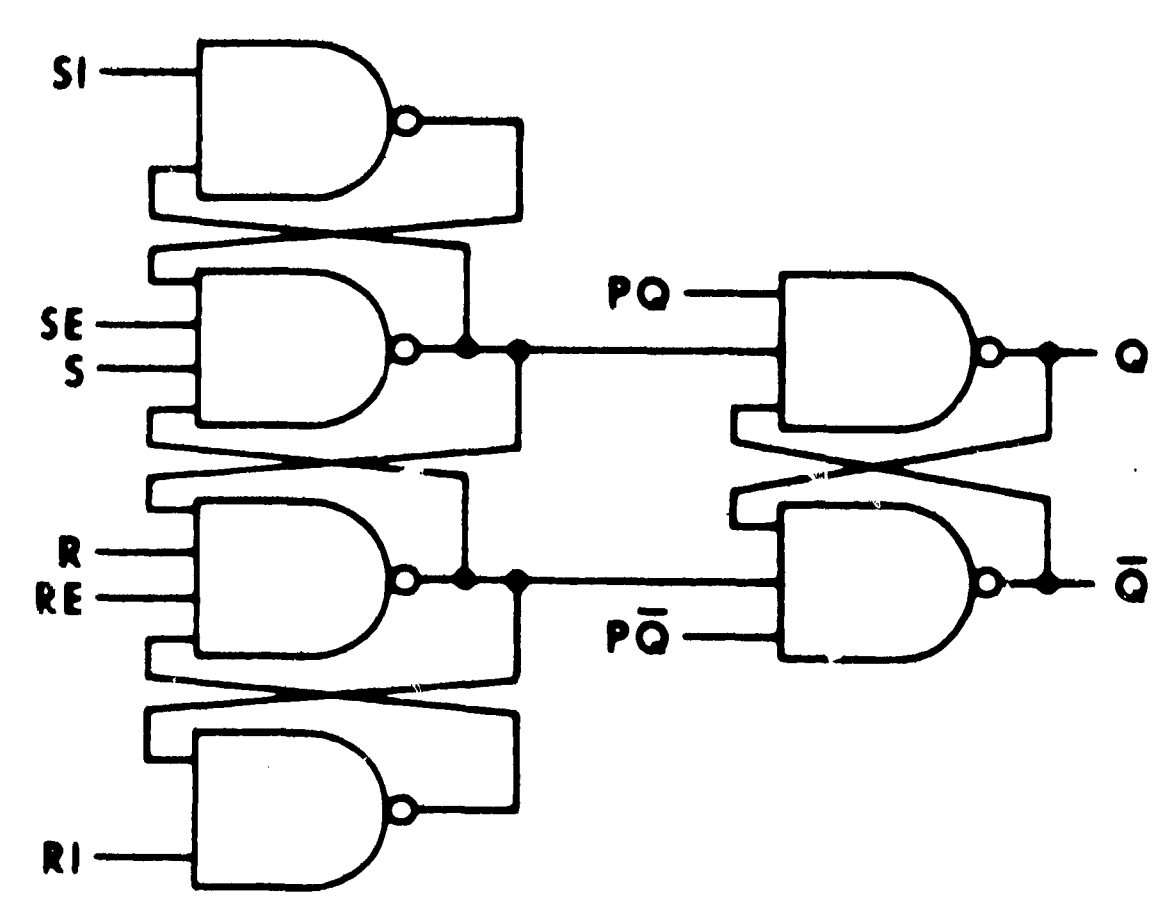
Circuit Designation A02, Fan-In 1, Vcc 4.0 Volts, Input Pulse Rep. Rate 1 MC									
Temperature		-55°C			-40°C			25°C	
Test Circuit:		Output @ N =			Output @ N =			Input	
		1	5	15	1	5	15	1	5
Pulse Amplitude (V _{pp})	1.8	1.8	1.6	1.5	1.7	1.7	1.5	1.7	1.6
Pulse Width (ns)	250	219	199	184	230	210	202	250	232
T _r (ns)	64	83	42	34	71	36	31	45	31
T _f (ns)	9	13	21	38	11	17	29	5	12
T _d (ns)		73	76	84	62	65	70		43
T _s (ns)		8	8	9	10	8	9		8
T _{pd} (ns)		44	39	48	38	34	41		24
Temperature		85°C			125°C				
Test Circuit:		Output @ N =			Output @ N =				
		1	5	15	1	5	15		
Pulse Amplitude (V _{pp})	1.6	1.5	1.4	1.2	1.5	1.3	1.1		
Pulse Width (ns)	250	251	244	245	250	280	275		
T _r (ns)	41	54	45	49	87	84	82		
T _f (ns)	5	8	12	17	7	12	18		
T _d (ns)		35	53	46		60	60		
T _s (ns)		10	10	10		12	15		
T _{pd} (ns)		25	22	25		37	36		

Circuit Designation A02, Fan-In 1, Vcc 5.0 Volts, Input Pulse Rep. Rate 1 MC													
Temperature		-55°C					-40°C			25°C			
Test Circuit:		Input	Output @ N =			Input	Output @ N =			Input	Output @ N =		
			1	5	15		1	5	15		1	5	15
Pulse Amplitude (Vpp)		2.0	1.9	1.8	1.7	1.9	1.9	1.8	1.7	1.8	1.8	1.7	1.5
Pulse Width (ns)		250	247	232	228	250	245	236	232	250	250	243	243
Tr (ns)		36	40	21	22	32	38	19	21	31	37	22	28
Tf (ns)		5	6	10	17	4	6	9	16	4	6	9	14
Td (ns)			38	39	41		34	36	38		42	29	30
Ts (ns)			8	8	8		9	8	8		9	8	8
Tpd (ns)			24	23	26		22	20	24		20	18	20
Temperature		85°C					125°C						
Test Circuit:		Input	Output @ N =			Input	Output @ N =						
			1	5	15		1	5	15				
Pulse Amplitude (Vpp)		1.7	1.7	1.5	1.3	1.6	1.5	1.4	1.1				
Pulse Width (ns)		250	276	276	277	250	284	280	281				
Tr (ns)		52	63	66	75	87	73	86	91				
Tf (ns)		4	5	9	15	7	8	12	19				
Td (ns)			49	50	50		59	60	61				
Ts (ns)			10	9	9		14	12	18				
Tpd (ns)			31	33	33		35	34	36				

Circuit Designation A02 , Fan-In 1 , Vcc 6.0 Volts, Input Pulse Rep. Rate 1MC									
Temperature		-55°C			-40°C			25°C	
Test Circuit:	Input	Output @ N =			Input	Output @ N =			Input
		1	5	15		1	5	15	
Pulse Amplitude (Vpp)	2.2	2.0	1.9	1.8	2.0	1.9	1.9	1.7	2.0
Pulse Width (ns)	250	247	238	236	250	250	242	240	250
Tr (ns)	25	30	16	18	24	27	16	18	28
Tr (ns)	4	5	8	14	4	5	8	13	3
Td (ns)		27	29	30		26	27	27	
Ts (ns)		9	6	8		9	8	7	
Tpd (ns)		19	17	20		18	17	19	
Temperature		85°C			125°C				
Test Circuit:	Input	Output @ N =			Input	Output @ N =			Input
		1	5	15		1	5	15	
Pulse Amplitude (Vpp)	1.8	1.8	1.6	1.3	1.7	1.6	1.5	1.2	
Pulse Width (ns)	250	278	275	280	250	292	286	279	
Tr (ns)	49	56	69	81	90	77	92	90	
Tr (ns)	4	5	9	16	7	8	12	21	
Td (ns)		45	52	52		63	65	65	
Ts (ns)		10	9	14		14	13	23	
Tpd (ns)		30	31	33		37	35	33	

**A03 Counter, Shift-Register Circuit
Characteristic Data and Graphs**

BLOCK DIAGRAM



TRUTH TABLE

SE	RE	SI	RI	Q^{n+1}
1	1	1	1	Q^n
1	1	1	0	0
1	1	0	1	1
1	1	0	0	*
1	0	1	1	Q^n
1	0	1	0	Q^n
1	0	0	1	1
1	0	0	0	1
0	1	1	1	Q^n
0	1	1	0	0
0	1	0	1	Q^n
0	1	0	0	0
0	0	1	1	Q^n
0	0	1	0	Q^n
0	0	0	1	Q^n
0	0	0	0	Q^n

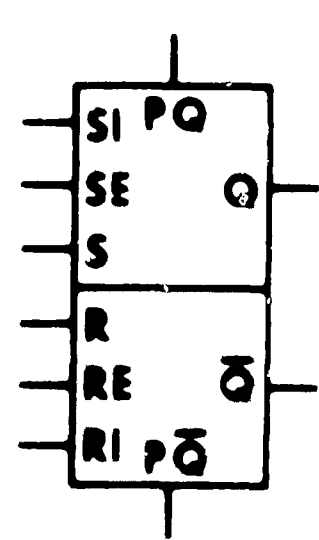
* INDETERMINATE

Each block in the diagram represents a single NAND gate.
Truth table assumes clock input to R and S.

AO3 COUNTER, SHIFT-REGISTER CIRCUIT

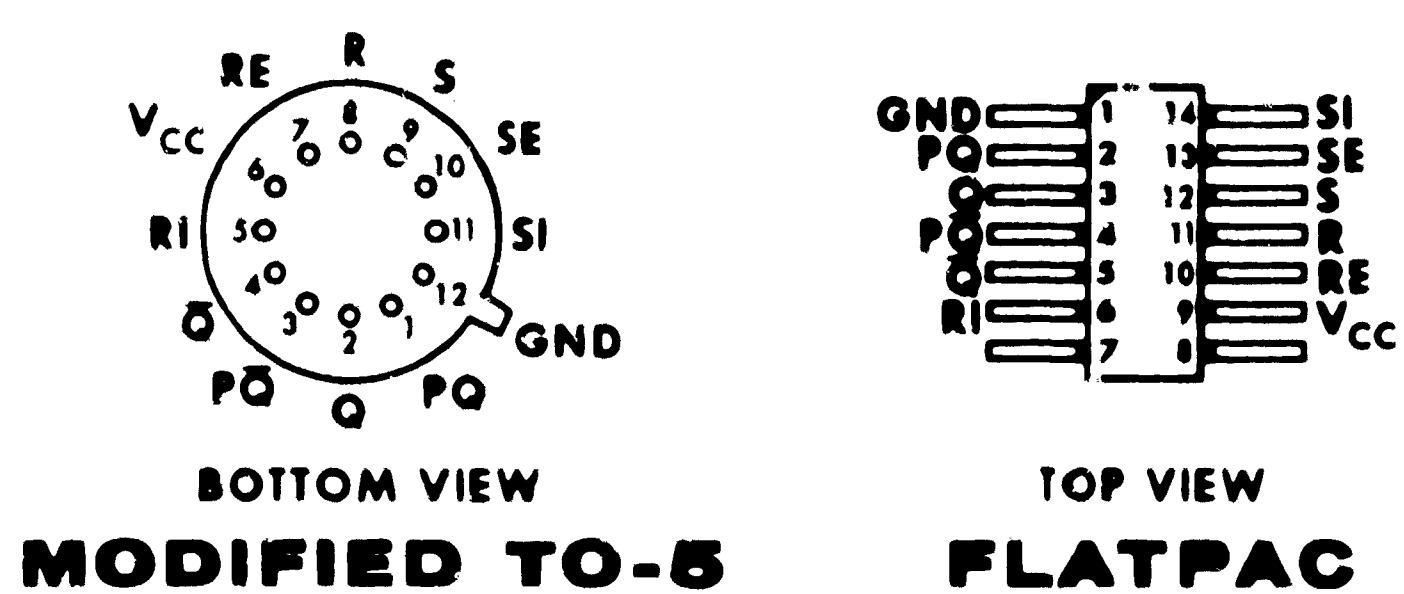
LOGIC DIAGRAM

Figure 3.1.11



- TERMINAL IDENTIFICATION
- SI - SET INHIBIT
 - SE - SET ENABLE
 - S - SET
 - R - RESET
 - RE - RESET ENABLE
 - RI - RESET INHIBIT
 - PQ - PRESET Q
 - PQ-bar - PRESET Q-bar
 - Q, Q-bar - COMPLEMENTARY OUTPUTS

PIN DIAGRAMS



ABSOLUTE MAXIMUM RATINGS AT 25°C

Power Supply Voltage V_{CC}	6 v
Input Voltage BV_i	6 v
Output Voltage BV_o	6 v
Operating Temperature Range T_A	-55 to +125°C
Storage Temperature Range T_s	-65 to +150°C
Output Current	50 ma

Voltage at any pin must be positive with respect to the common terminal.

AO3 COUNTER, SHIFT-REGISTER CIRCUIT

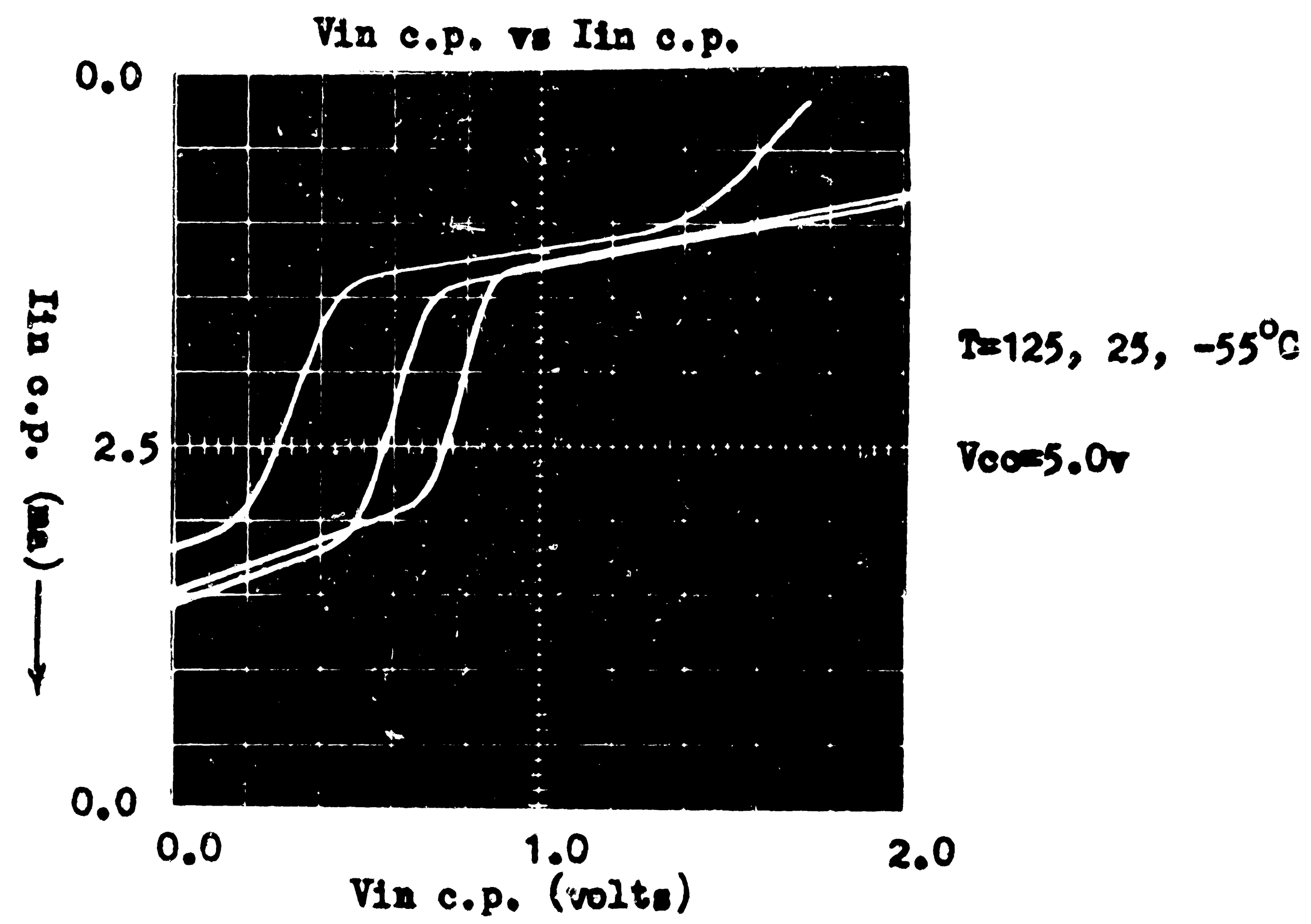
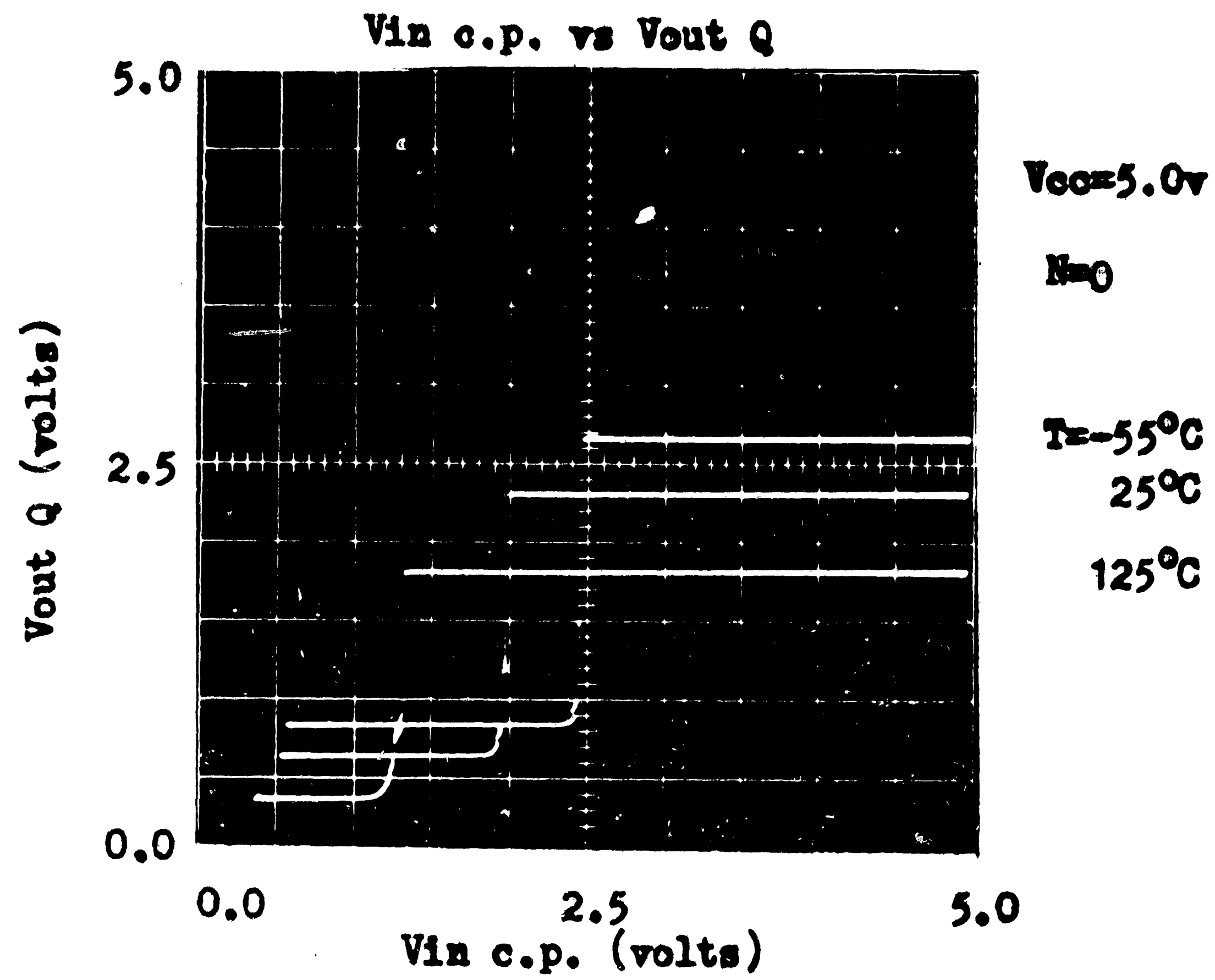
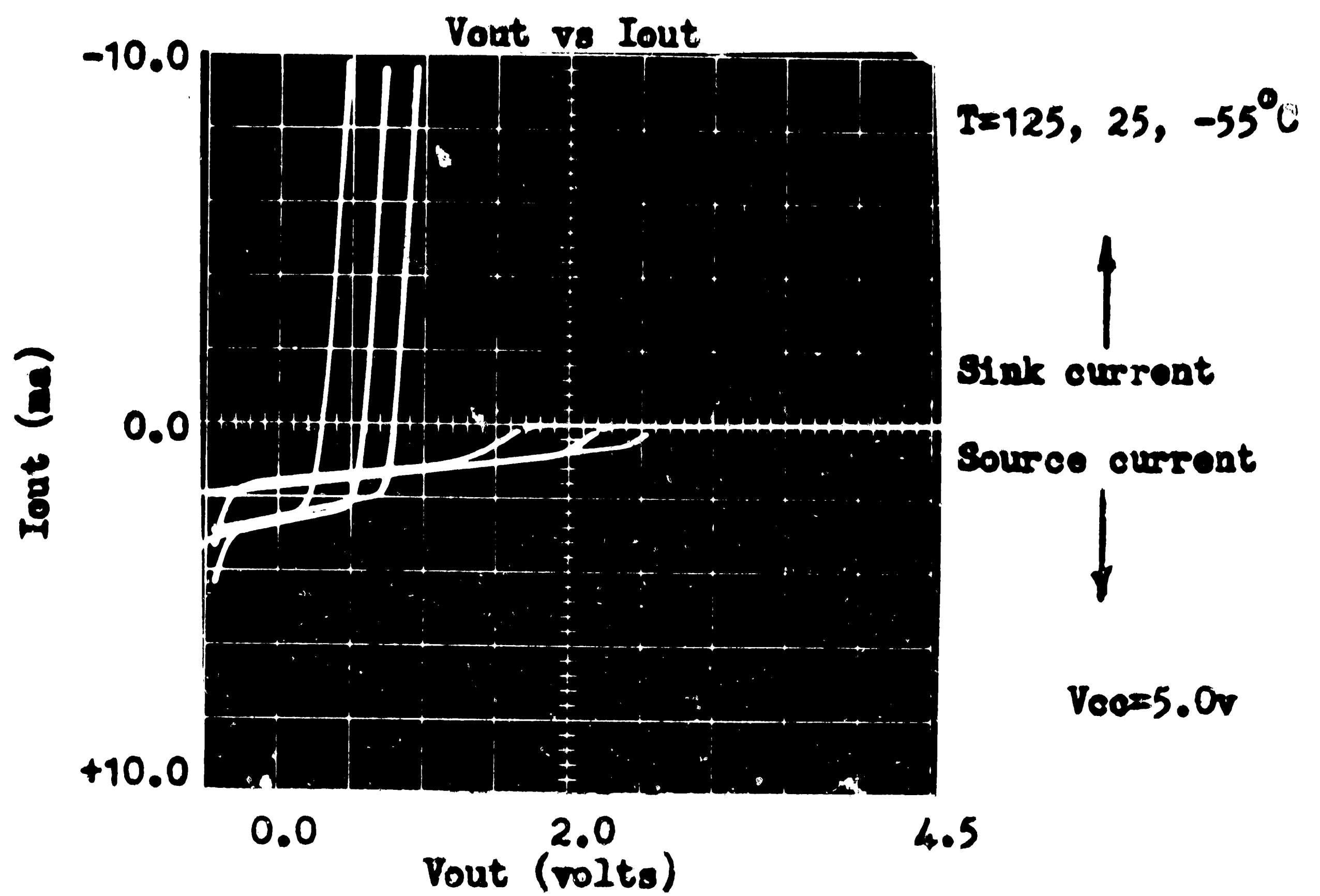


Figure 3.1.12

A03 COUNTER SHIFT-REGISTER CIRCUIT



Both Q and \bar{Q} outputs are shown. Q , in this case, is in the "on" state.

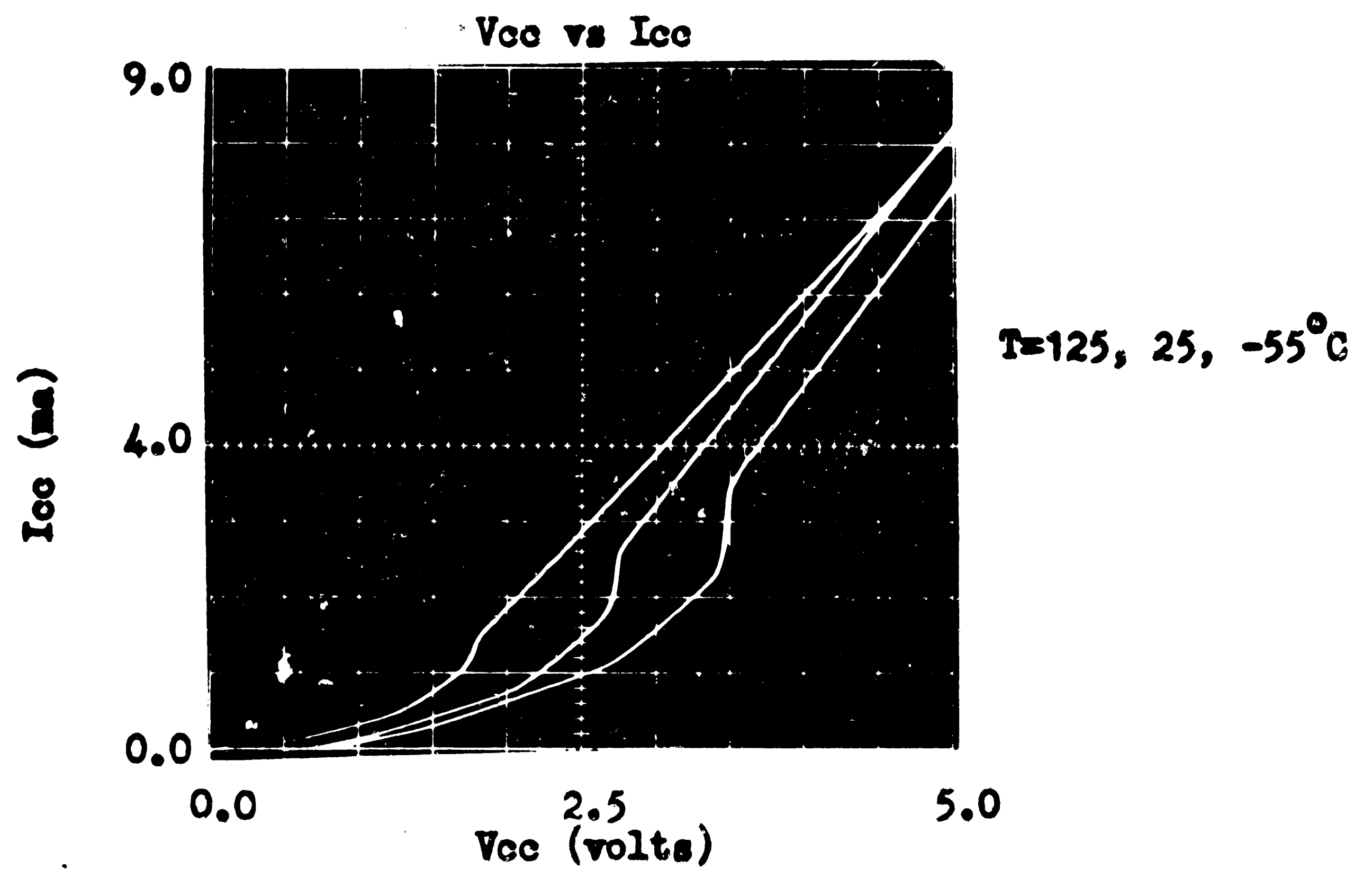
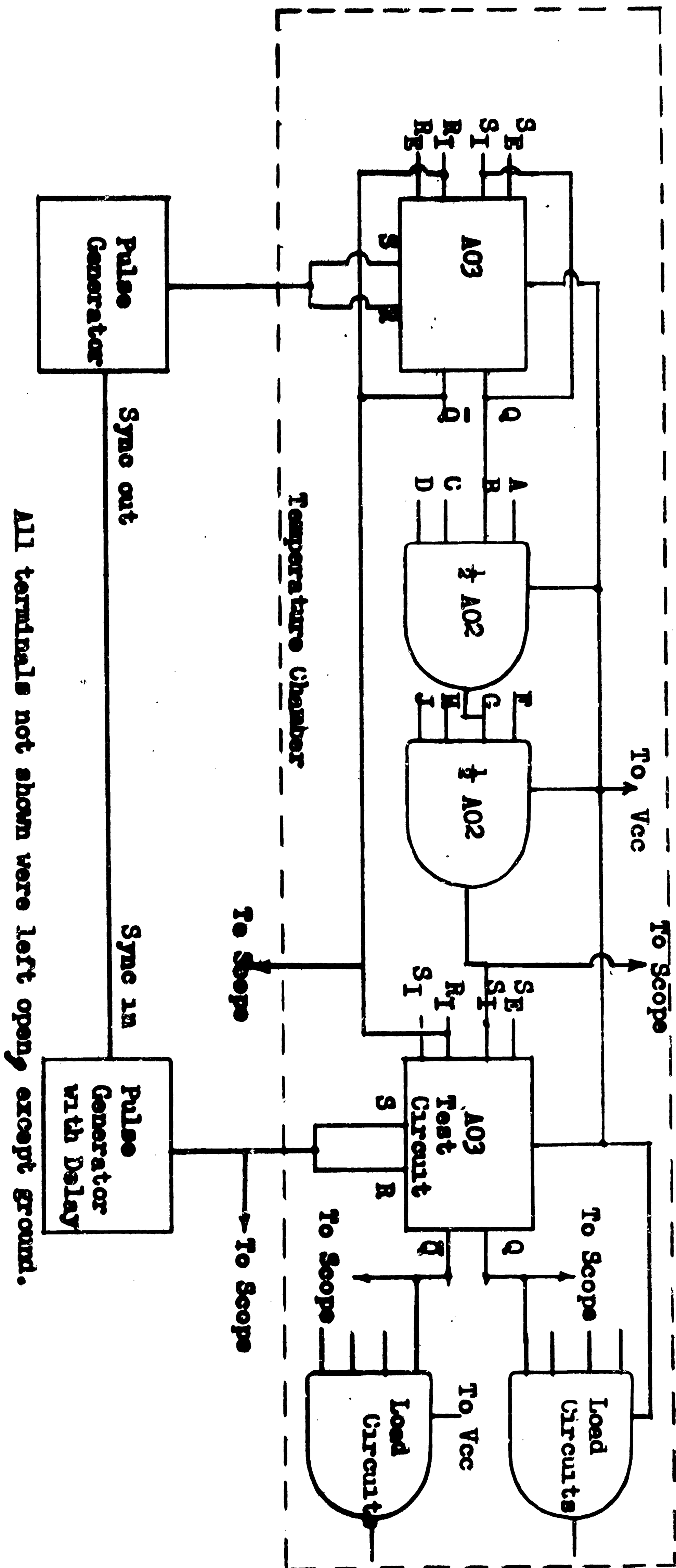
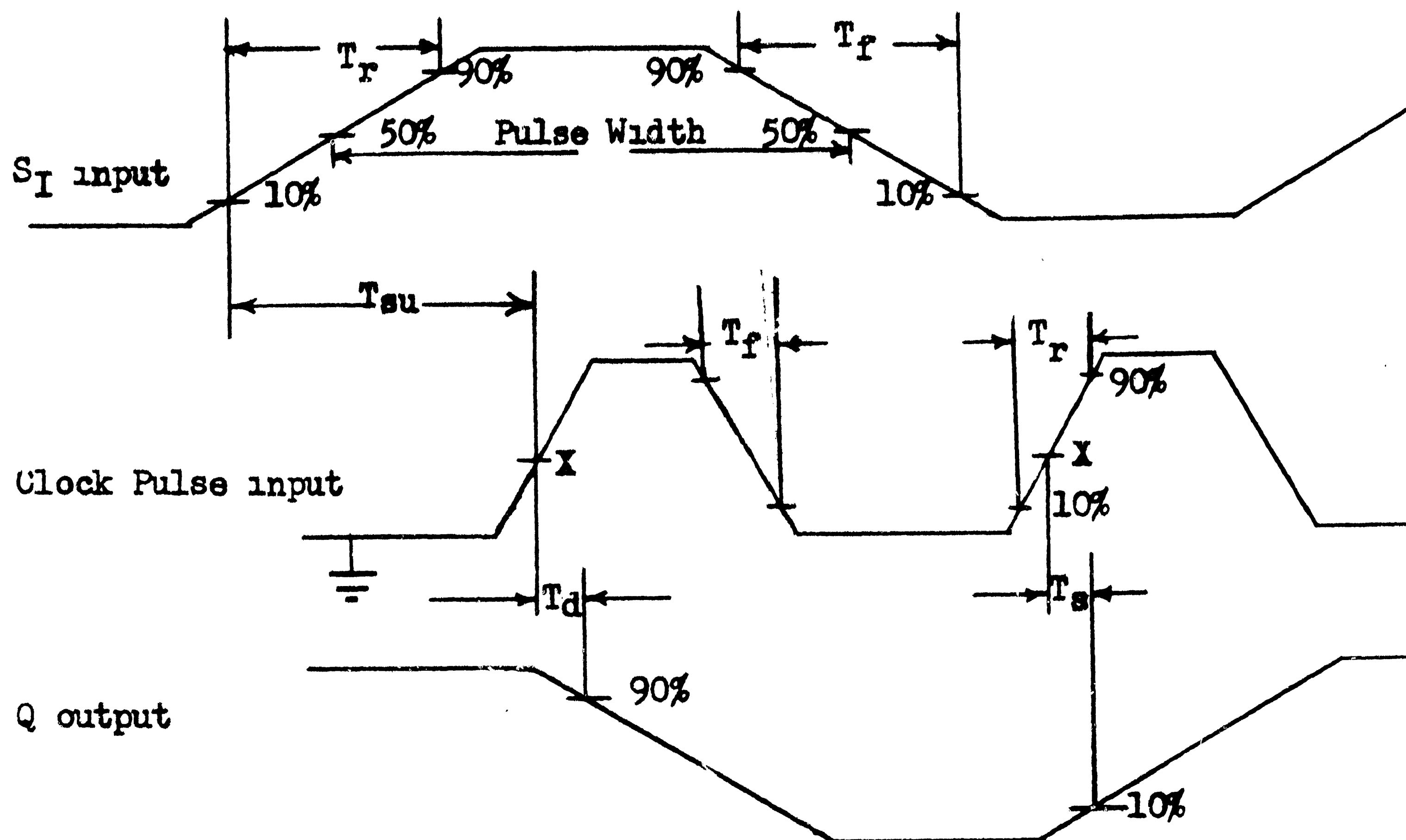


Figure 3.1.13



Test set-up for the A03 counter, shift-register circuit.

Figure 3.1.14



Rise time (T_r), Fall time (T_f), Delay time (T_d),
Storage time (T_s), Set-up time (T_{su})

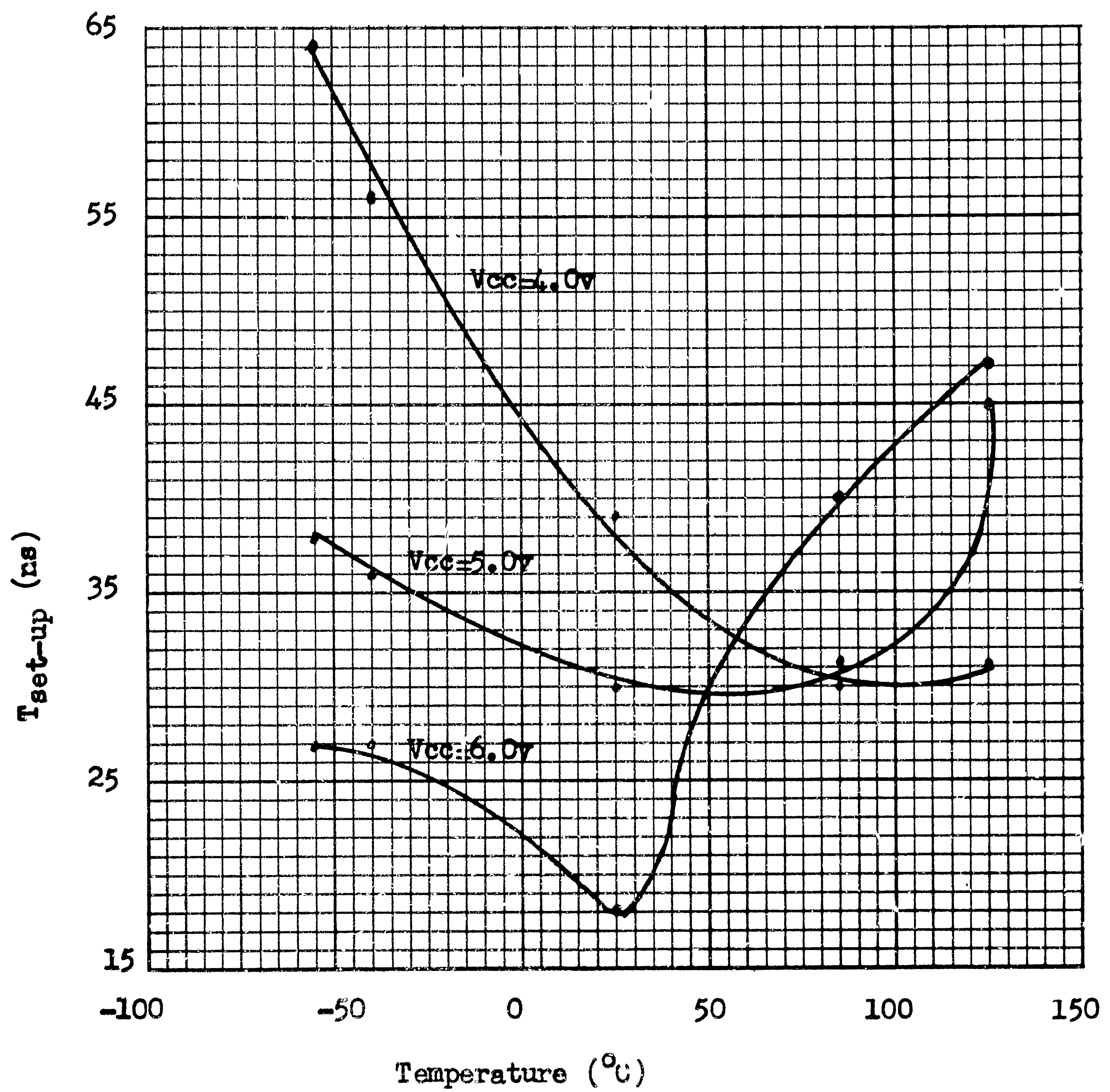
$T^{\circ}C$	-55	-40	25	85	125
X volts	2.5	2.5	2.0	1.3	1.3

A03 Counter-Shift Register Waveform Definition. See notes below.

Figure 3.1.15

NOTE 1: The X voltage points were used instead of percentage points on the clock pulse. This was done because the clock pulse was swinging from ground and not from an offset voltage as would be the case if it had been supplied through a Siliconix driver circuit. The points were determined from the static clock pulse input vs. Q output voltage curves of Figure 12. It should be noted however, that the rise time of the clock pulse was less than 10 ns and therefore the points from which the measurements were made were not critical.

NOTE 2: The criteria used to measure the setup time was as follows. Refer to Figure 13 for the test setup and to Figures 16 and 17 for actual pulse data oscillographs. The clock pulse was moved to the left until a steady state (no toggling) output was observed. At this point the logic and clock pulse input was similar to that shown in Figure 18. The clock pulse was then slowly moved to the right until toggling was observed and the discontinuity in the logic input vanished. The setup time was measured at this point.



AO3 Counter, Shift-Register. Set-up time vs temperature with V_{cc} as a parameter. $M=1$.

Figure 3.1.16

A03 COUNTER, SHIFT-REGISTER CIRCUIT

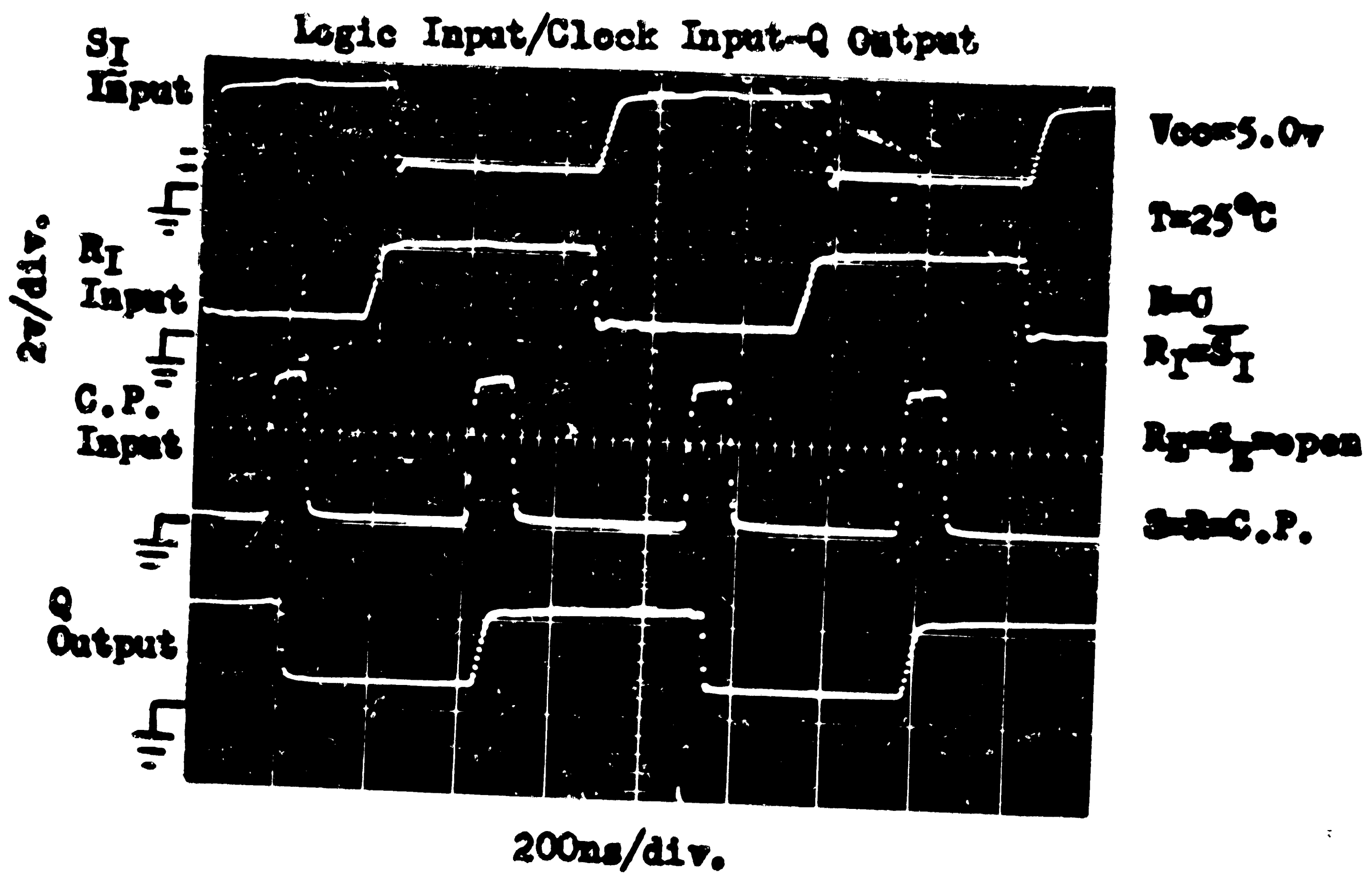
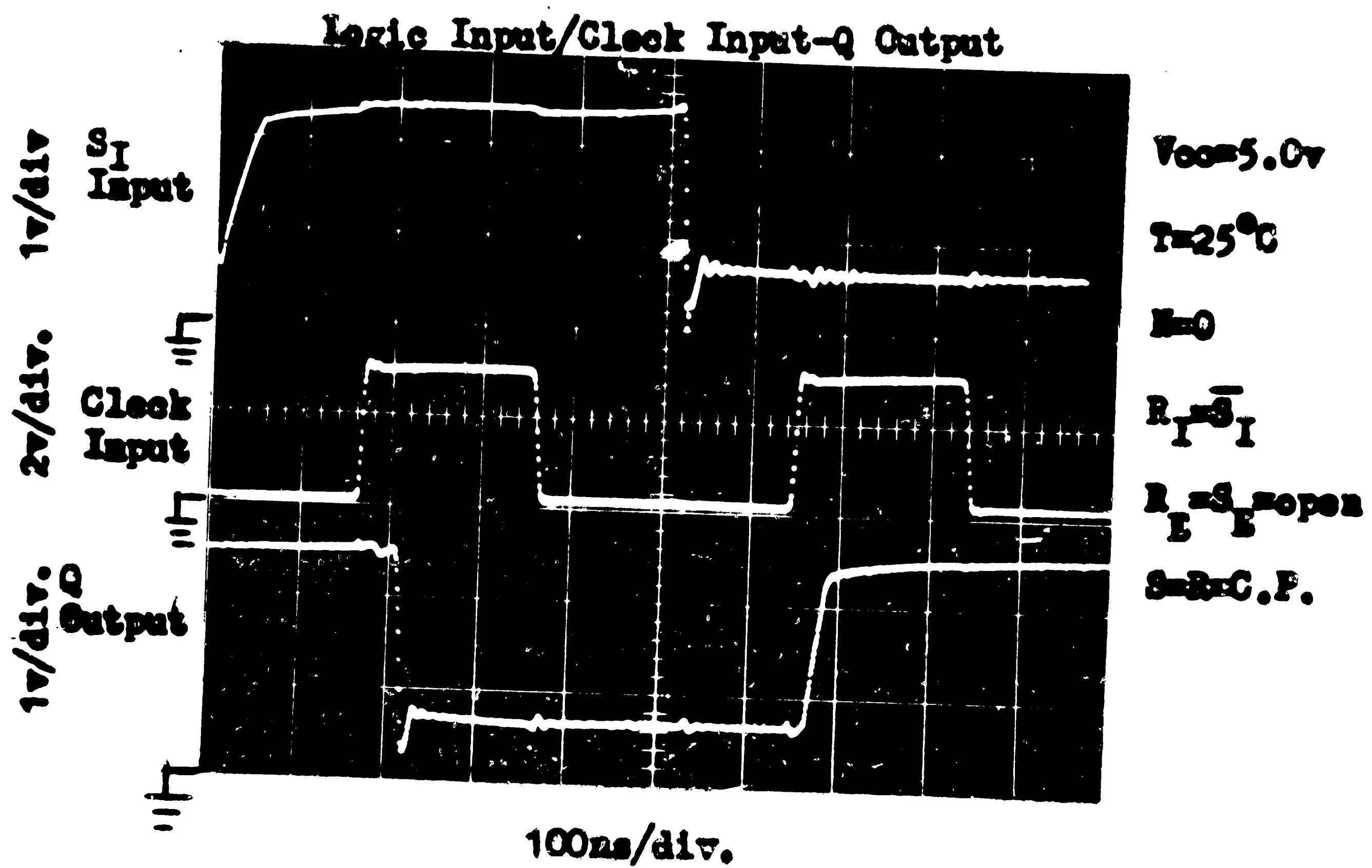
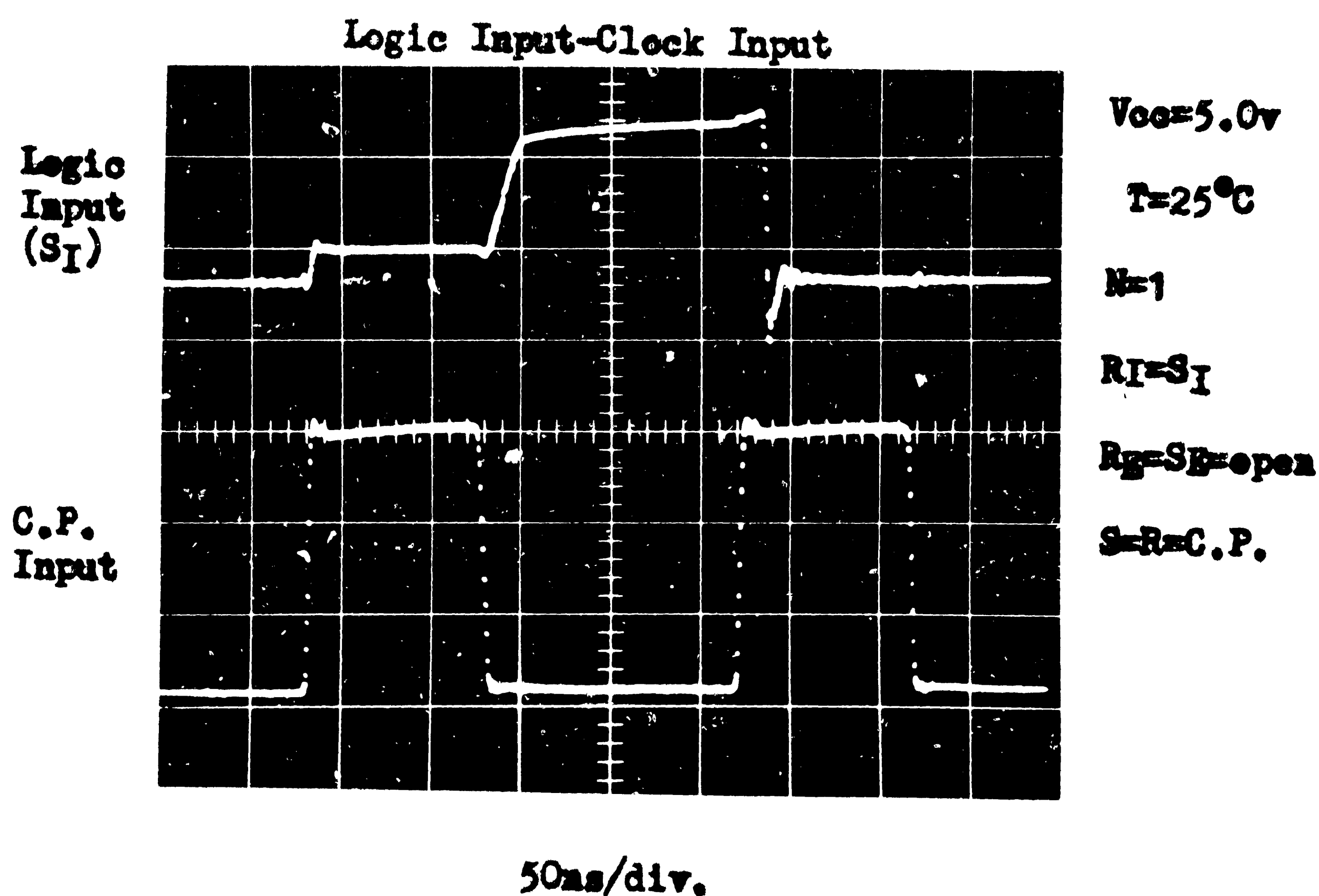


Figure 3.1.17

AO3 COUNTER, SHIFT REGISTER CIRCUIT



Oscilloscope shows the effect of applying the clock pulse too soon after the logic input.
 See paragraph III.A.4.

Figure 3.1.18

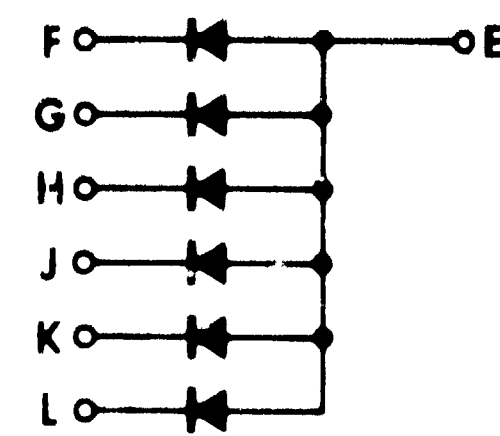
Circuit Designation		Vcc 4.0 Volts, Clock Pulse Rep. Rate 2 Mc									
		A03									
Temperature		-55°C					-40°C				
Test Circuit:		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input
				N=1	N=5			N=1	N=5		
Pulse Amplitude (V _{pp})		1.8	3.0	1.7	1.7	1.8	3.0	1.7	1.7	1.6	3.0
Pulse Width (ns) 50-50%		546	200	454	455	539	200	458	459	526	200
T _r (ns) 10 to 90%		101	7	48	45	77	7	42	36	64	7
T _f (ns) 90 to 10%		10	8	22	55	8	8	16	41	6	7
T _d (ns) X to 10%				104	101			89	88		
T _s (ns) X to 90%				51	52			48	46		
T Set Up 10% to X			64				56				39
Temperature		85°C					125°C				
Test Circuit:		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input
				N=1	N=5			N=1	N=5		
Pulse Amplitude (V _{pp})		1.5	3.0	1.5	1.4	1.4	3.0	1.4	1.4		
Pulse Width (ns) 50-50%		515	200	468	476	520	200	498	505		
T _r (ns) 10 to 90%		65	7	32	28	78	6	46	46		
T _f (ns) 90 to 10%		5	7	7	12	7	7	7	15		
T _d (ns) X to 10%				55	54			55	53		
T _s (ns) X to 90%				26	26			24	23		
T Set Up 10% to X			30				31				
Temperature		Minimum Vcc=4.0 at -55°C =3.5 at 25°C =2.7 at 125°C N=5									
Test Circuit:		Minimum clock pulse width =65ns at -55°C =34ns at 25°C =48ns at 125°C N=5									
Pulse Amplitude (V _{pp})		The minimum parameter measurements were taken at the point just above that necessary to produce toggling on the output. X _{cp} =2.5v at -40 and -55°C =2.0v at 25°C =1.3v at 85 and 125°C									

Circuit Designation		A03										Vcc 5.0 Volts, Clock Pulse Rep. Rate 2 MC									
Temperature		-55°C					-40°C					25°C									
Test Circuit:		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input
				N = 1	N = 5			N = 1	N = 5					N = 1	N = 5			N = 1	N = 5		
Pulse Amplitude (V _{pp})		1.9	3.0	1.9	1.8	1.9	3.0	1.9	1.8	1.9	3.0	1.7	3.0	1.7	1.7	1.7	3.0	1.7	1.7		
Pulse Width (ns) 50-50%		512	200	474	469	512	200	477	474	506	200	474	200	480	478	478	200	480	478		
T _r (ns) 10 to 90%		52	6	25	22	49	6	24	22	40	6	22	6	23	19	19	6	23	19		
T _f (ns) 90 to 10%		5	8	8	17	5	8	7	15	4	8	15	8	6	11	11	8	6	11		
T _d (ns) X to 10%				58	58			54	54			54		45	45	45		45	45		
T _s (ns) X to 90%				29	29			27	27			27		21	21	21		21	21		
T Set Up 10% to X			38								36		30								
Temperature		85°C					125°C														
Test Circuit:		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Q Output	
				N = 1	N = 5			N = 1	N = 5			N = 1	N = 5			N = 1	N = 5			N = 1	N = 5
Pulse Amplitude (V _{pp})		1.6	3.0	1.6	1.5	1.5	3.0	1.5	1.5	1.5	3.0	1.5	1.5	1.5	1.5	1.5	3.0	1.5	1.5		
Pulse Width (ns) 50-50%		518	200	480	476	520	200	477	476	520	200	477	476	476	476	476	200	477	476		
T _r (ns) 10 to 90%		61	6	31	28	75	6	51	57	75	6	51	57	57	57	57	6	51	57		
T _f (ns) 90 to 10%		5	8	6	12	6	8	8	15	6	8	8	15	15	15	15	8	8	15		
T _d (ns) X to 10%				47	47			54	52			54	52	52	52	52		54	52		
T _s (ns) X to 90%				21	21			19	20			19	20	20	20	20		19	20		
T Set Up 10% to X			31				45														
		Minimum clock pulse width = 31 ns at -55°C = 23 ns at 25°C = 53 ns at 125°C N=5 X = 2.5vp at -40 and -55°C = 2.0vp at 25°C = 1.3vp at 85 and 125°C																			

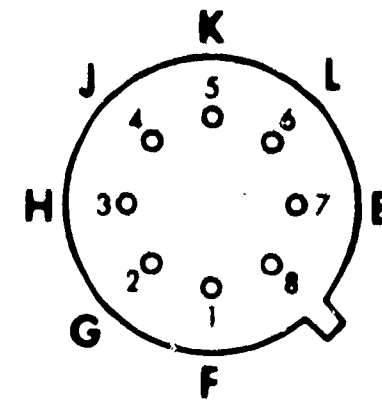
Circuit Designation A03										
Vcc 6.0 Volts, Clock Pulse Rep. Rate 2 Mc										
Temperature	-55°C					-40°C				
Test Circuit:	Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input
			N = 1	N = 5			N = 1	N = 5		
Pulse Amplitude (V _{pp})	2.1	3.0	2.0	1.9	2.0	3.0	2.0	1.9	1.9	3.0
Pulse Width (ns) 50-50%	511	200	493	477	509	200	481	478	507	200
T _r (ns) 10 to 90%	37	6	19	16	35	7	19	15	32	7
T _f (ns) 90 to 10%	4	7	6	13	3	7	5	11	3	8
T _d (ns) x to 10%			41	41			38	39		
T _s (ns) x to 90%			26	28			15	17		
T Set Up 10% to x		27				27			18	
Temperature	85°C					125°C				
Test Circuit:	Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input	Q Output		Logic Input	C.P. Input
			N = 1	N = 5			N = 1	N = 5		
Pulse Amplitude (V _{pp})	1.8	3.0	1.7	1.7	1.6	3.0	1.6	1.6		
Pulse Width (ns) 50-50%	515	200	497	477	519	200	467	481		
T _r (ns) 10 to 90%	64	7	37	40	69	7	52	64		
T _f (ns) 90 to 10%	5	7	6	13	6	7	8	16		
T _d (ns) x to 10%			49	46			53	50		
T _s (ns) x to 90%			16	16			17	17		
T Set Up 10% to x		40				47				
Minimum clock pulse width = < 23ns at -55°C = < 23ns at 25°C = 53ns at 125°C N=5 x _{ep} = 2.5vp at -40 and -55°C = 2.0vp at 25°C = 1.3vp at 85 and 125°C										

A04 Diode Array
Characteristic Data and Graphs

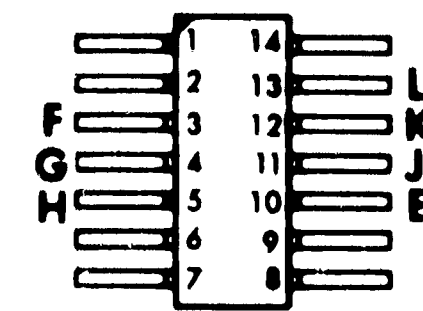
CIRCUIT DIAGRAM



PIN DIAGRAMS



BOTTOM VIEW
MODIFIED TO-5

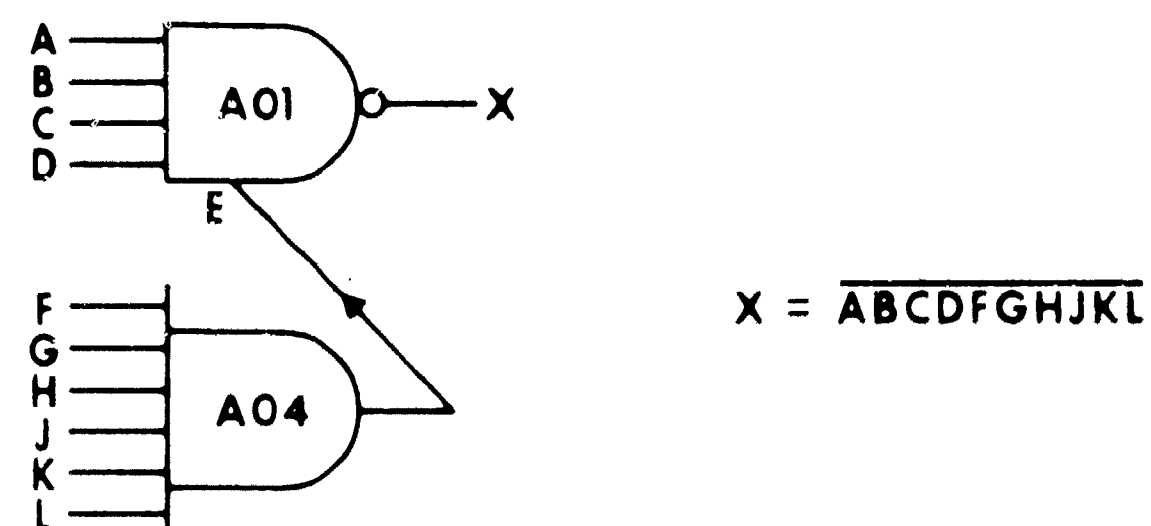


TOP VIEW
FLAT PAC

A04 DIODE ARRAY

LOGIC DIAGRAM

The diode array is represented here in the normal application of expanding the inputs of a single NAND gate.

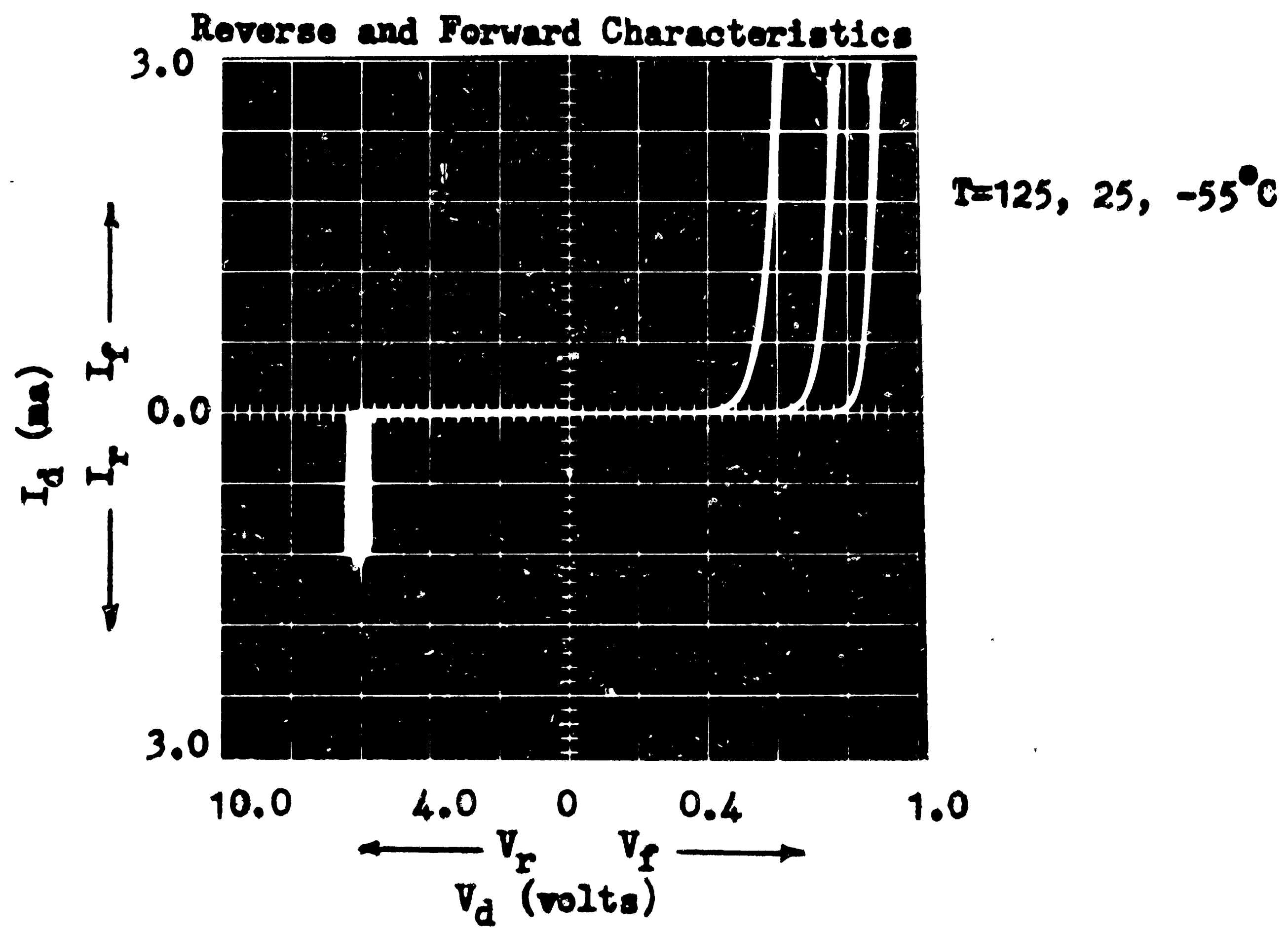


ABSOLUTE MAXIMUM RATINGS

Breakdown Voltage BV	—55 to 125°C	6 v
Operating Temperature Range T _A	—55 to +125°C	
Storage Temperature Range T _S	—65 to +150°C	

Figure 3.1.19

AO4 DIODE ARRAY

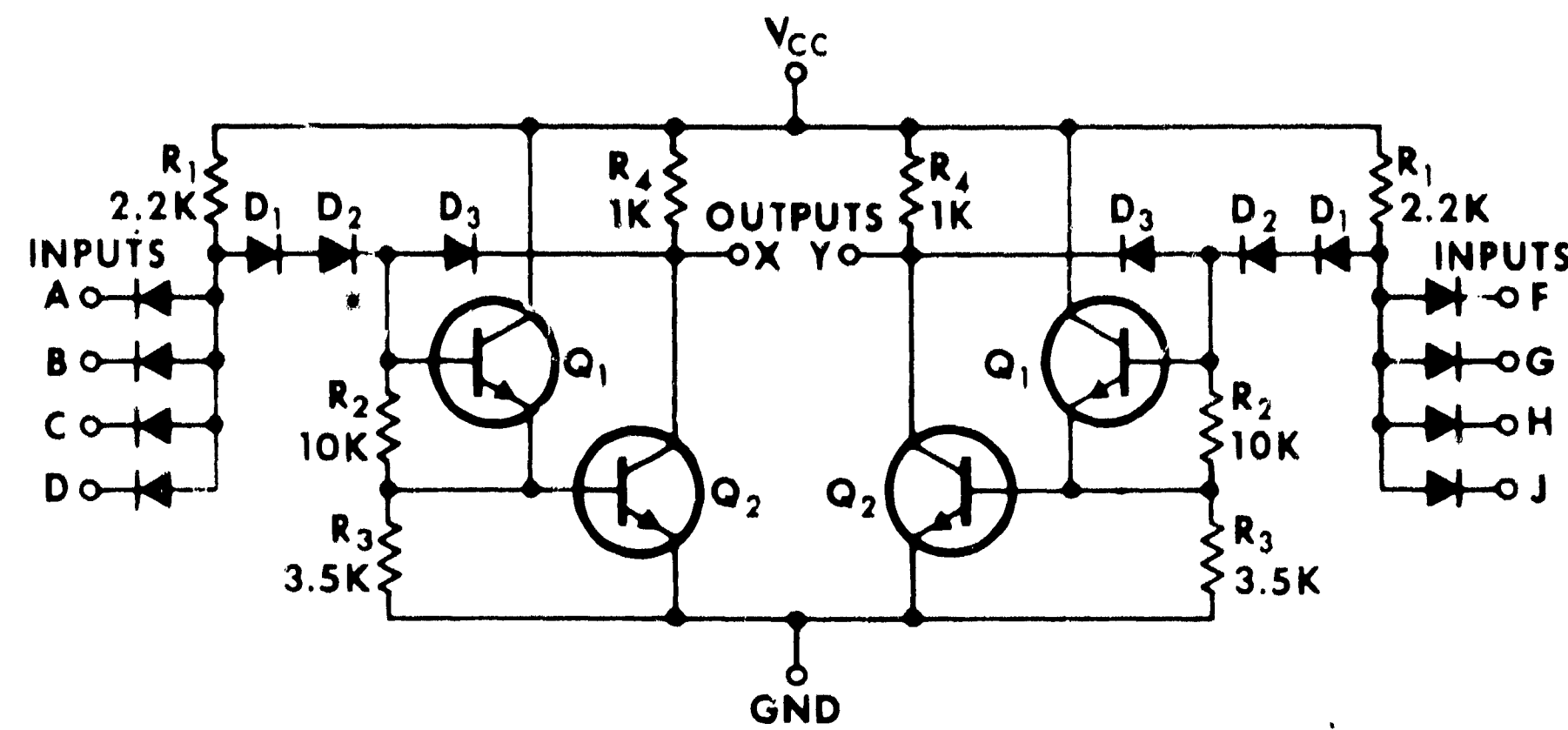


This is the only data obtained for this device.

Figure 3.1.20

A05 Dual Line Driver
Characteristic Data and Graphs

CIRCUIT DIAGRAM

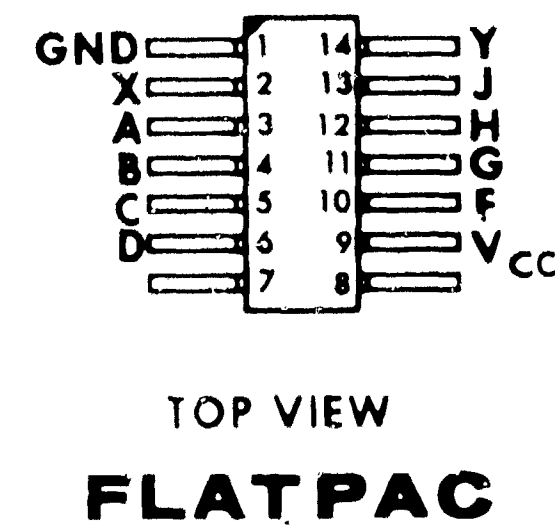
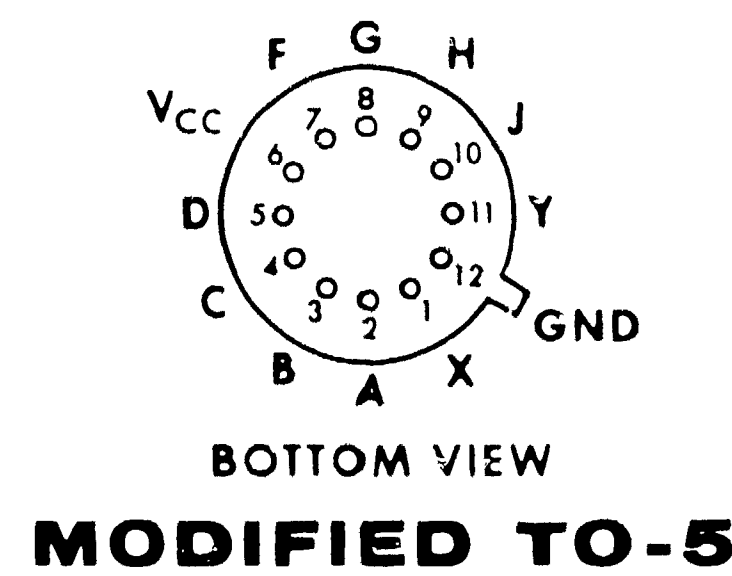


DUAL GATE

A05 Dual Line Driver

Figure 3.1.21

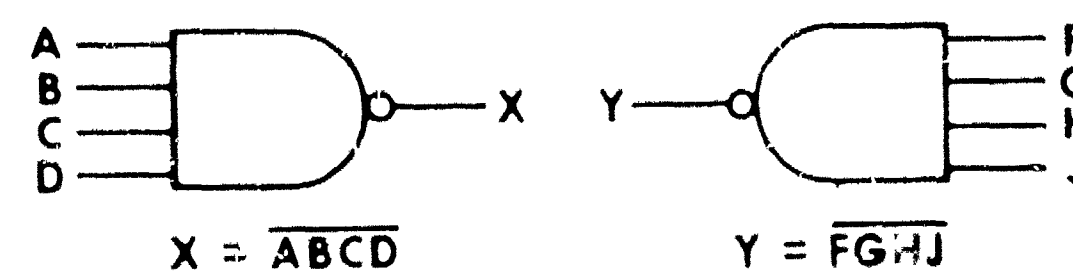
PIN DIAGRAMS



MODIFIED TO-5

FLATPAC

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS AT 25°C

Power Supply Voltage V_{CC}	6 v
Input Voltage BV_i	6 v
Output Voltage BV_o	6 v
Operating Temperature Range T_A	-55 to +125°C
Storage Temperature Range T_S	-65 to +150°C
Output Current	50 ma

Voltage at any pin must be positive with respect to the common terminal.

A05 DUAL LINE DRIVER

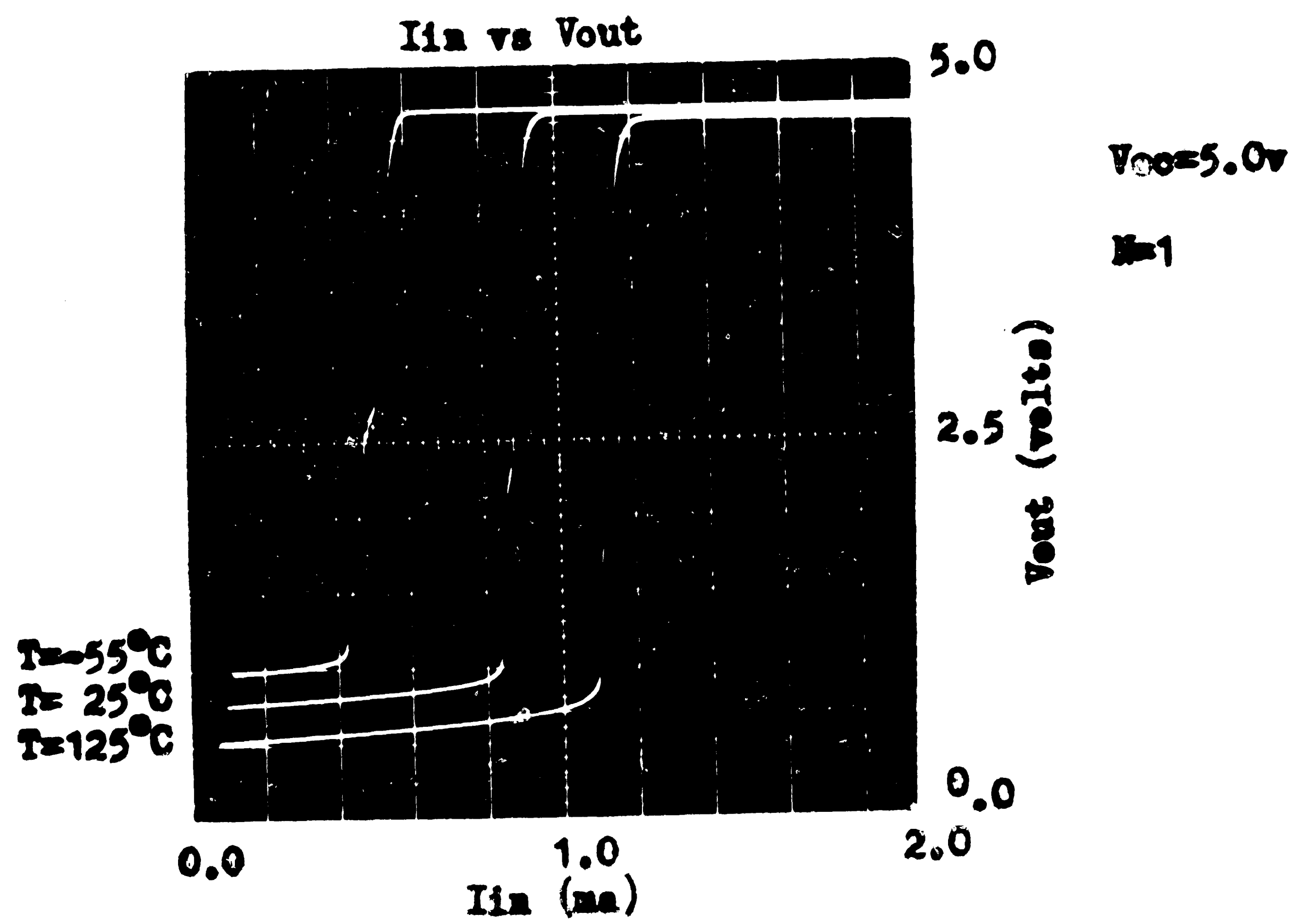
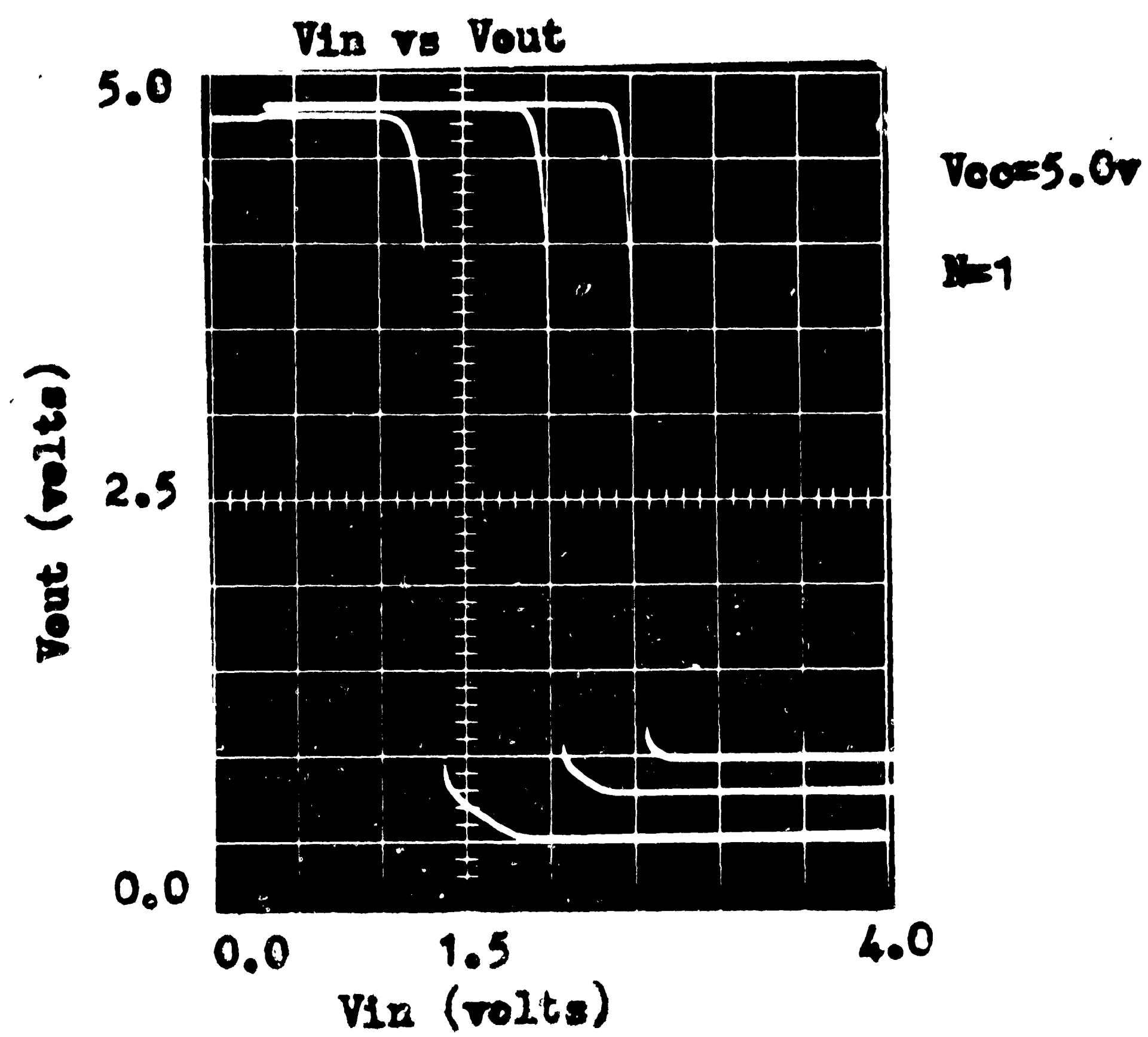


Figure 3.1.22

A05 DUAL LINE DRIVER

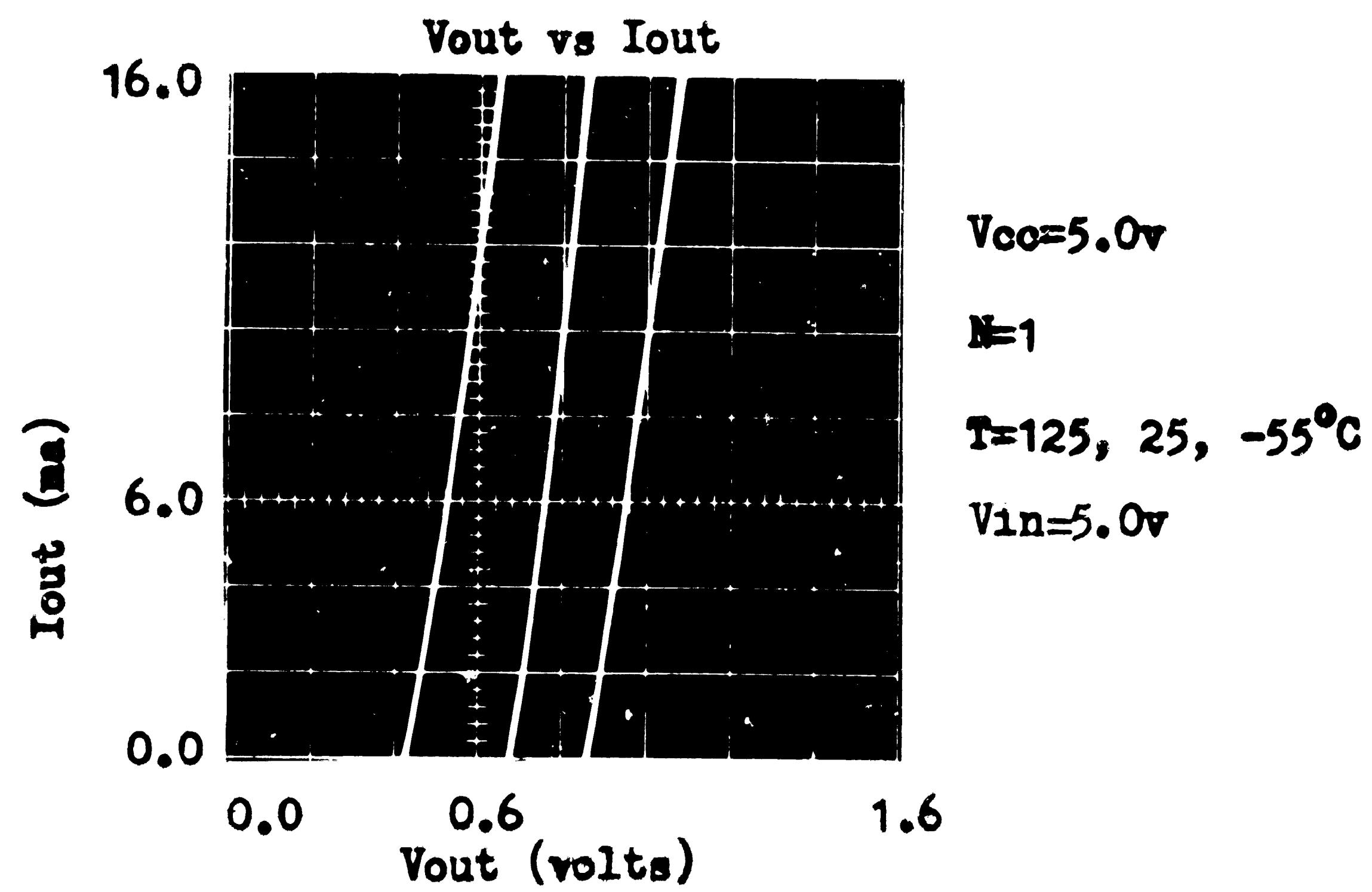
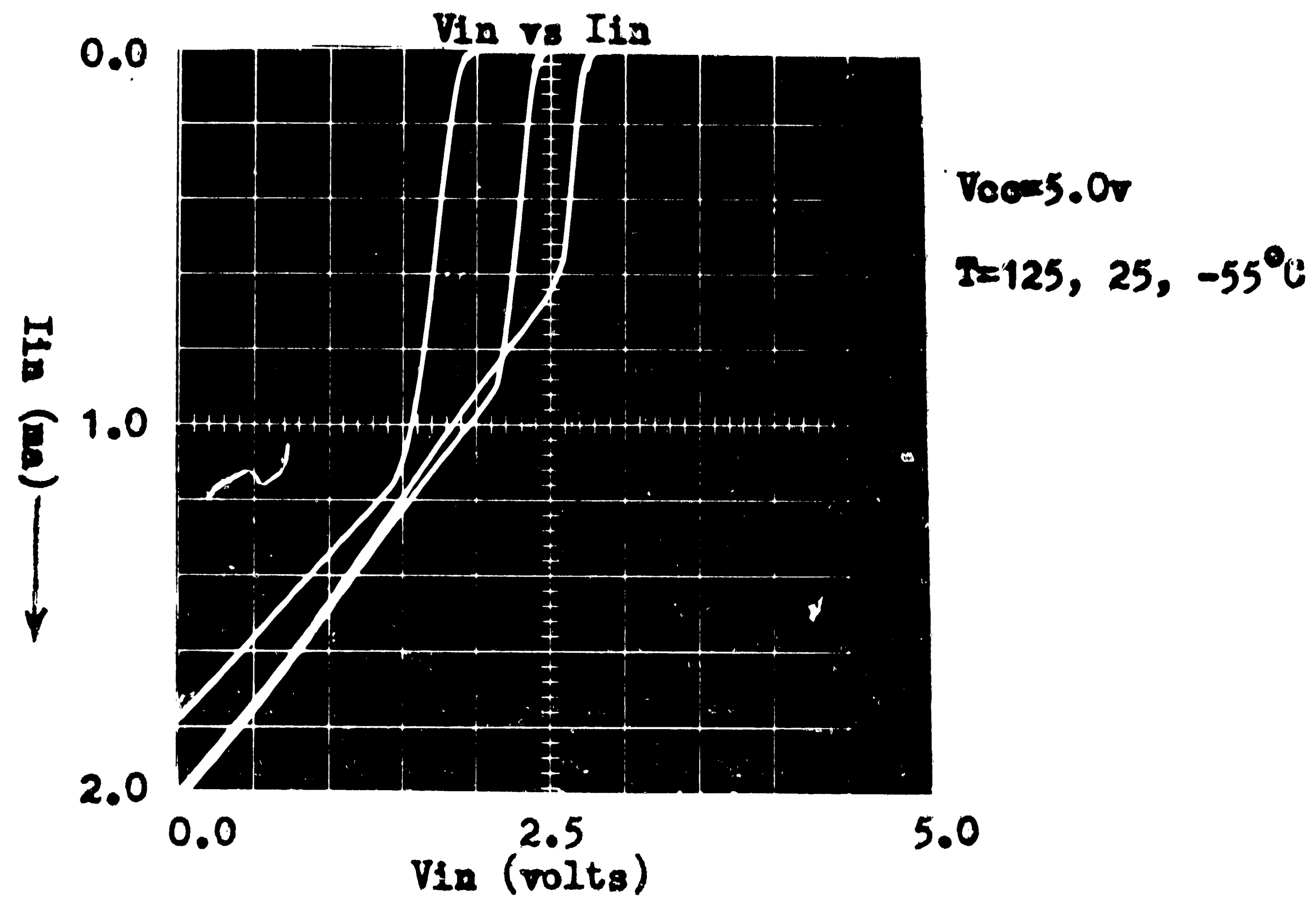
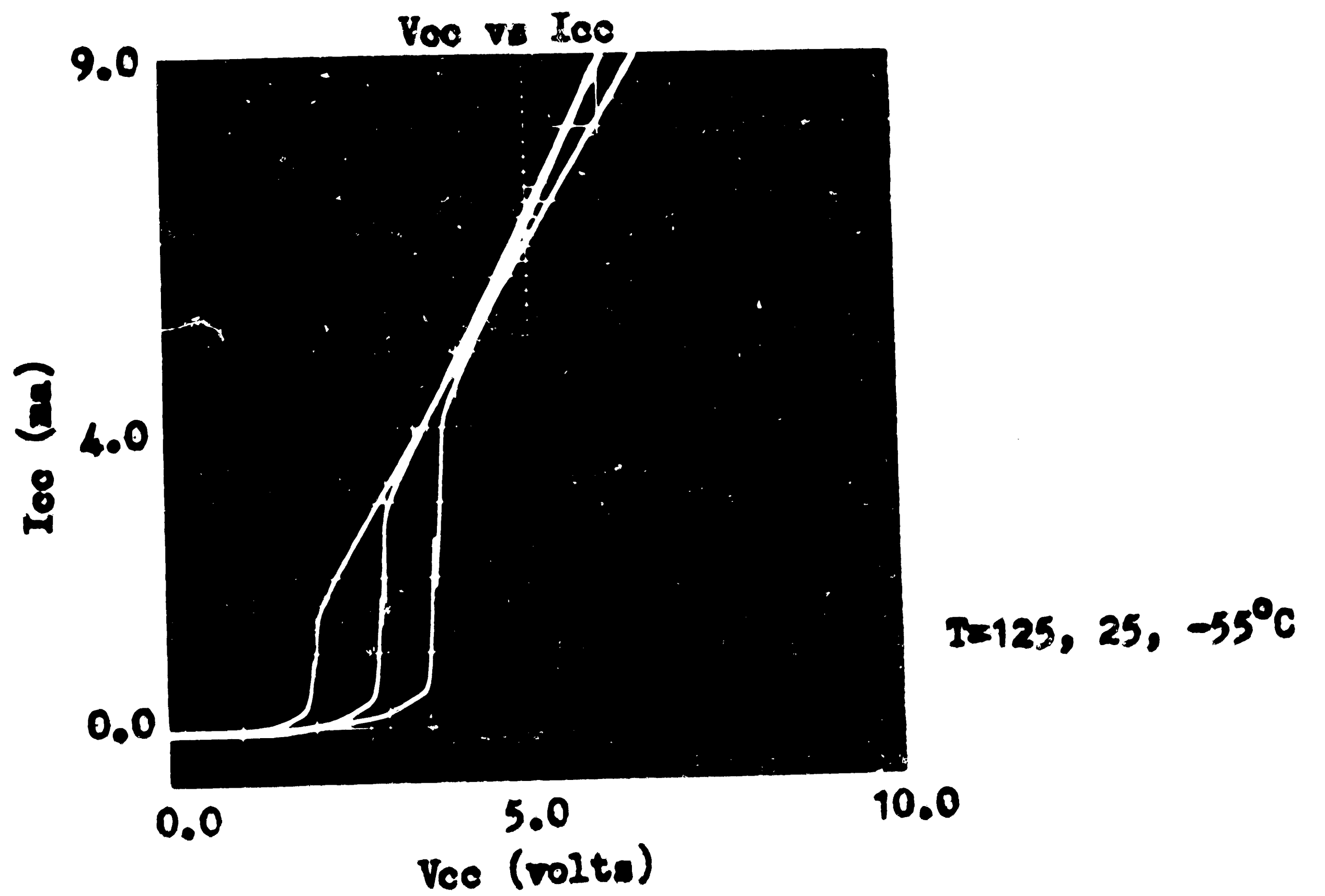
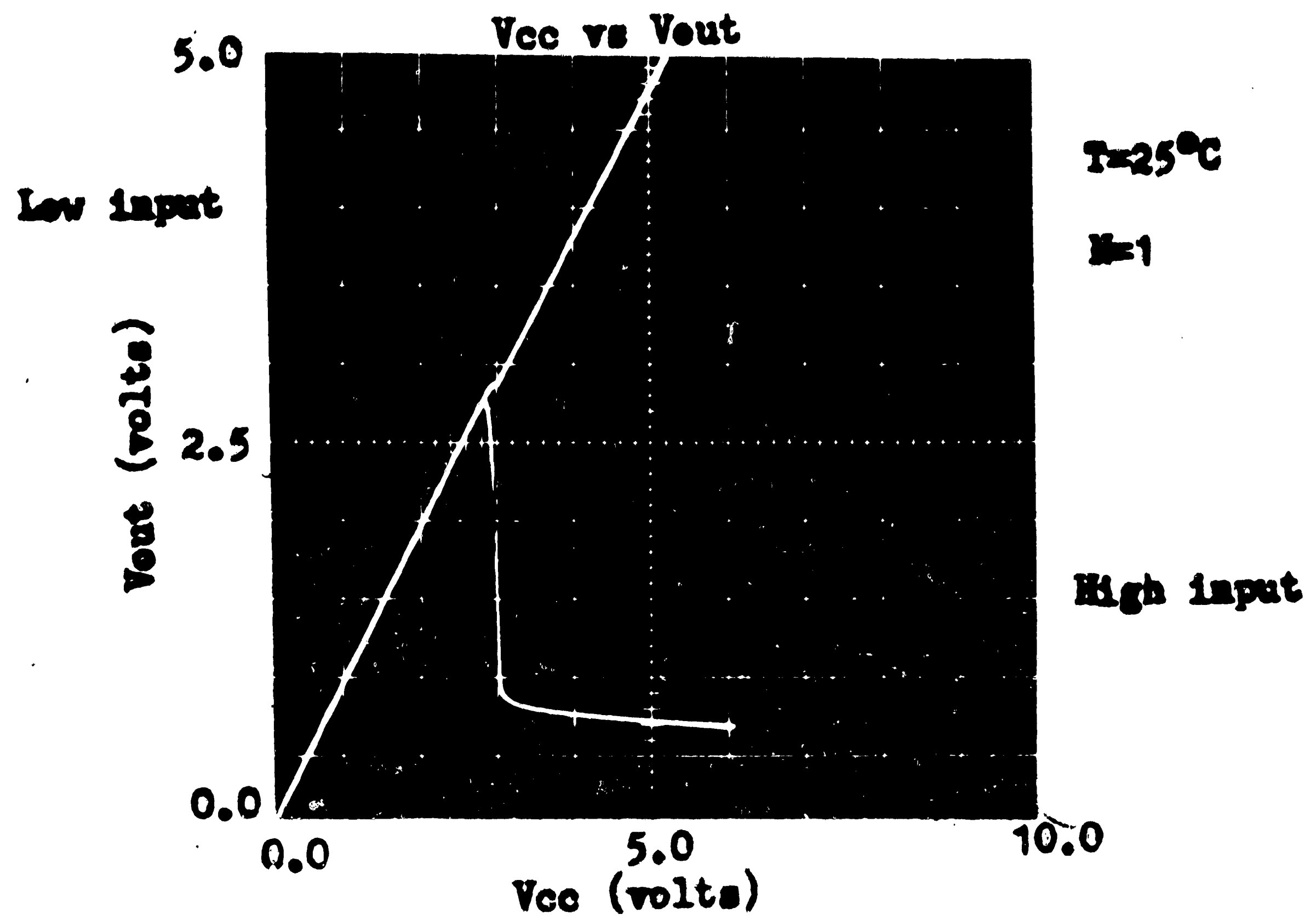
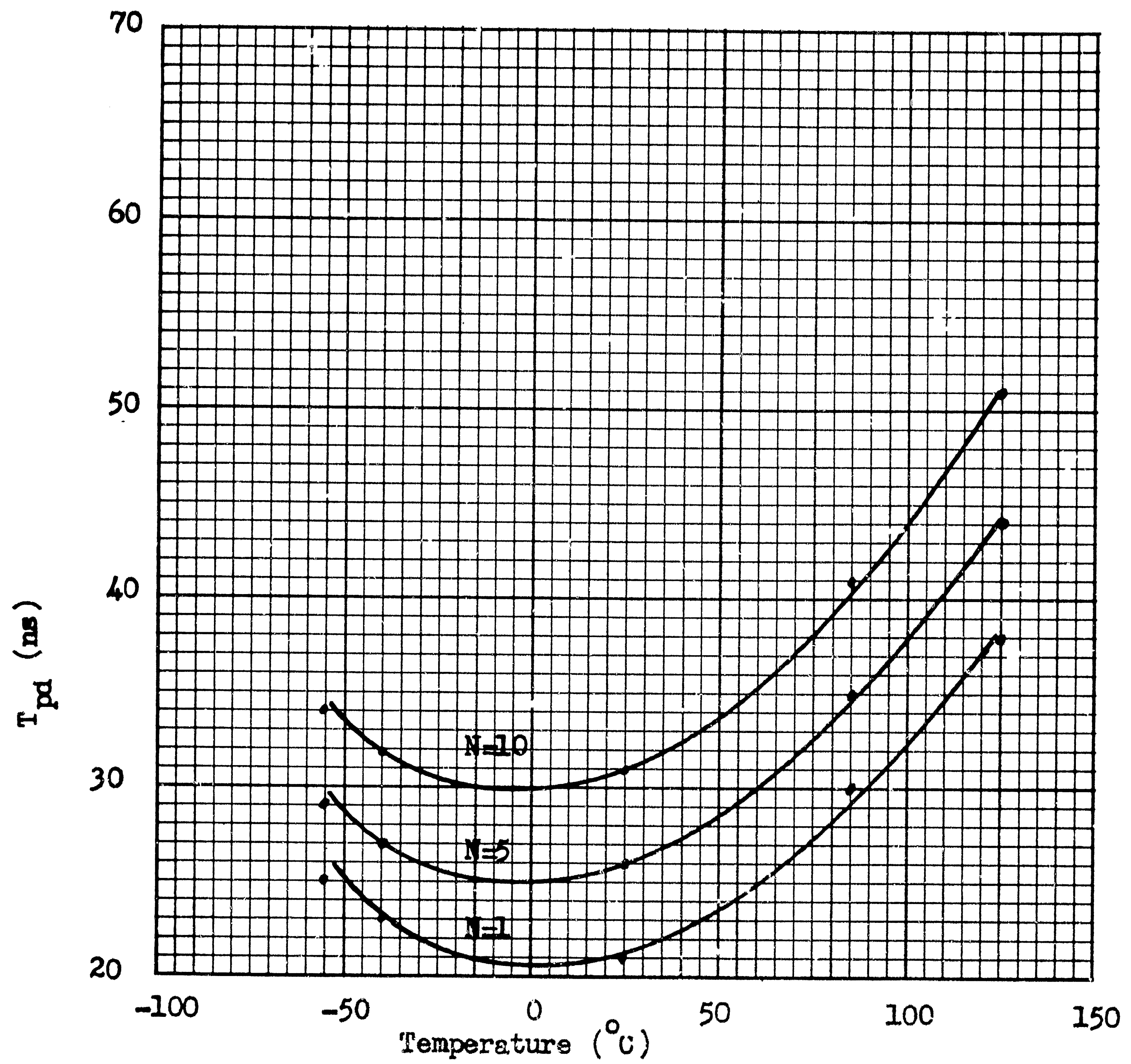


Figure 3.1.23

A05 DUAL LINE DRIVER



See the Vcc vs Icc curve of the A02 circuit for an explanation of the above curve. Figure 3.1.24



A05 Dual Line Driver. Propagation delay vs temperature with the number of loads (N) as a Parameter. $V_{cc}=5.0v$

Figure 3.1.25

A05 DUAL LINE DRIVER

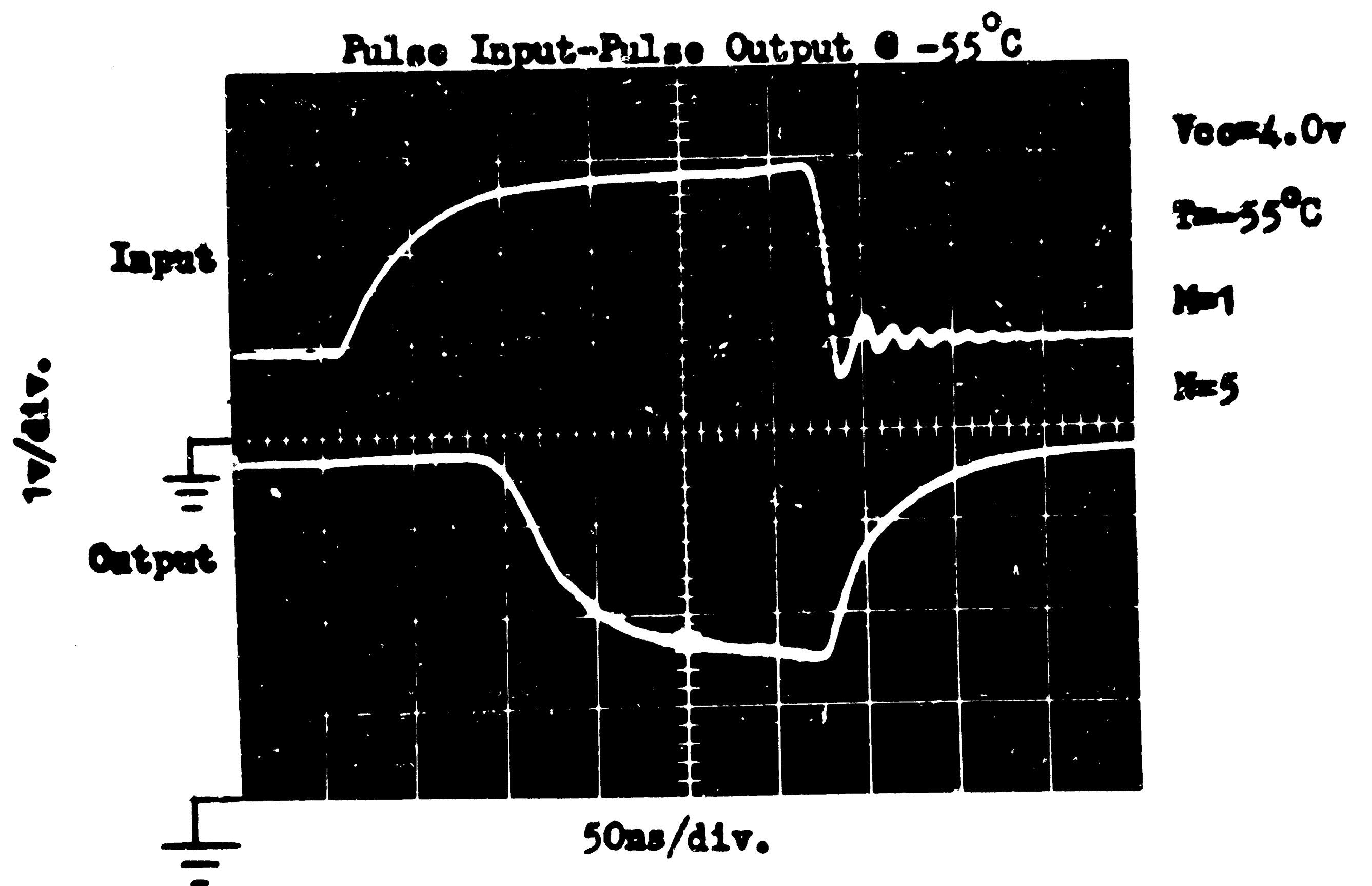
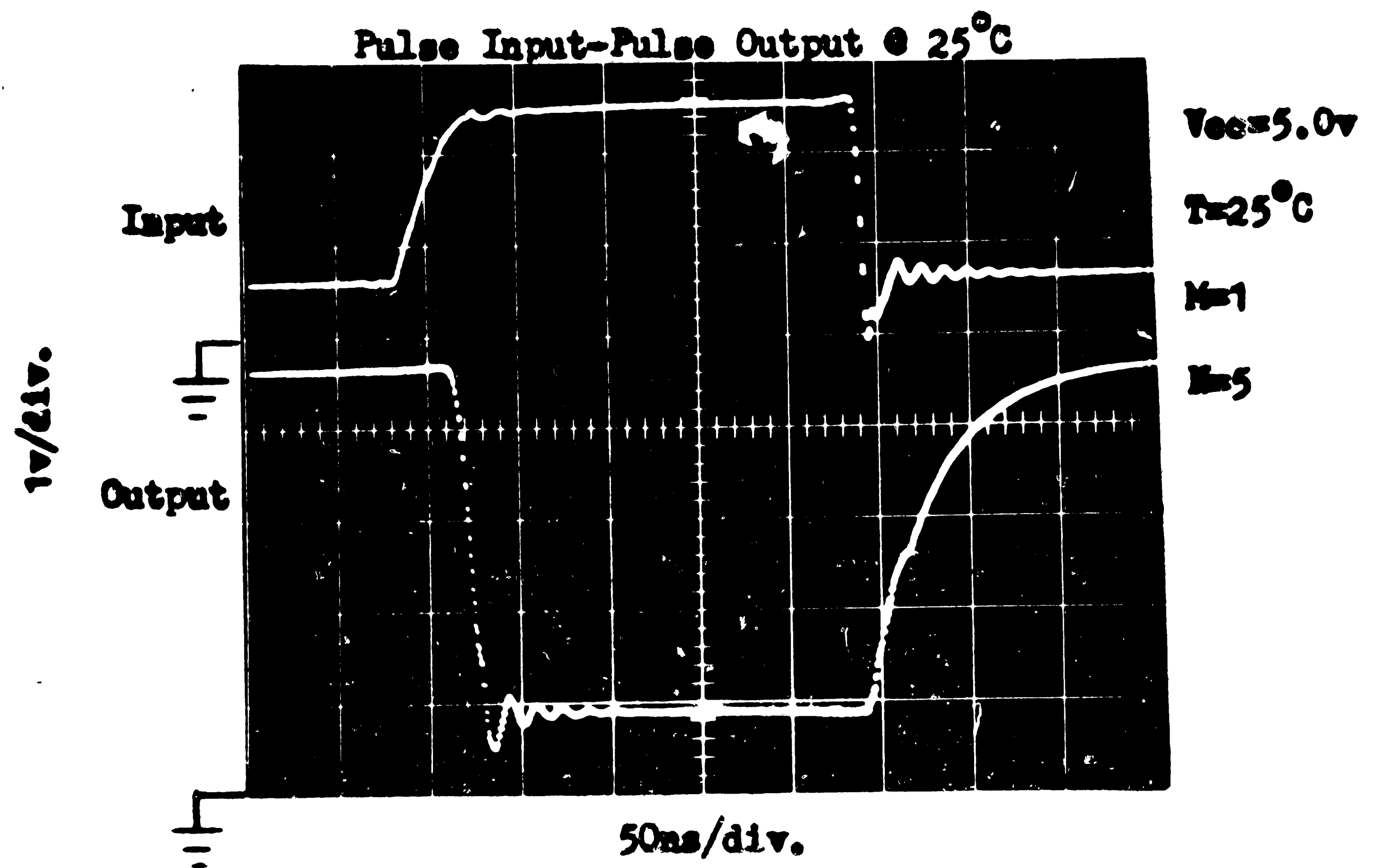


Figure 3.1.26

A05 DUAL LINE DRIVER

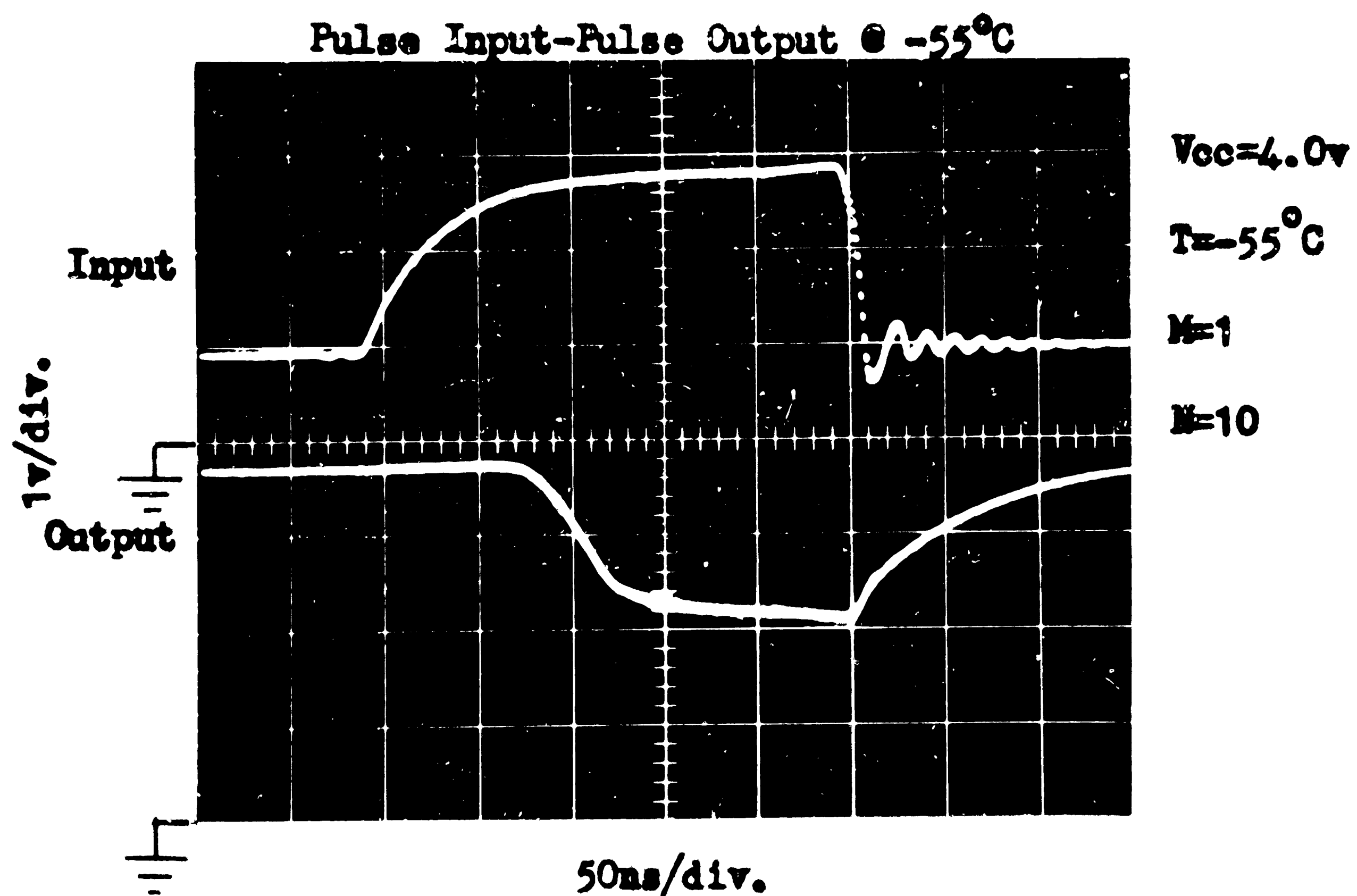
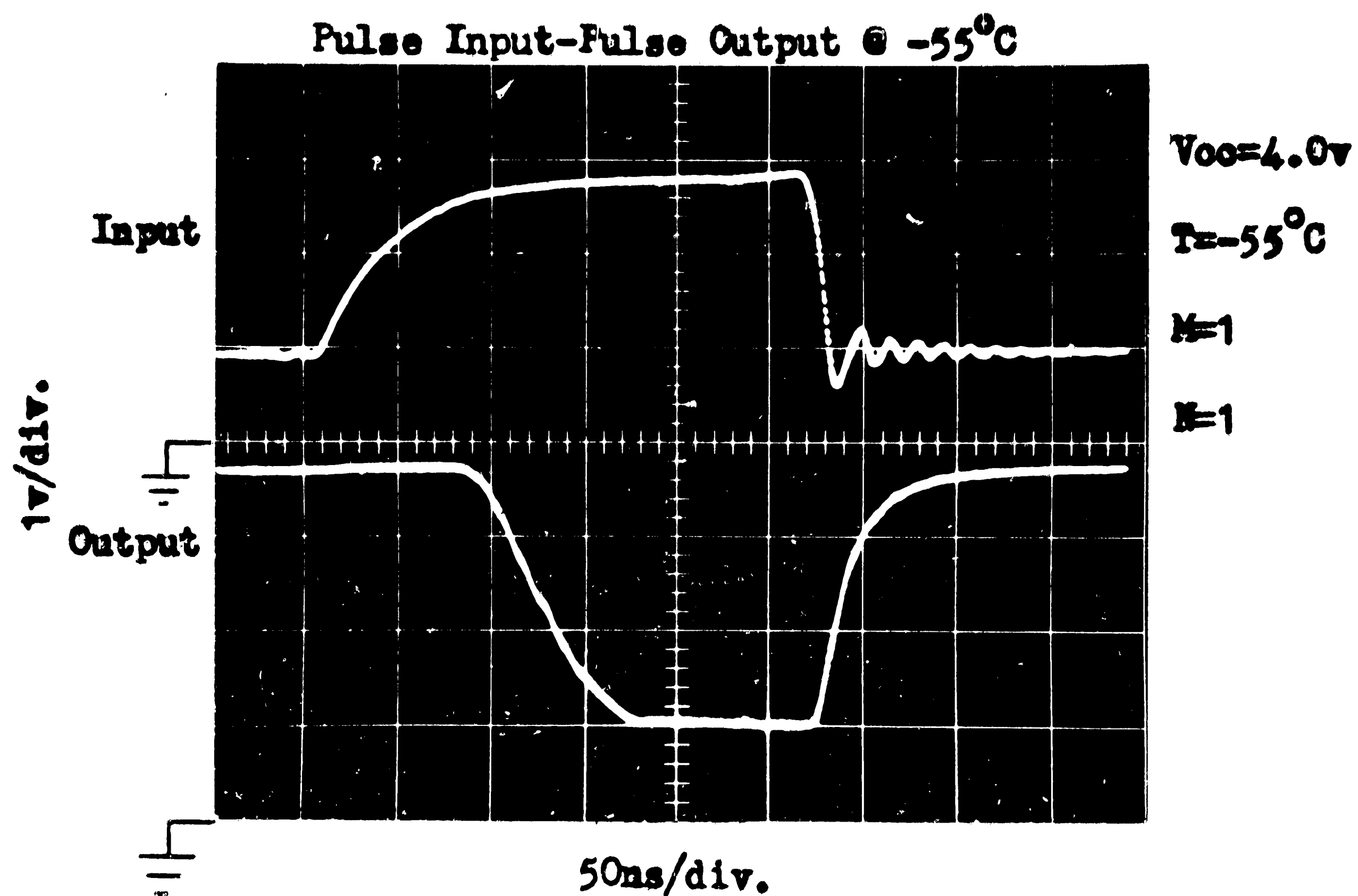


Figure 3.1.27

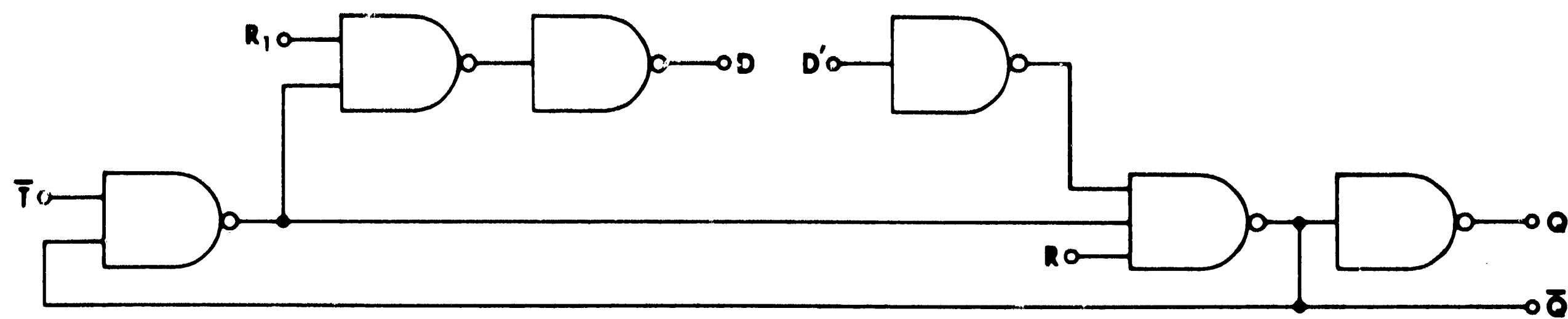
Circuit Designation A05 , Fan-In 1 , Vcc 4.0 Volts, Input Pulse Rep. Rate 1 MC									
Temperature		-55°C			-40°C			25°C	
Test Circuit:		Output @ N =			Output @ N =			Input	
		1	5	10	1	5	10	Output @ N =	
Pulse Amplitude (V _{pp})		1.9	2.8	2.8	1.9	2.8	2.2	1.8	3.0
Pulse Width (ns)		250	171	179	250	191	200	250	232
T _r (ns)		82	44	85	73	45	119	50	83
T _f (ns)		9	60	84	8	35	77	6	14
T _d (ns)			90	92		75	77		44
T _s (ns)			6	6		6	7		8
T _{pd} (ns)			56	57		42	50		25
Temperature		85°C			125°C				
Test Circuit:		Output @ N =			Output @ N =				
		1	5	10	1	5	10		
Pulse Amplitude (V _{pp})		1.7	3.0	3.0	1.6	3.1	3.0		
Pulse Width (ns)		250	248	256	250	268	285		
T _r (ns)		66	55	94	72	74	157		
T _f (ns)		6	11	14	6	11	15		
T _d (ns)			59	60		62	62		
T _s (ns)			9	10		12	15		
T _{pd} (ns)			25	29		33	43		

Circuit Designation A05 , Fan-In 1 , Vcc 5.0 Volts, Input Pulse Rep. Rate 1 MC													
Temperature	-55°C					-40°C				25°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =			Input	Output @ N =			
		1	5	10		1	5	10		1	5	10	
Pulse Amplitude (V _{pp})	2.1	3.9	3.8	3.7	2.0	3.9	3.8	3.7	1.9	4.1	4.0	3.9	
Pulse Width (ns)	250	232	239	244	250	235	242	250	250	248	257	264	
T _r (ns)	40	47	82	119	37	46	79	118	32	50	85	124	
T _f (ns)	5	14	20	30	5	12	17	23	4	9	12	14	
T _d (ns)		41	40	42		37	38	38		30	30	30	
T _s (ns)		7	8	8		7	8	8		8	8	9	
T _{pd} (ns)		25	29	34		23	27	32		21	26	31	
Temperature	85°C					125°C							
Test Circuit:	Input	Output @ N =			Input	Output @ N =			Input	Output @ N =			
		1	5	10		1	5	10		1	5	10	
Pulse Amplitude (V _{pp})	1.8	4.0	4.1	4.0	1.6	4.2	4.1	4.0					
Pulse Width (ns)	250	271	278	287	250	283	296	308					
T _r (ns)	54	68	105	150	69	68	109	167					
T _f (ns)	5	8	10	12	6	10	11	13					
T _d (ns)		50	51	52		63	63	64					
T _s (ns)		12	13	13		31	33	27					
T _{pd} (ns)		30	35	41		38	44	51					

Circuit Designation AO5 , Fan-In 1 , Vcc 6.0 Volts, Input Pulse Rep. Rate 1 MC												
Temperature			-55°C			-40°C			25°C			
Test Circuit:			Output @ N =			Input			Output @ N =			Input
			1	5	10				1	5	10	
Pulse Amplitude (V _{pp})	2.3		4.8	4.8	4.7	2.2			4.9	4.8	4.7	2.0
Pulse Width (ns)	250		244	248	261	250			246	252	262	250
T _r (ns)	27		46	80	119	25			46	79	118	30
T _f (ns)	4		10	14	19	4			9	12	16	4
T _d (ns)			29	30	30				27	28	28	
T _s (ns)			7	8	8				7	8	8	
T _{pd} (ns)			20	26	31				20	25	30	
Temperature			85°C			125°C						
Test Circuit:			Output @ N =			Input			Output @ N =			Input
			1	5	10				1	5	10	
Pulse Amplitude (V _{pp})	1.9		5.1	4.1	5.0	1.7			5.1	4.1	5.0	
Pulse Width (ns)	250		281	292		250			289	303	319	
T _r (ns)	57		61	99	151	73			71	112	164	
T _f (ns)	5		8	9	10	7			10	11	12	
T _d (ns)			53	53	54				66	67	68	
T _s (ns)			28	30	23				34	34	35	
T _{pd} (ns)			33	35	46				39	47	55	

**A08 Monostable Multivibrator
Characteristic Data and Graphs**

BLOCK DIAGRAM



A08 Monostable Multivibrator

PIN DIAGRAMS

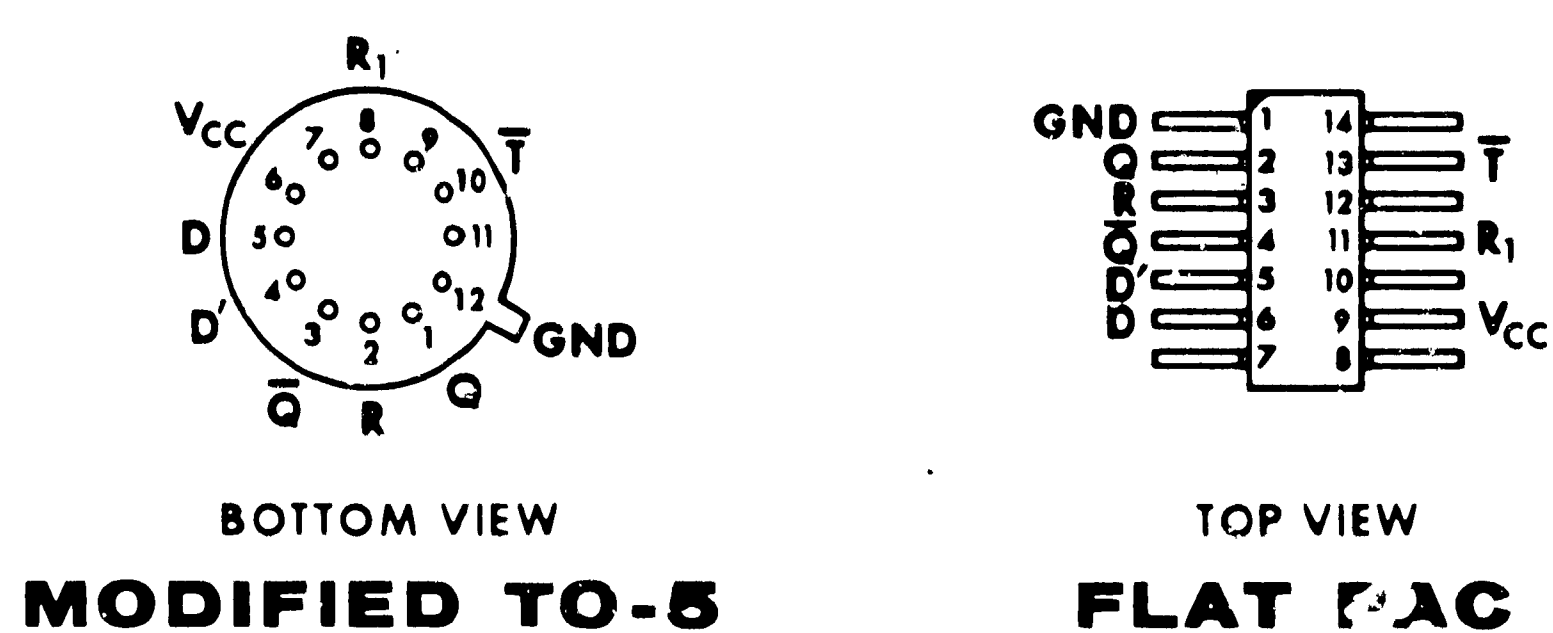
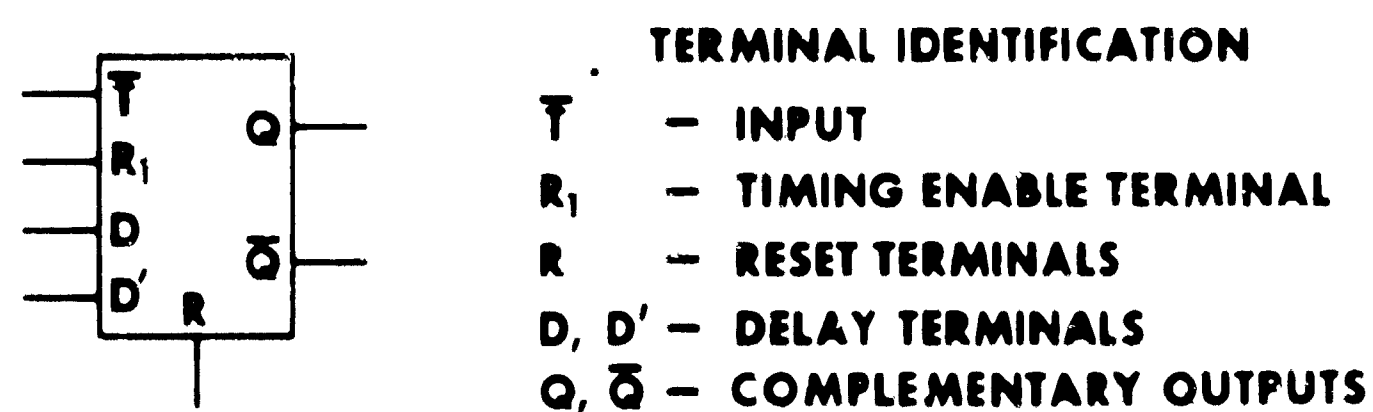


Figure 3.1.28

LOGIC DIAGRAM

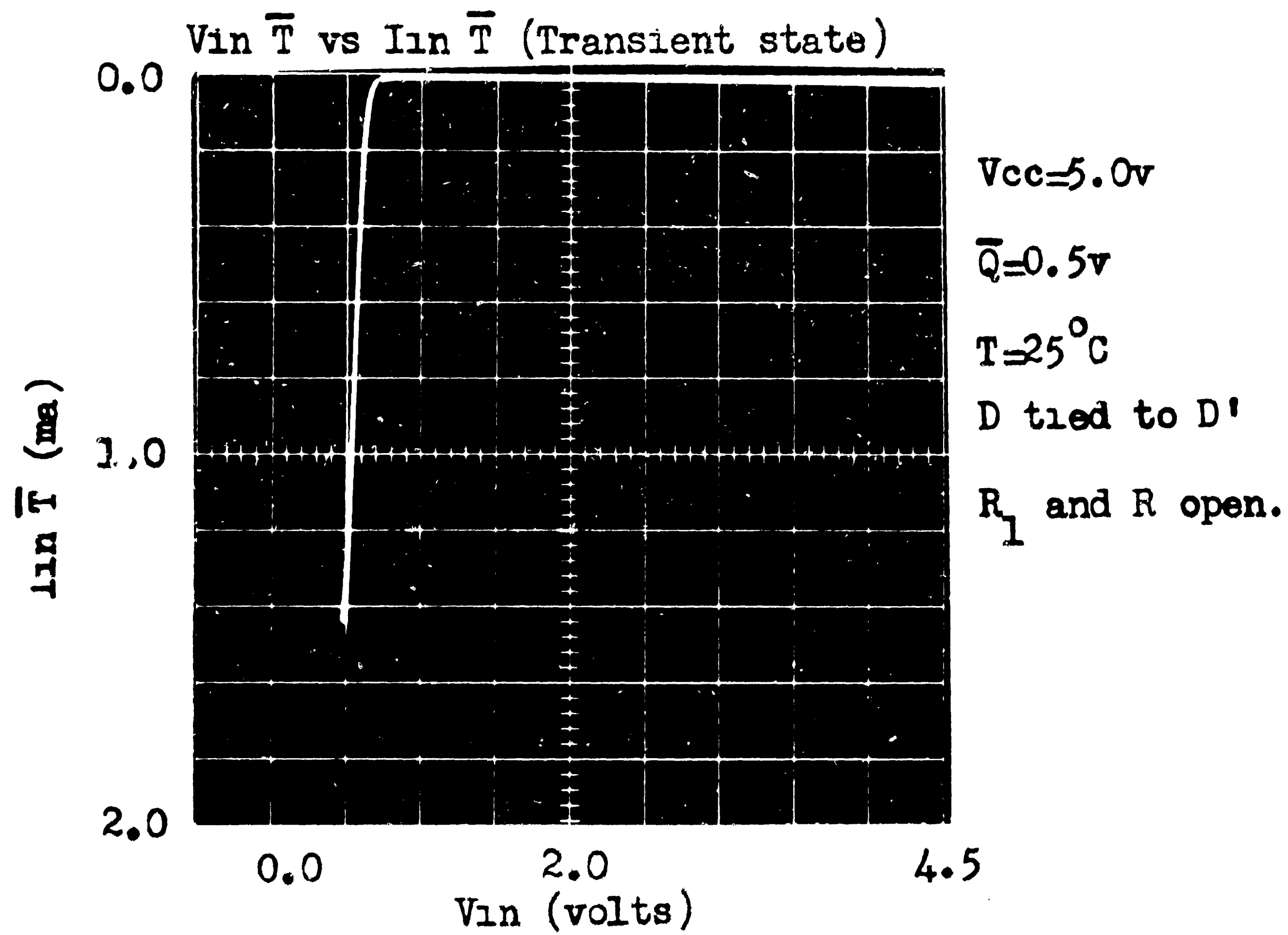
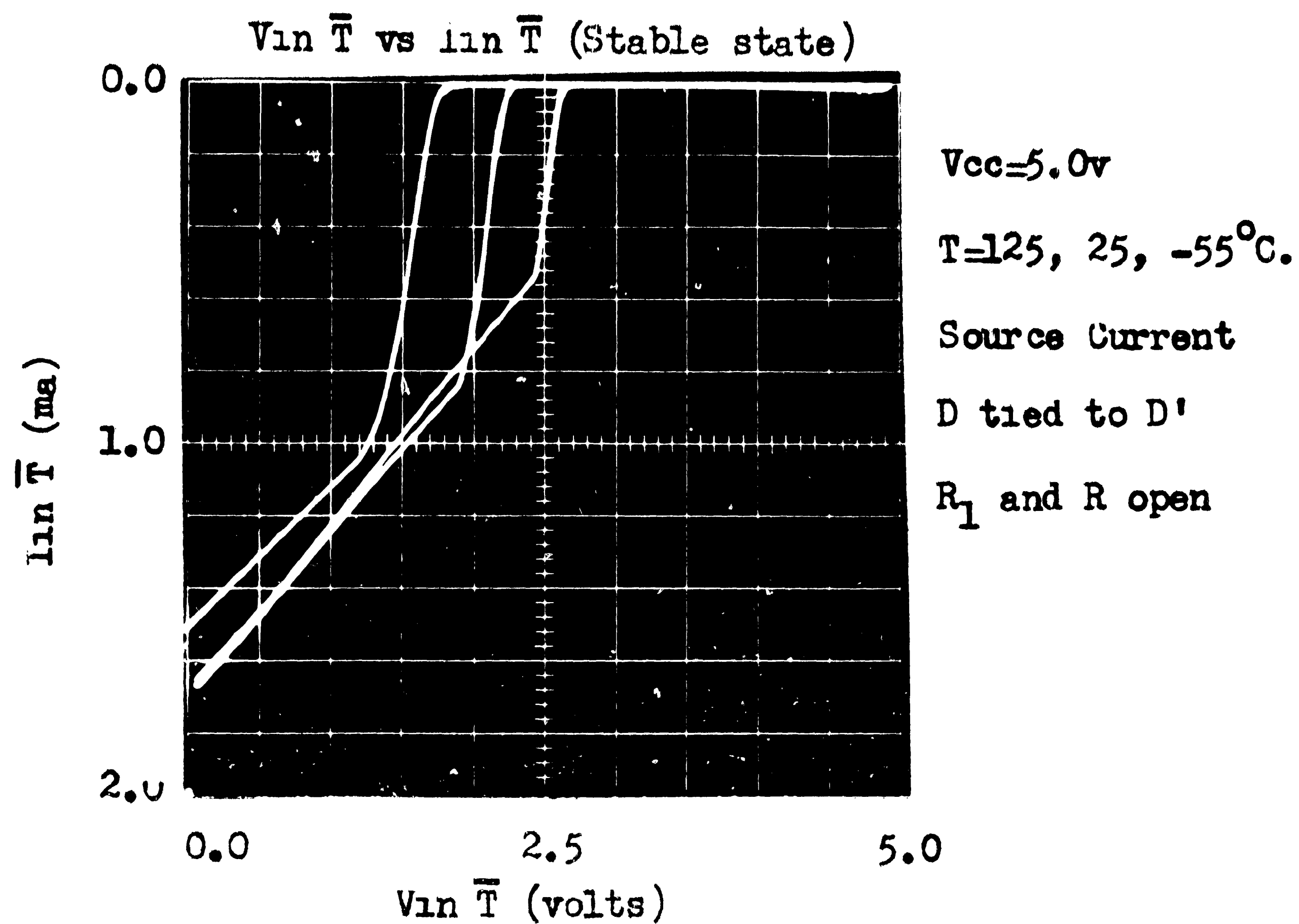


ABSOLUTE MAXIMUM RATINGS AT 25°C

Power Supply Voltage V_{cc}	6 v
Input Voltage BV_i	6 v
Output Voltage BV_o	6 v
Operating Temperature Range T_A	-55 to +125°C
Storage Temperature Range T_s	-65 to +150°C
Output Current	50 ma

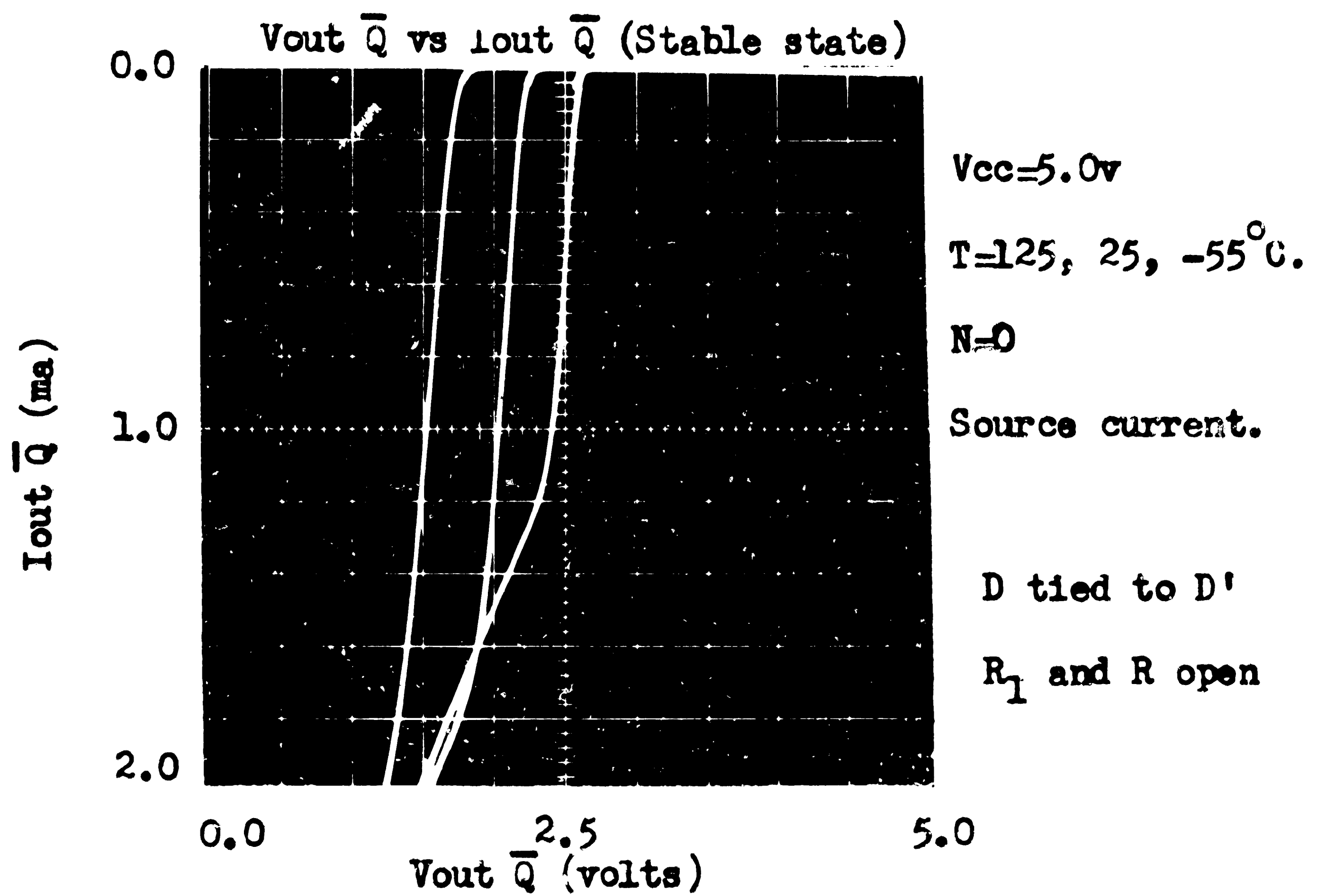
Voltage at any pin must be positive with respect to the common terminal.

A08 MONOSTABLE MULTIVIBRATOR



Note: To obtain the above curve \bar{Q} was tied to a 0.5v supply. In actual operation V_{in} would approach the voltage \bar{Q} assumes in its transient state. **Figure 3.1.29**

A08 MONOSTABLE MULTIVIBRATOR



Note: Refer to the V_{out} vs I_{out} curve for the A02 if the stable state $V_{out} \bar{Q}$ vs $I_{out} \bar{Q}$ curve for the A08 is desired. The two curves are identical.

Figure 3.1.30

A08 MONOSTABLE MULTIVIBRATOR

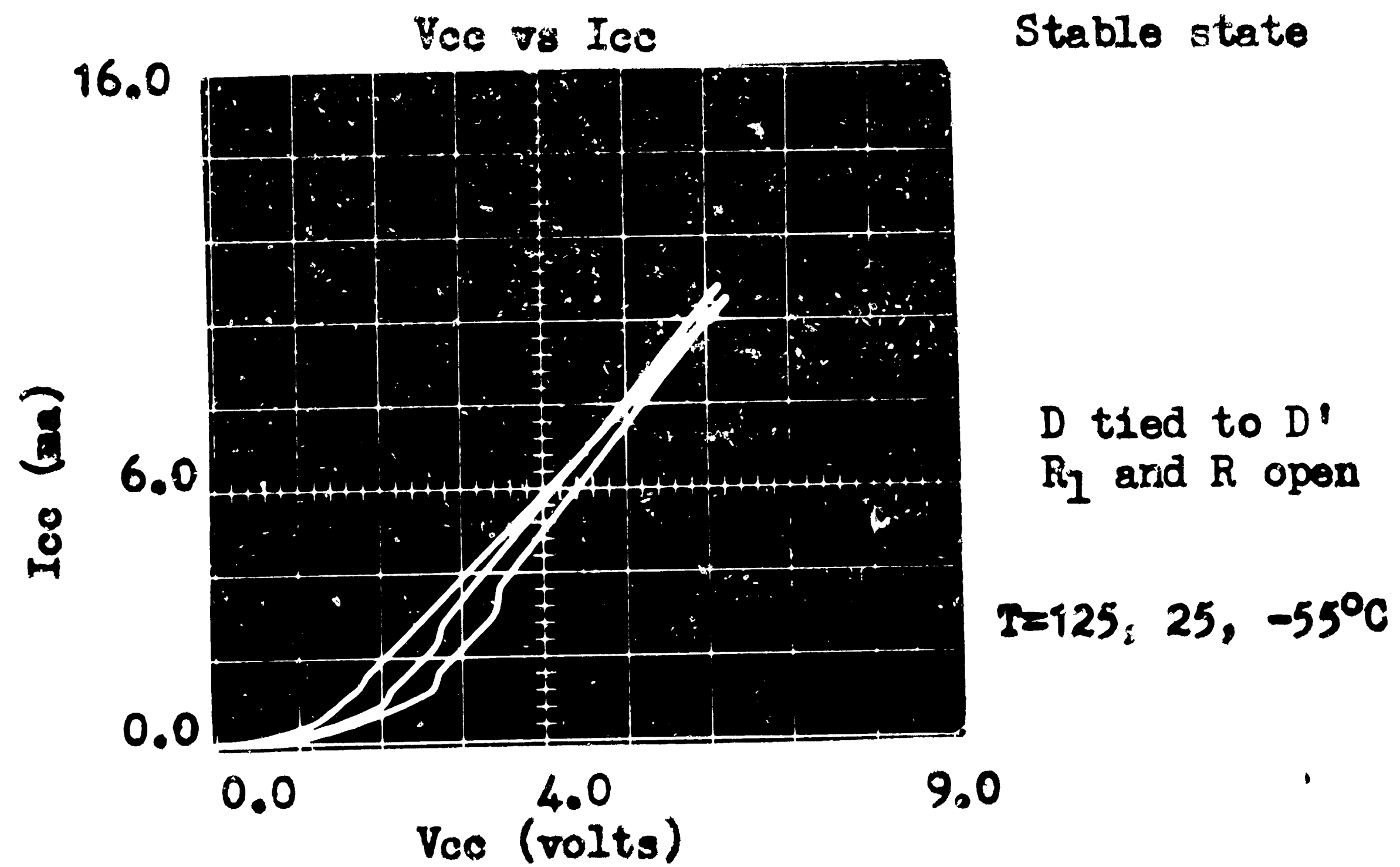
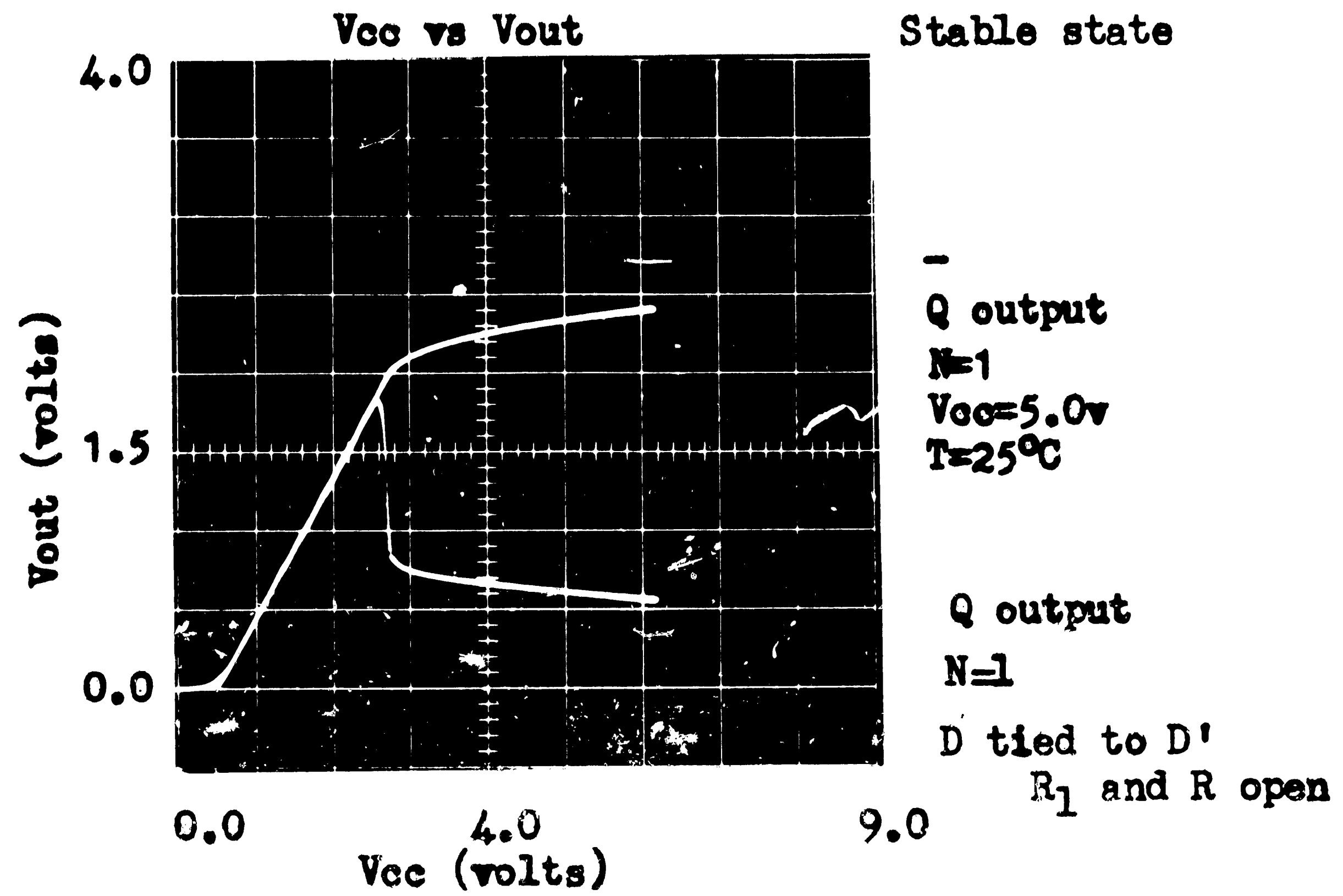
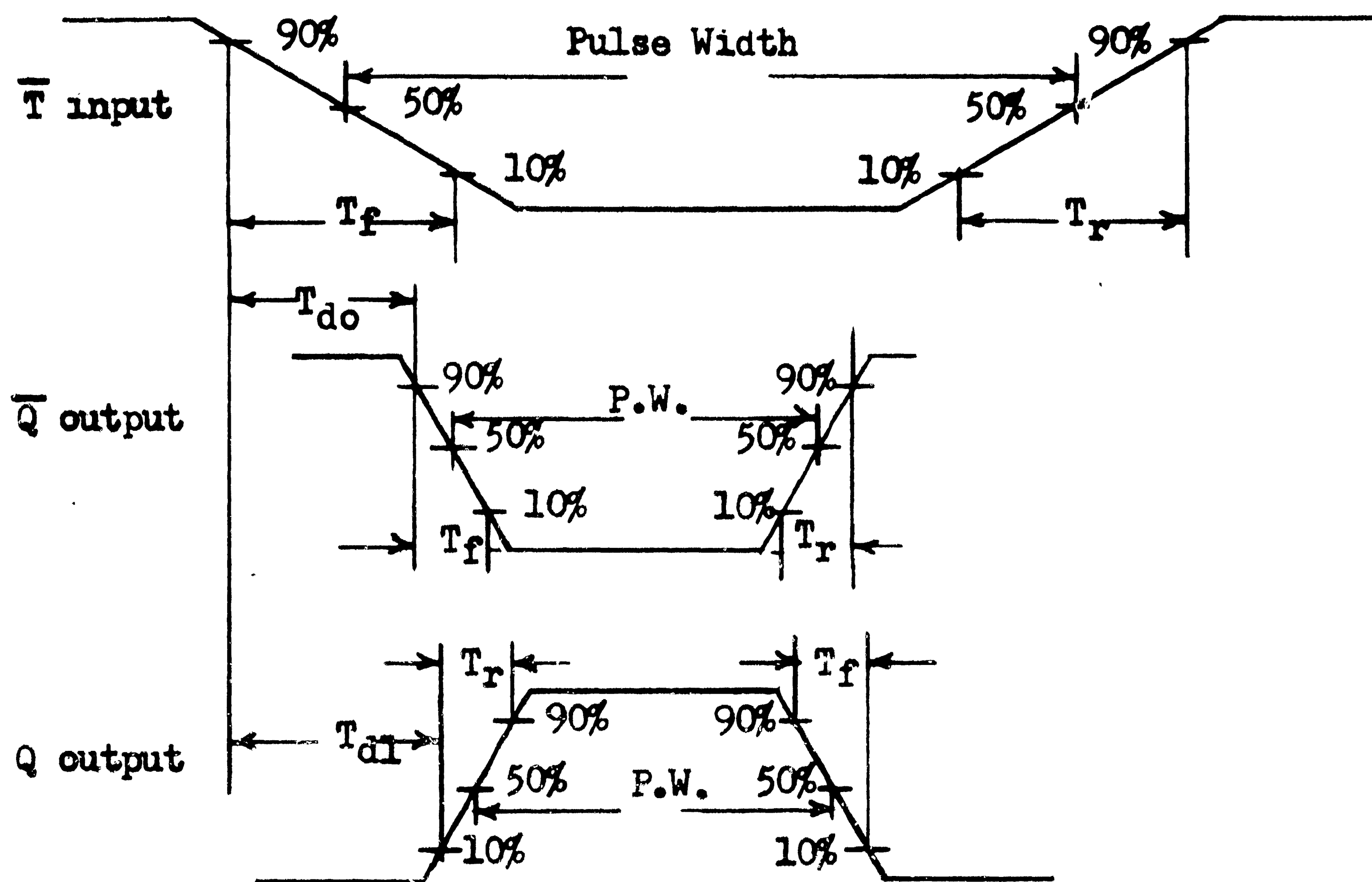


Figure 3.1.31

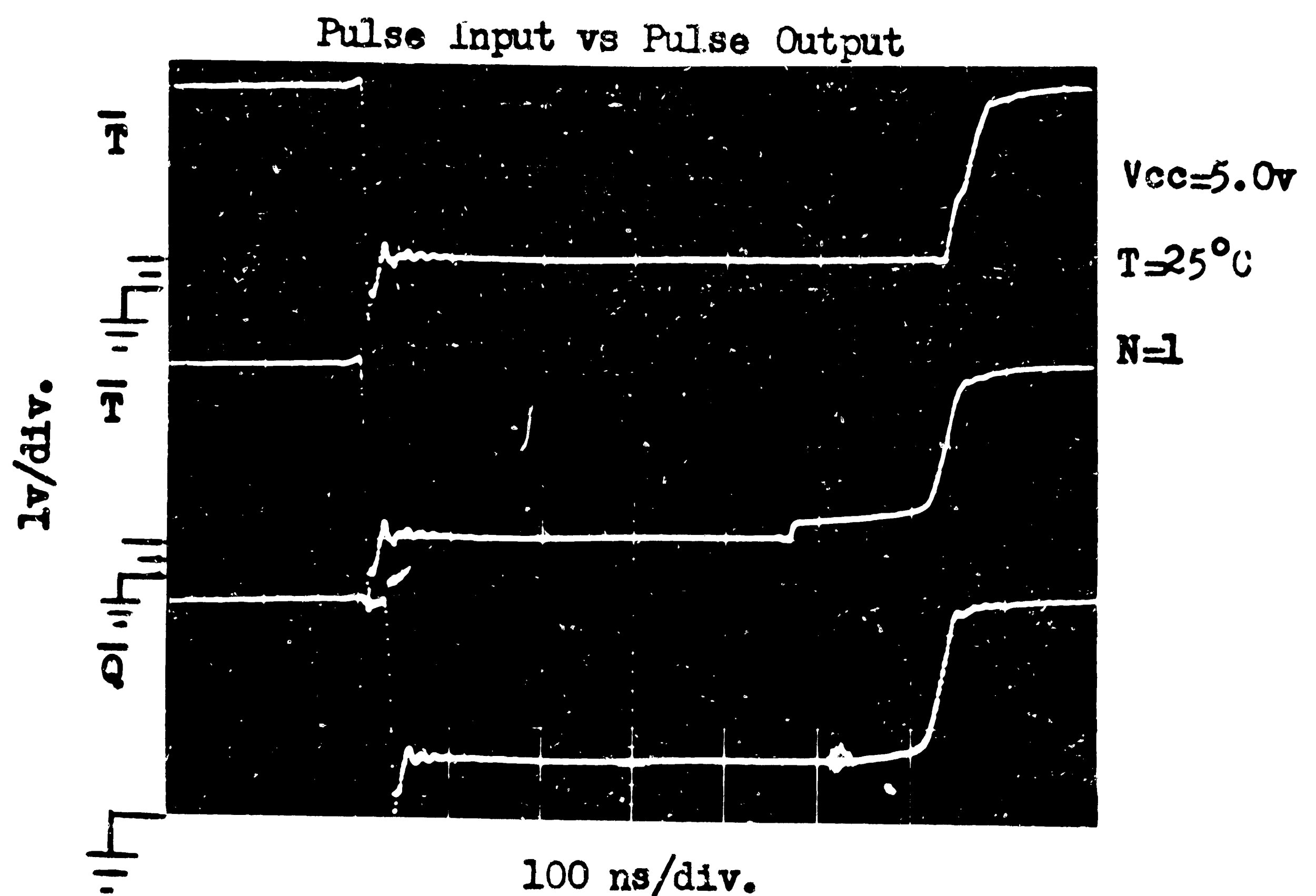
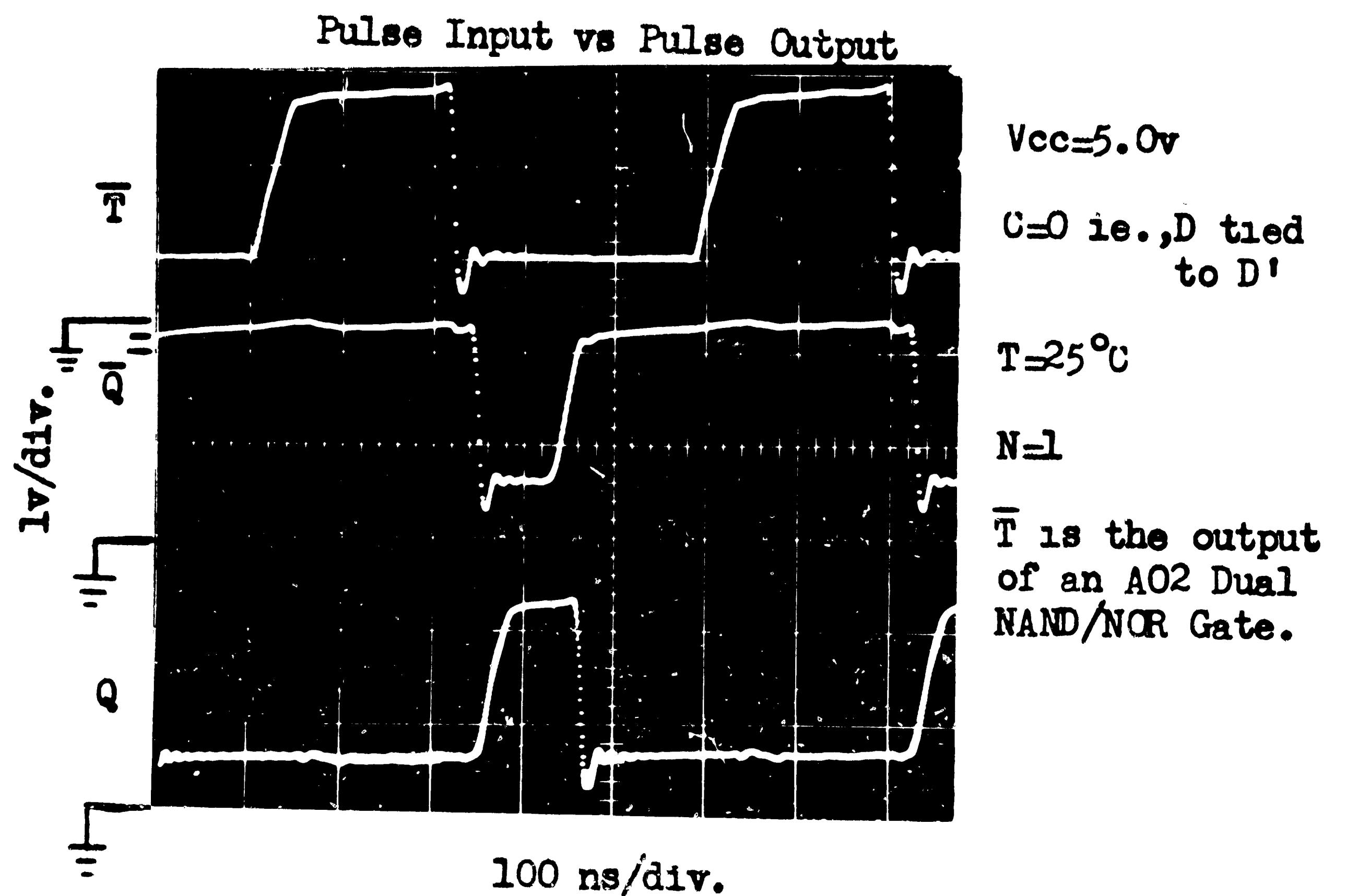


A08 One-Shot Multivibrator Waveform Definition.

Rise time (T_r), Fall time (T_f), Delay time of the \overline{Q} output, one to zero transient (T_{do}), Delay time of the Q output, zero to one transient (T_{d1}).

Figure 3.1.33

A08 MONOSTABLE MULTIVIBRATOR



The bottom oscillograph was obtained using the output of an A02 Dual NAND/NOR gate to furnish the \bar{T} input and a value of capacitance from D-D' to ground to produce the \bar{Q} output shown. The oscillograph illustrates (center trace) that the \bar{T} input will remain at a low voltage level as long as the \bar{Q} output is low ie., in its transient state. This would not occur if a pull up resistor were used on the output of the driving circuit. The top trace shows an input pulse width of sufficient duration so as not to be affected by the output.

Figure 3.1.34

Circuit Designation A08		Fan-out 1		Vcc 4.0v		Pulse Rep. Rate 1Mc													
Temperature		-55°C				-40°C				25°C									
Test Circuit:		Input \overline{T}	C=113pf		C=226pf		Input \overline{T}	C=113pf		C=226pf		Input \overline{T}	C=113pf		C=226pf				
			Q	\overline{Q}	Q	\overline{Q}		Q	\overline{Q}	Q	\overline{Q}		Q	\overline{Q}	Q	\overline{Q}			
Pulse Amplitude (Vpp)		1.9	1.7	1.8	1.7	1.8	1.9	1.7	1.7	1.7	1.8	1.7	1.6	1.6	1.6	1.6			
Pulse Width (ns)		500	212	185	350	321	500	189	171	316	296	500	141	136	231	227			
Tr (ns)		84	85	66	84	64	75	73	60	73	60	55	46	41	45	40			
Tf (ns)		9	18	21	17	19	8	14	14	14	15	6	8	9	8	9			
Td (ns)			62	52	61	53		55	47	55	45		41	34	41	34			
Min. Pulse Width, C=0			79	38				61	36				41	31					
Temperature		85°C				125°C				The input pulse width (\overline{T}) can be varied without affecting the pulse widths of the outputs. This was verified for pulse widths varying from 100 to 900 ns.									
Test Circuit:		Input \overline{T}	C=113pf		C=226pf		Input \overline{T}	C=113pf										C=226pf	
			Q	\overline{Q}	Q	\overline{Q}		Q	\overline{Q}									Q	\overline{Q}
Pulse Amplitude (Vpp)		1.7	1.5	1.4	1.5	1.5	1.6	1.4	1.4									1.4	1.4
Pulse Width (ns)		500	109	110	180	183	500	94	102									153	160
Tr (ns)		77	42	37	43	41	95	42	49									43	49
Tf (ns)		6	7	7	7	7	7	8	8									7	8
Td (ns)			41	32	41	32		43	32	43	33								
Min. Pulse Width, C=0			37	34				39	42										

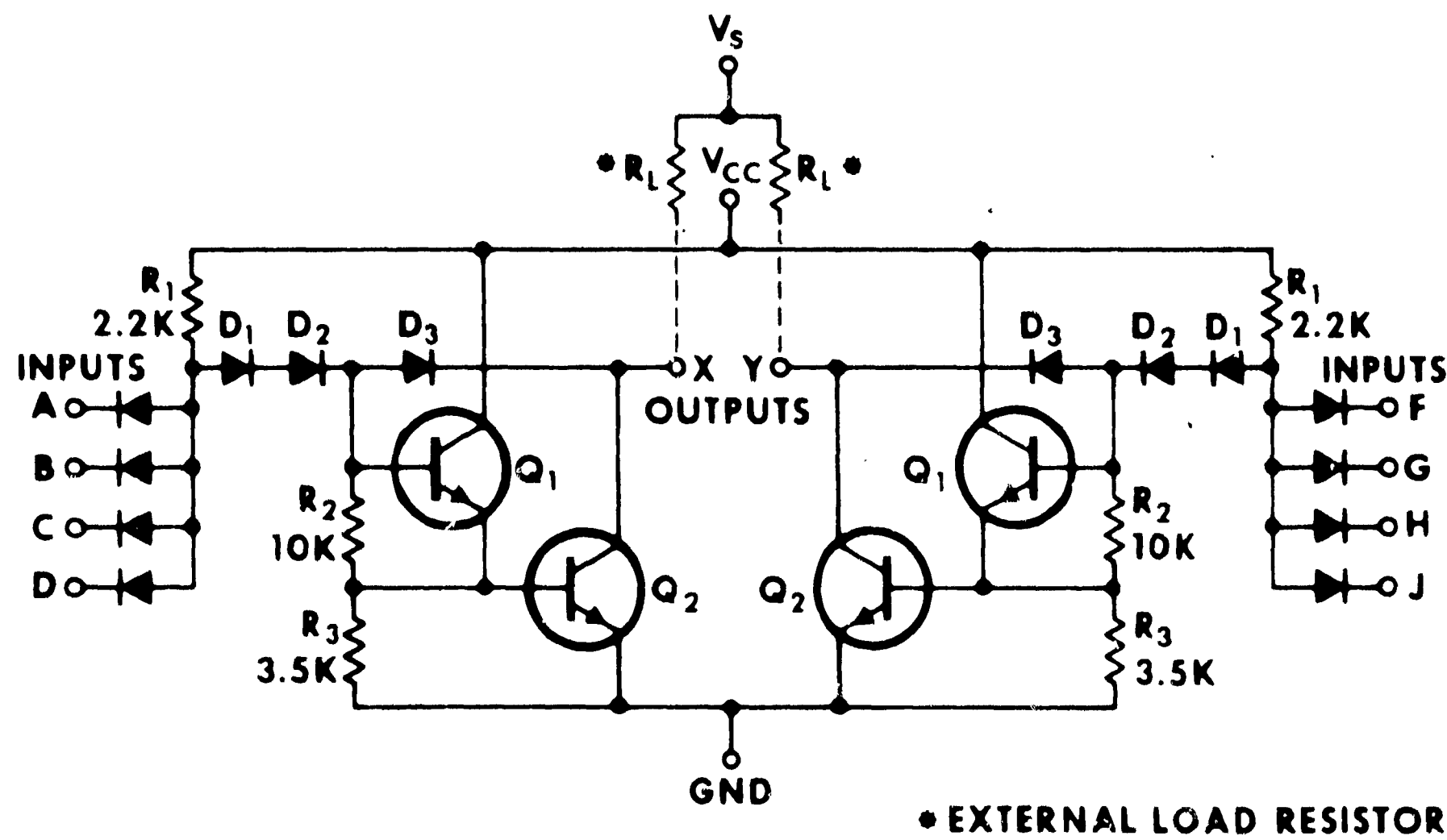
Circuit Designation A08		Fan-out 1		Vcc 5.0v		Pulse Rep. Rate 1Mc					
Temperature		-55°C				-40°C		25°C			
Test Circuit:	Input \overline{T}	C=113pf		Input \overline{T}	C=226pf		Input \overline{T}	C=113pf		C=226pf	
		Q	\overline{Q}		Q	\overline{Q}		Q	\overline{Q}	Q	\overline{Q}
Pulse Amplitude (Vpp)	2.1	1.9	1.9	1.9	1.9	1.9	1.9	1.8	1.8	1.8	1.8
Pulse Width (ns)	500	143	138	220	227	220	210	99	99	166	166
Tr (ns)	46	39	34	34	39	34	36	31	28	31	32
Tf (ns)	5	7	8	8	7	8	7	6	6	6	6
Td (ns)		36	29	29	36	29	34	32	26	33	26
Min. Pulse Width, C=0		39	29					32	29		
Temperature		85°C				125°C					
Test Circuit:	Input \overline{T}	C=113pf		Input \overline{T}	C=226pf		Input \overline{T}	C=113pf		C=226pf	
		Q	\overline{Q}		Q	\overline{Q}		Q	\overline{Q}	Q	\overline{Q}
Pulse Amplitude (Vpp)	1.8	1.6	1.6	1.6	1.6	1.6	1.5	1.5	1.5	1.5	1.5
Pulse Width (ns)	500	87	91	146	142	146	79	89	124	134	134
Tr (ns)	67	32	25	29	33	29	40	42	43	44	44
Tf (ns)	5	6	6	6	6	6	8	9	6	9	9
Td (ns)		36	28	28	36	28	43	32	44	32	
Min. Pulse Width, C=0		35	35				39	44			
				</							

Circuit Designation A08		Fan-out 1		Vcc 6.0		Pulse Rep. Rate 1MC									
Temperature		-55°C				-40°C				25°C					
Test Circuit:	Input \bar{T}	C=113pf		C=226pf		Input \bar{T}	C=113pf		C=226pf		Input \bar{T}	C=113pf		C=226pf	
		Q	\bar{Q}	Q	\bar{Q}		Q	\bar{Q}	Q	\bar{Q}		Q	\bar{Q}	Q	\bar{Q}
Pulse Amplitude (Vpp)	2.2	2.0	2.0	2.0	2.0	2.0	1.9	1.9	2.0	2.0	2.0	1.9	1.9	1.9	1.9
Pulse Width (ns)	500	103	101	178	174	500	96	96	161	160	500	84	89	139	141
Tr (ns)	32	27	23	27	23	30	27	21	26	24	47	25	21	25	24
Tf (ns)	4	6	6	6	6	3	5	5	5	5	4	5	5	5	5
Td (ns)		29	23	29	23		28	23	28	23		29	23	29	23
Min. Pulse Width, C=0		30	27				30	27				29	29		
Temperature		85°C				125°C				The input pulse width (\bar{T}) can be varied without affecting the pulse widths of the outputs. This was verified for input pulse widths ranging from 100 to 900 ns.					
Test Circuit:	Input \bar{T}	C=113pf		C=226pf		Input \bar{T}	C=113pf		C=226pf		Input \bar{T}	C=113pf		C=226pf	
		Q	\bar{Q}	Q	\bar{Q}		Q	\bar{Q}	Q	\bar{Q}		Q	\bar{Q}		
Pulse Amplitude (Vpp)	1.9	1.7	1.8	1.7	1.8	1.8	1.5	1.6	1.6	1.6	1.6	1.5	1.6	1.6	1.6
Pulse Width (ns)	500	75	82	120	126	500	70	78	105	117	500	78	105	117	117
Tr (ns)	59	32	25	32	26	99	39	42	47	42	99	42	47	42	42
Tf (ns)	5	6	8	5	7	7	9	10	6	10	7	9	10	6	10
Td (ns)		37	29	38	30		51	41	52	41		51	41	52	41
Min. Pulse Width, C=0		36	38				41	47				41	47		

1. A20 Dual NAND/NOR Gate Equivalent Circuit

2. Siliconix Test Circuits and Waveform Definitions

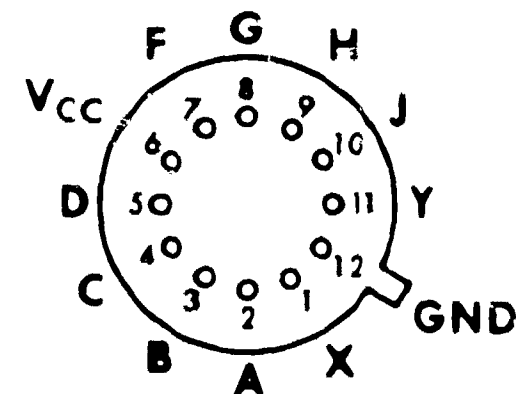
CIRCUIT DIAGRAM



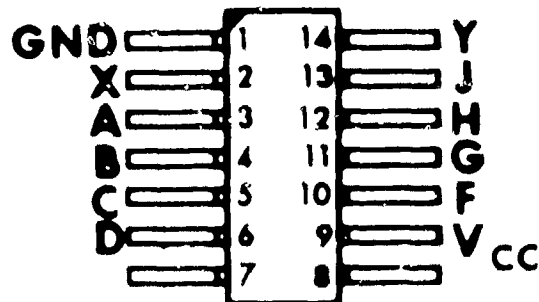
A20 Dual NAND/NOR Gate
UNIFET Commutator Driver and Buffer

PIN DIAGRAMS

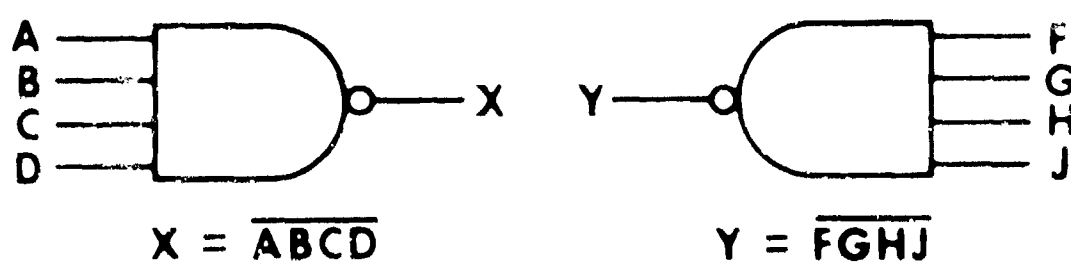
Figure 3.1.35 LOGIC DIAGRAMS



Modified TO-5



FlatPac



ABSOLUTE MAXIMUM RATINGS AT 25°C

External Source Voltage V_S	18 v
Circuit Power Supply Voltage V_{CC}	6 v
Input Voltage BV_i	6 v
Output Voltage BV_{CEX} at 1 μa	18 v
Sustaining Output Voltage LV_{CEX} at 1 ma	18 v
Operating Temperature Range T_A	-55 to +125°C
Storage Temperature Range T_S	-65 to +150°C
Output Current	35 ma

Voltage at any pin must be positive with respect to the common terminal.

This circuit was not tested because of its similarity with the A02 Dual NAND/NOR Gate.

NOTES #9.3.2

EVALUATION OF GENERAL MICRO-ELECTRONICS FUNCTIONAL DEVICES

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CIRCUITS WHICH COMPRISE GENERAL MICROELECTRONICS LINE

Low-Power RTL

1. G, 4 input OR/NOR Gate
2. D₂, Dual 2 input NOR Gate
3. D₃, Dual 3 input NOR Gate
4. E, Dual 2 input Expander Gate
5. B, 2 input Buffer Element
6. H, Exclusive or Element, Half Adder
7. A, Adder Element
8. R, Register Element

High-Power RTL

1. Dual 3 input NOR Gate

CML

1. 543G5 5 input OR/NOR Gate

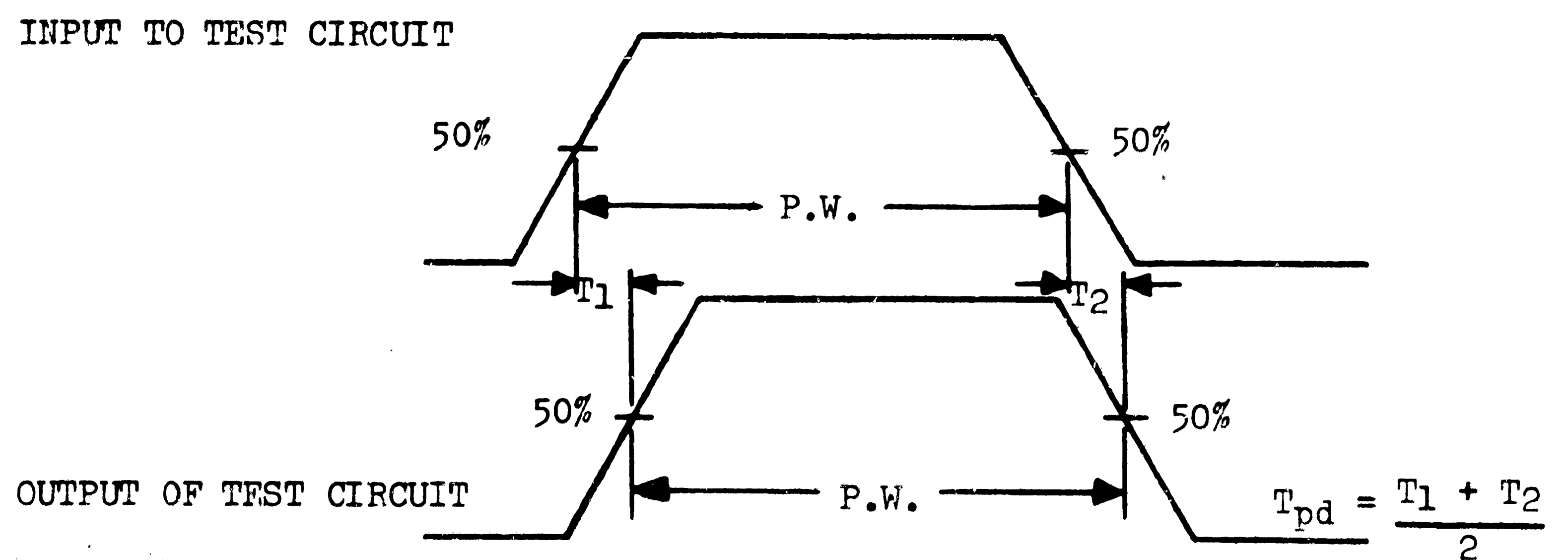
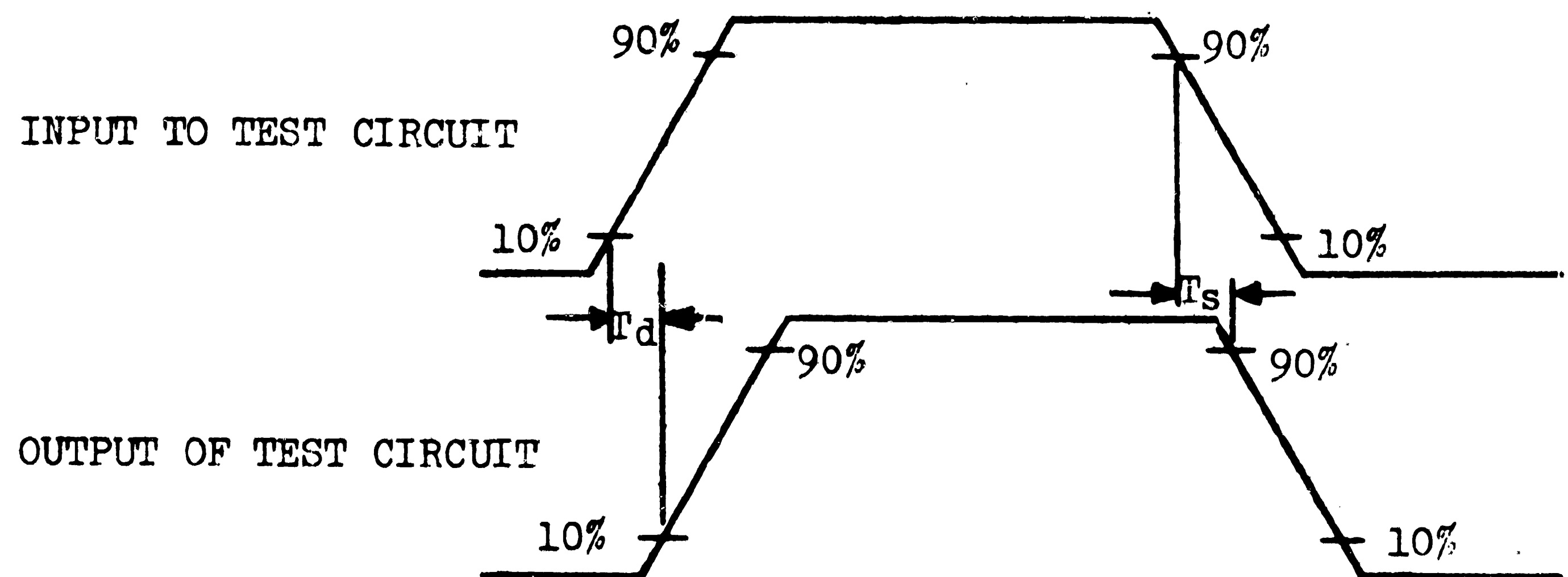
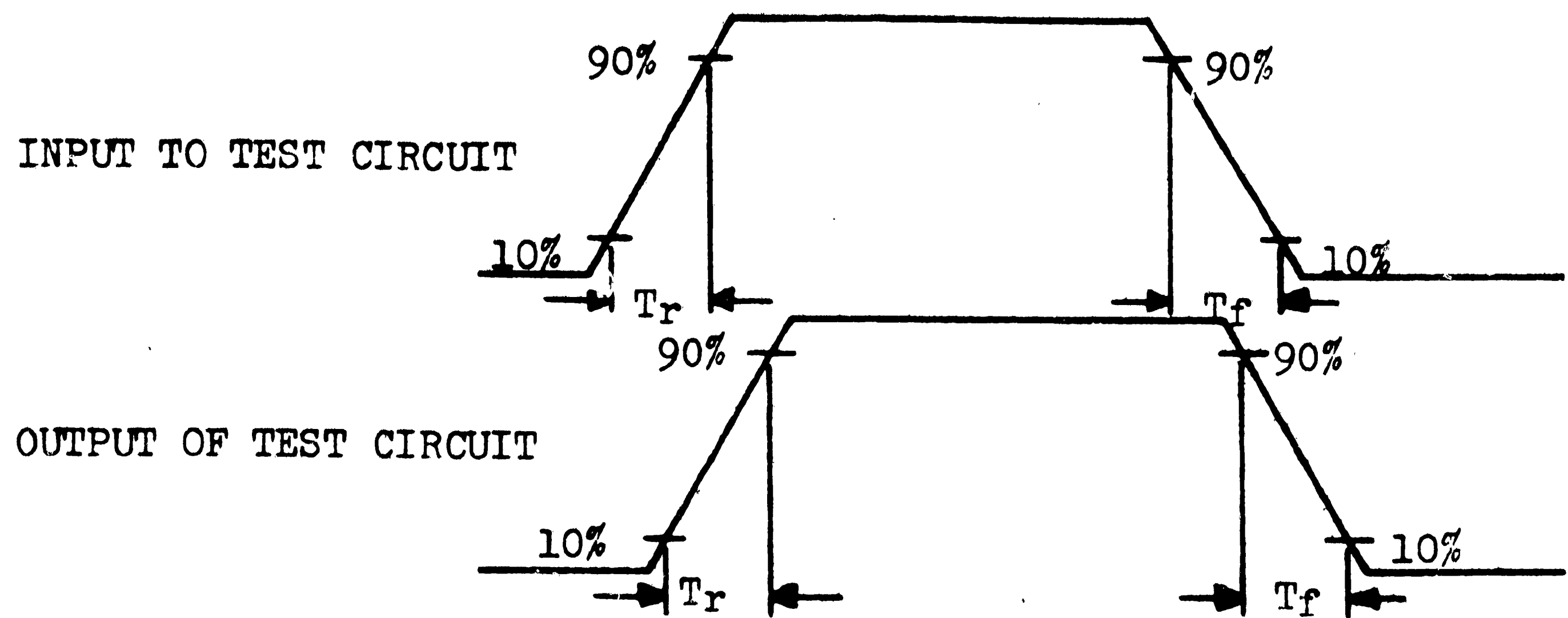
TTL

1. 365D4 Dual 4 input Gate
2. 365G8 8 input Gate

DTL

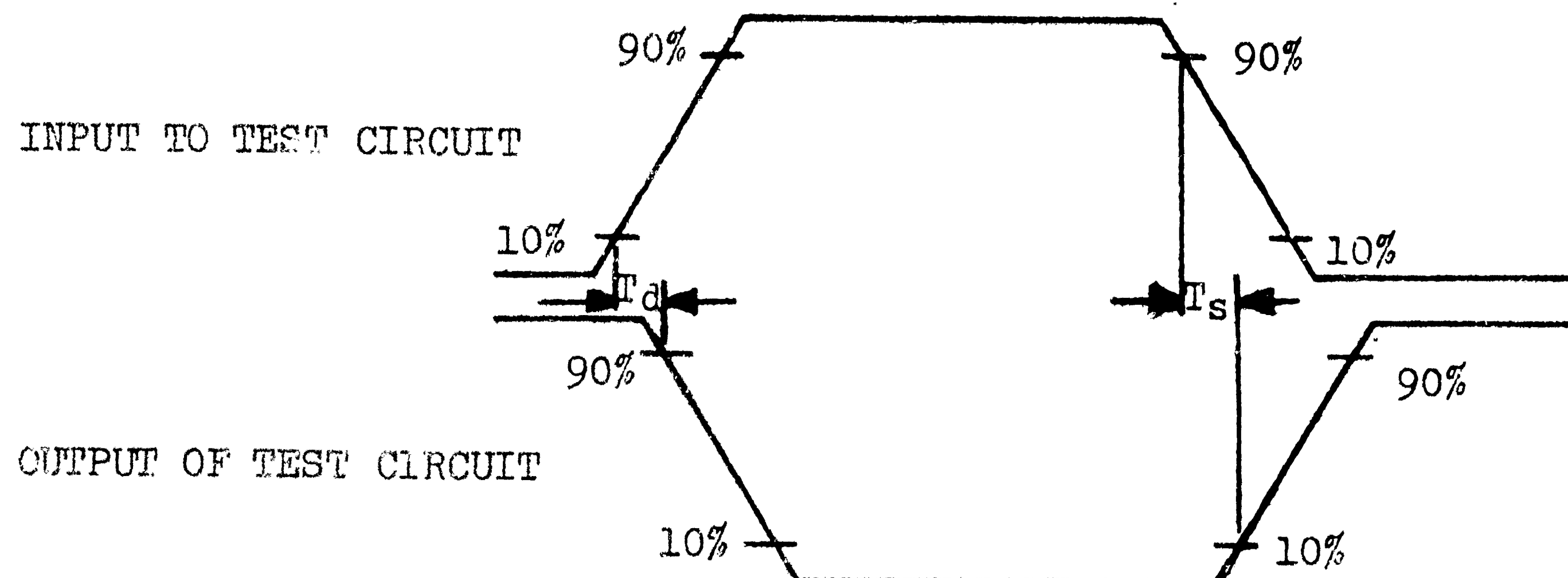
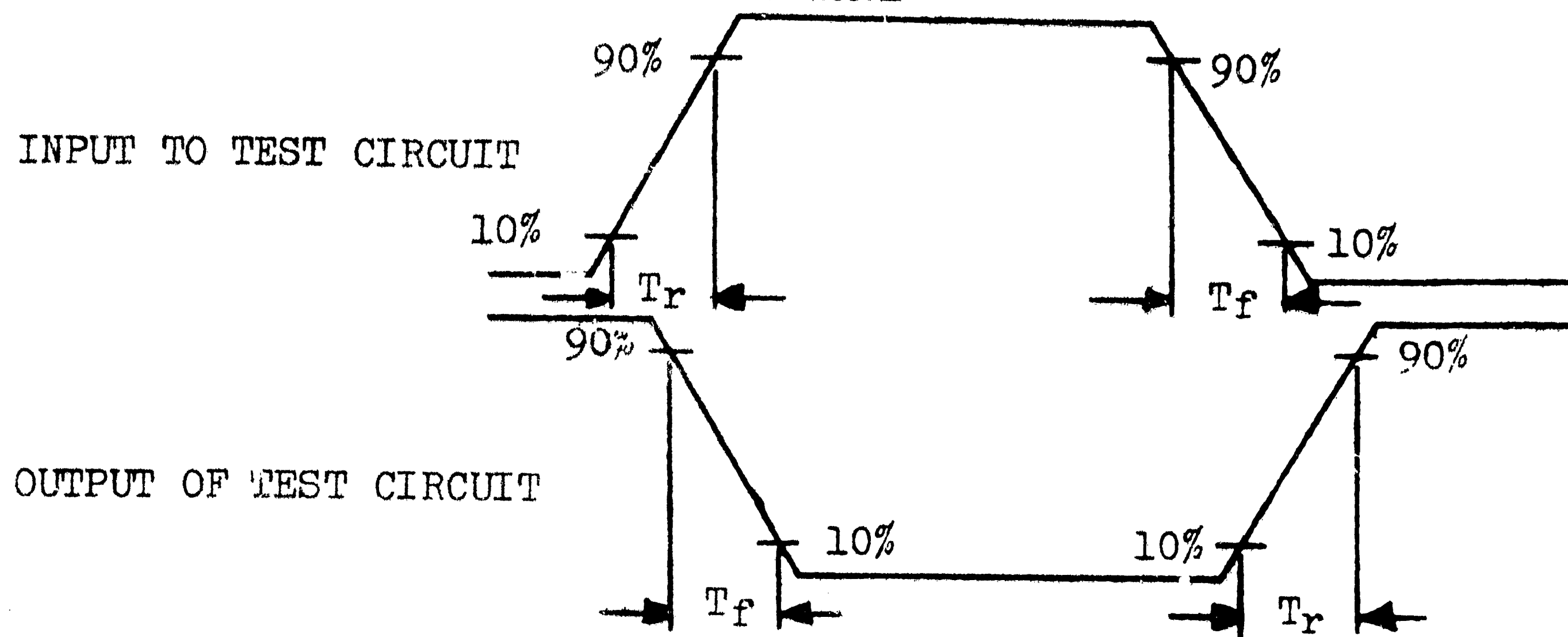
1. 254G4 4 input NOR Gate
2. 254G3 3 input NOR Gate
3. 254G6 6 input Diode and Gate
4. 254P 3 input Power Gate
5. 264D₂ Dual 2 input Gate
6. 264B Binary Element
7. 254D₃ Dual 3 input Diode and Gate

WAVEFORM DESCRIPTION AND TIME MEASUREMENT DEFINITION FOR A POSITIVE INPUT WAVE AND A POSITIVE OUTPUT WAVE

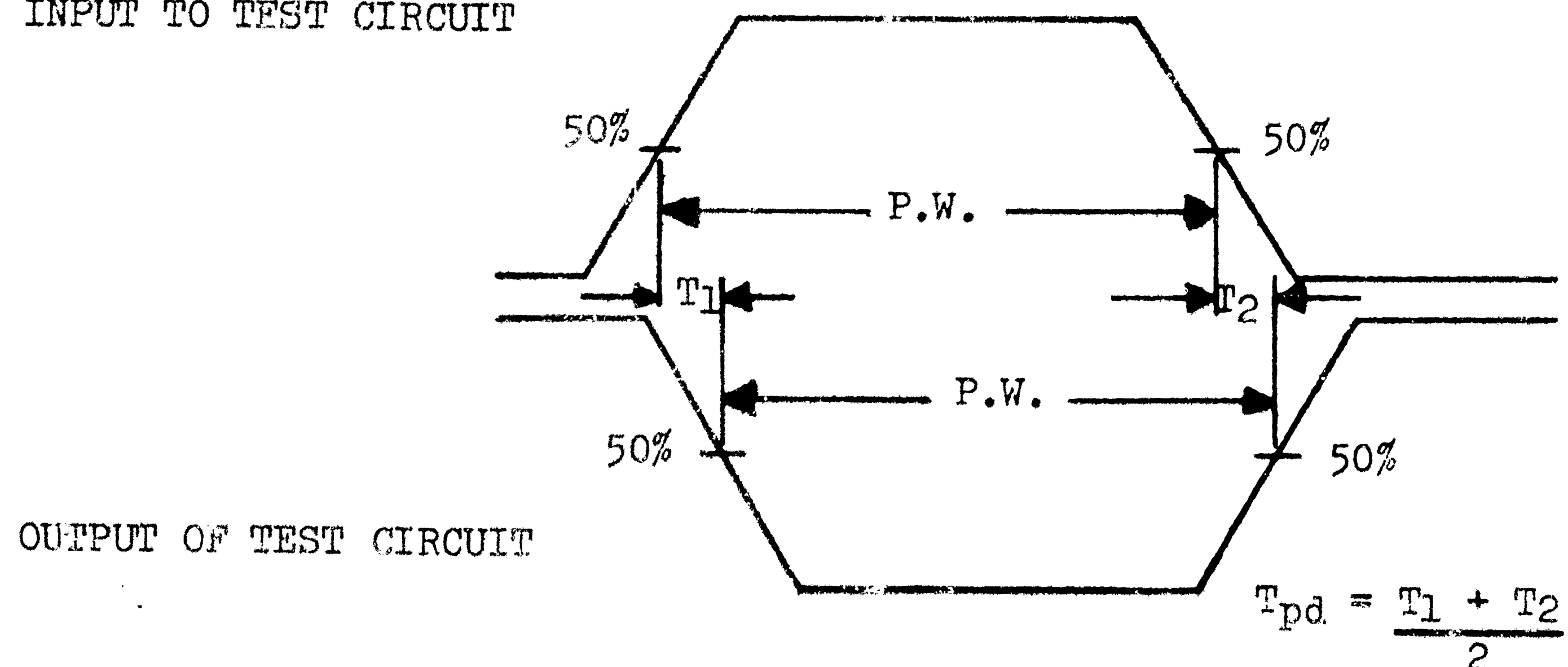


GENERAL MICROELECTRONICS

WAVEFORM DESCRIPTION AND TIME MEASUREMENT DEFINITION FOR A POSITIVE INPUT WAVE AND A NEGATIVE OUTPUT WAVE



INPUT TO TEST CIRCUIT



EQUIPMENT LIST FOR EVALUATION OF GENERAL MICROELECTRONIC

1. Oscilloscope:

Tektronix, Model 567 with: 3S76 Sampling dual trace
3T77 Sampling Sweep
6R1 Digital plug-in units
P6032 Probes

2. Pulse Generators:

Texas Instruments, Model 6611
Texas Instruments, Model 6303

3. Power Supplies:

Trygon Model HR40-750
Harrison Laboratories, Model 802B
Harrison Laboratories, Model 6204A

4. Transistor Curve Tracer:

Tektronix, Model 575

5. Voltmeter:

Hewlett Packard, Model 412A

6. Temperature Chamber:

Stratham, Model SD-6

EVALUATION

The General Microelectronic RTL line is a series of monolithic, planar, epitaxial devices which are packaged in a flat pack or TO-5 can. The family consists of the following elements:

G, D ₂ , D ₃	Basic NAND Gates
153D ₃	A basic higher power NAND Gate
E	Contains 2 sets of 2 input transistors used to extend the fan-in of the basic gates
B	Primarily a driver circuit to extend the fan-out capabilities of the basic gates
A	Provides the sum and carry outputs for two inputs to be added
H	Generates an exclusive OR function
R	Functions as a shift register or delay flip-flop

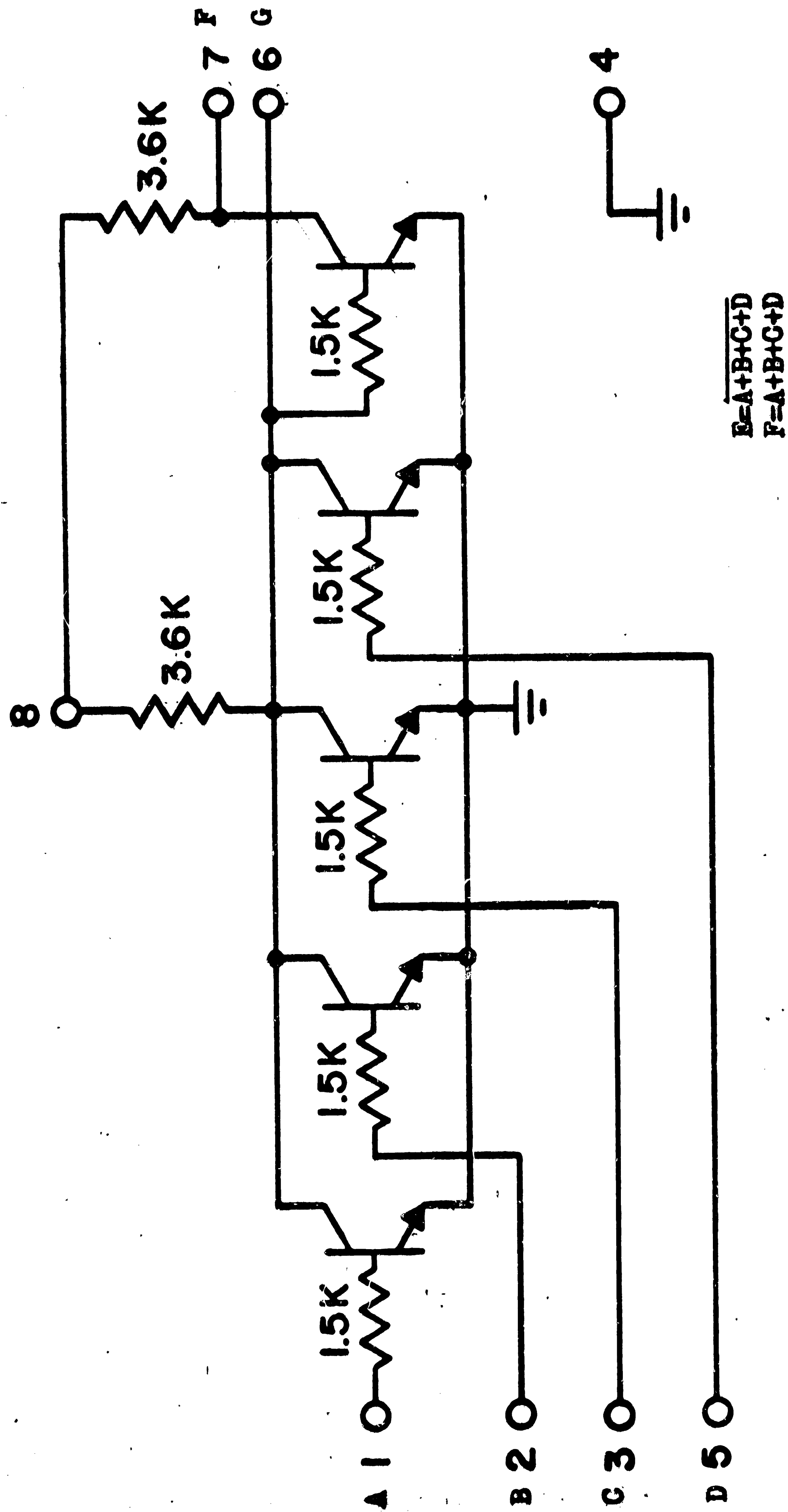
The circuits were tested on a transistor curve tracer to obtain demonstrative circuit static characteristics. The only circuit not tested statically was the R element due to the nature of the time spacing requirements between the clock and the data inputs.

The same circuits used to obtain the static curves were tested dynamically and only representative circuits were tested. The G element, for instance, gives a good indication of the performance of the D₂, D₃, and 153D₃. The Buffer Element was tested because of the additional circuitry to obtain the high output drive. The A element should give a performance profile of the H element also. The R element was tested dynamically because of its unique circuit function.

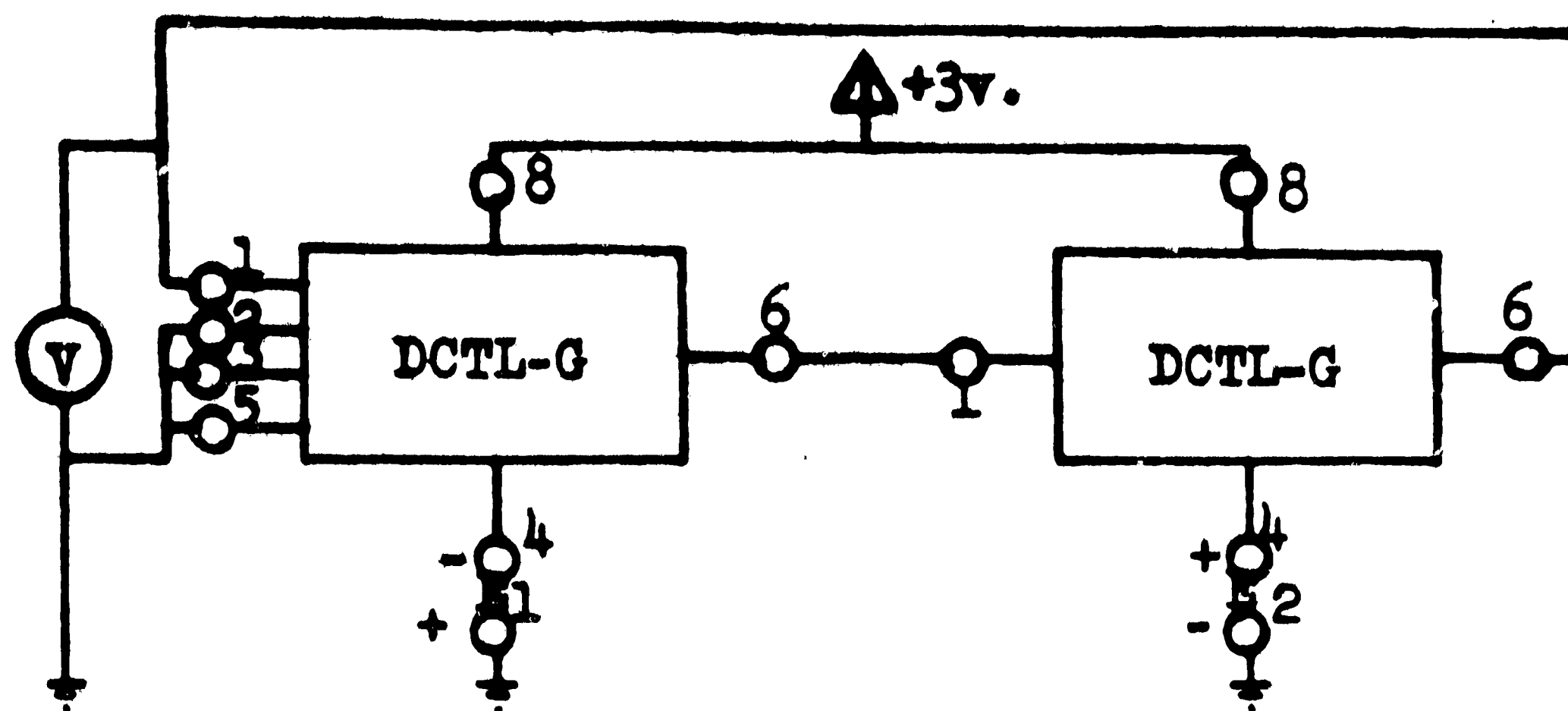
DYNAMIC TEST PROCEDURE:

1. The block diagram for each circuit is given preceeding the data for that circuit.
2. The load supply was held constant at the manufacturers rated for all tests.
3. The temperature was regulated at 25°C.
4. The test circuit supply was set at 2.0 volts, the frequency at 1MC and the pulse width to the test circuit at 500 ns and load of 1.
5. The supply was increased to 3.0 with all else constant. Data and a picture were taken.

6. The Supply was increased to 4.0 volts and full data was again taken.
7. The above procedure from 2 to 6 was repeated at -40°C , -55°C , $+85^{\circ}\text{C}$, $+125^{\circ}\text{C}$.
8. The procedure from 2 to 7 was repeated for loads of 3 and 5.
9. In the case of the buffer the load values were 2, 6 and 10.
10. The test procedure for the R element is included with the data.



4 - INPUT DCTL GATE ELEMENT, G



NOISE TEST

Procedure:

1. The circuits were connected as in the above block diagram.
2. E_2 was replaced by a short.
3. E_1 was increased until V indicated a change of state.
4. The system was reset by disconnecting the negative terminal of E_1 which set V to zero.
5. E_1 was replaced by a short.
6. E_2 was increased until V indicated a change of state.
7. The system was reset by disconnecting E_1 's short which set V to zero.

Data:

The average of five test runs was:

E_1 at system change of state -0.596

E_2 at system change of state +0.603

The noise margin of the DCTL elements used was 0.596v.

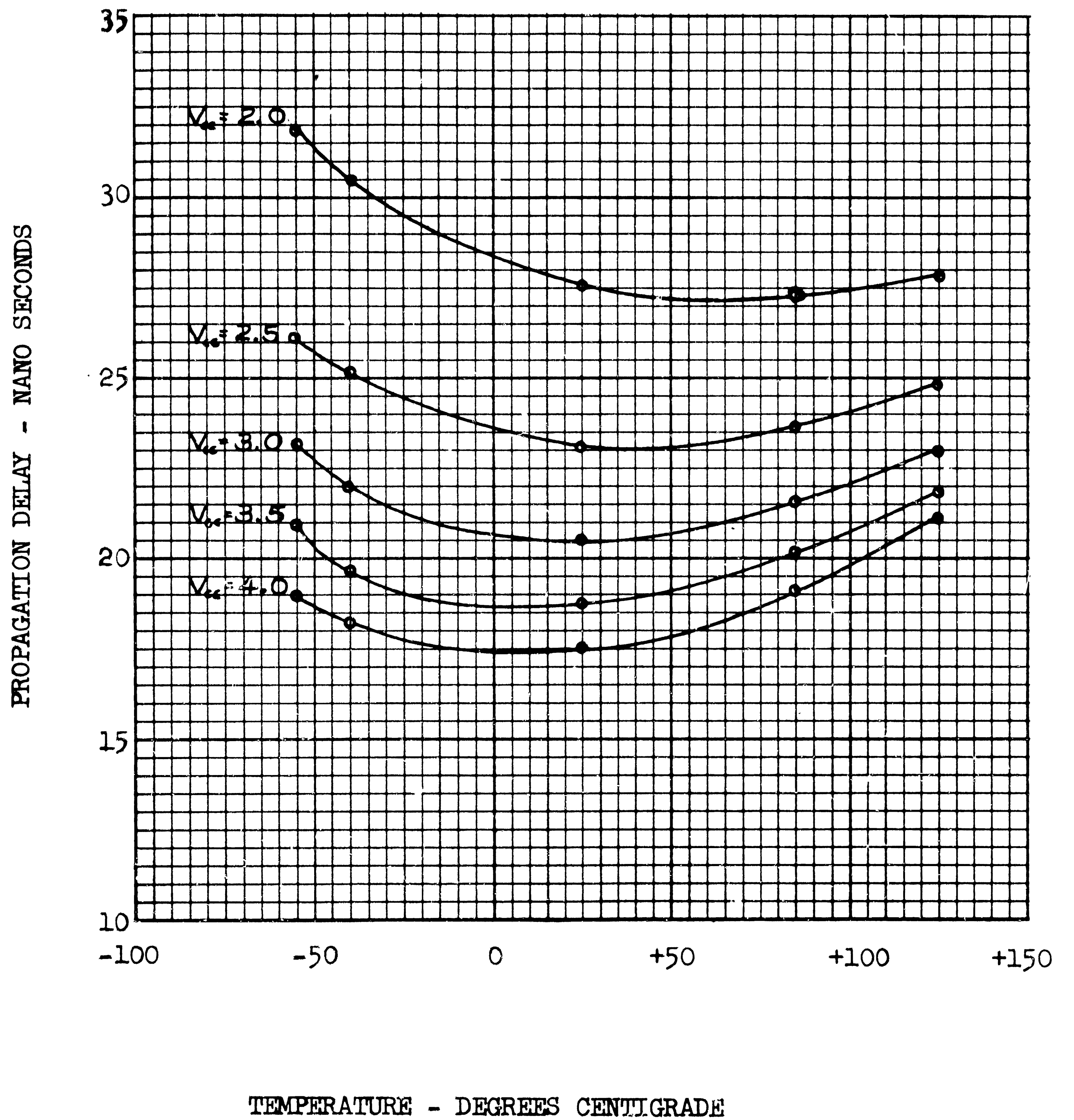
Equipment:

Voltmeter; Hewlett Packard, Model 412A
 Power supply; Trygon Electronics, Model HR40-750
 E_1 and E_2 ; Harrison Laboratories, Model 6204A

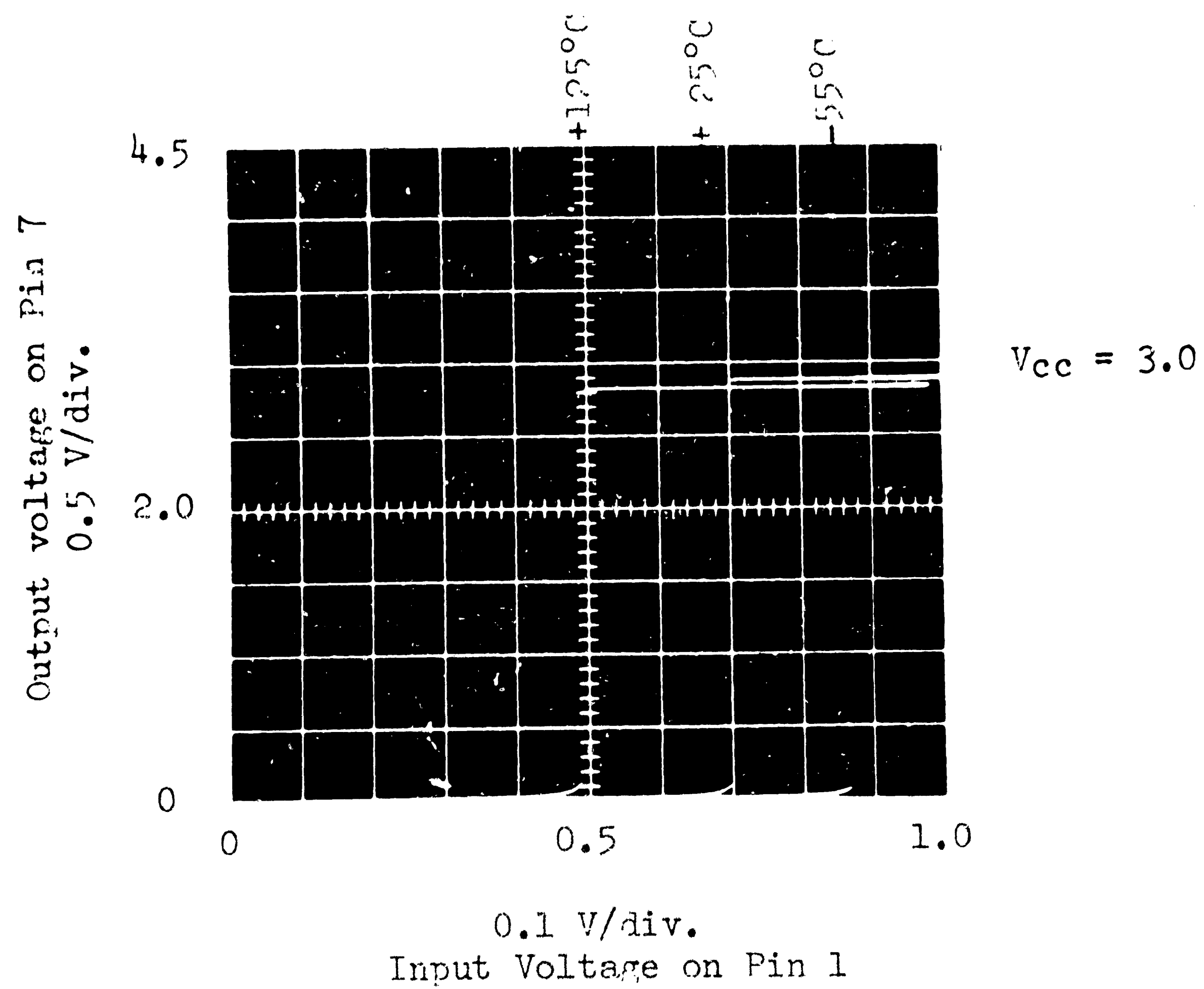
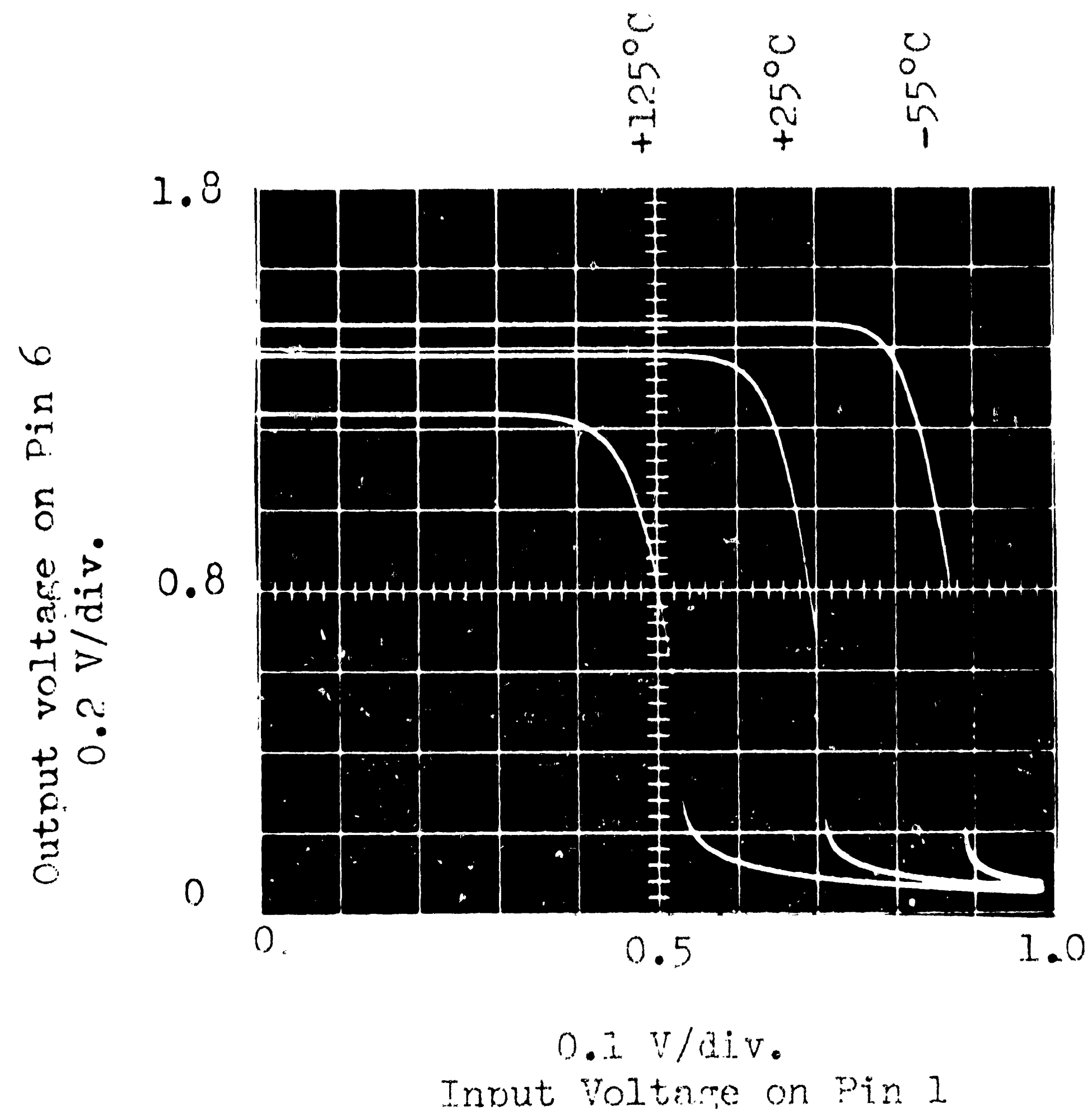
TEMP.-°C	V _{cc} -VOLTS	PERIOD-NS	AMPL.-VOLTS	T _{pd} -NS
-55	2.0	446	0.94	31.8
	2.5	365	1.02	26.1
	3.0	323	1.11	23.1
	3.5	291	1.20	20.8
	4.0	264	1.30	18.9
-40	2.0	427	0.91	30.5
	2.5	353	1.00	25.2
	3.0	308	1.08	22.0
	3.5	275	1.19	19.6
	4.0	253	1.28	18.1
+25	2.0	387	0.80	27.6
	2.5	325	0.90	23.2
	3.0	287	1.00	20.5
	3.5	262	1.10	18.7
	4.0	245	1.20	17.5
+85	2.0	383	0.70	27.3
	2.5	332	0.78	23.7
	3.0	302	0.84	21.6
	3.5	282	0.92	20.2
	4.0	269	1.00	19.2
+125	2.0	389	0.64	27.8
	2.5	347	0.74	24.8
	3.0	322	0.84	23.0
	3.5	306	0.93	21.8
	4.0	297	1.02	21.2

TABLE FOR PROPAGATION DELAY VERSUS TEMPERATURE CURVES
DCTL - G ELEMENT

PROPAGATION DELAY versus TEMPERATURE

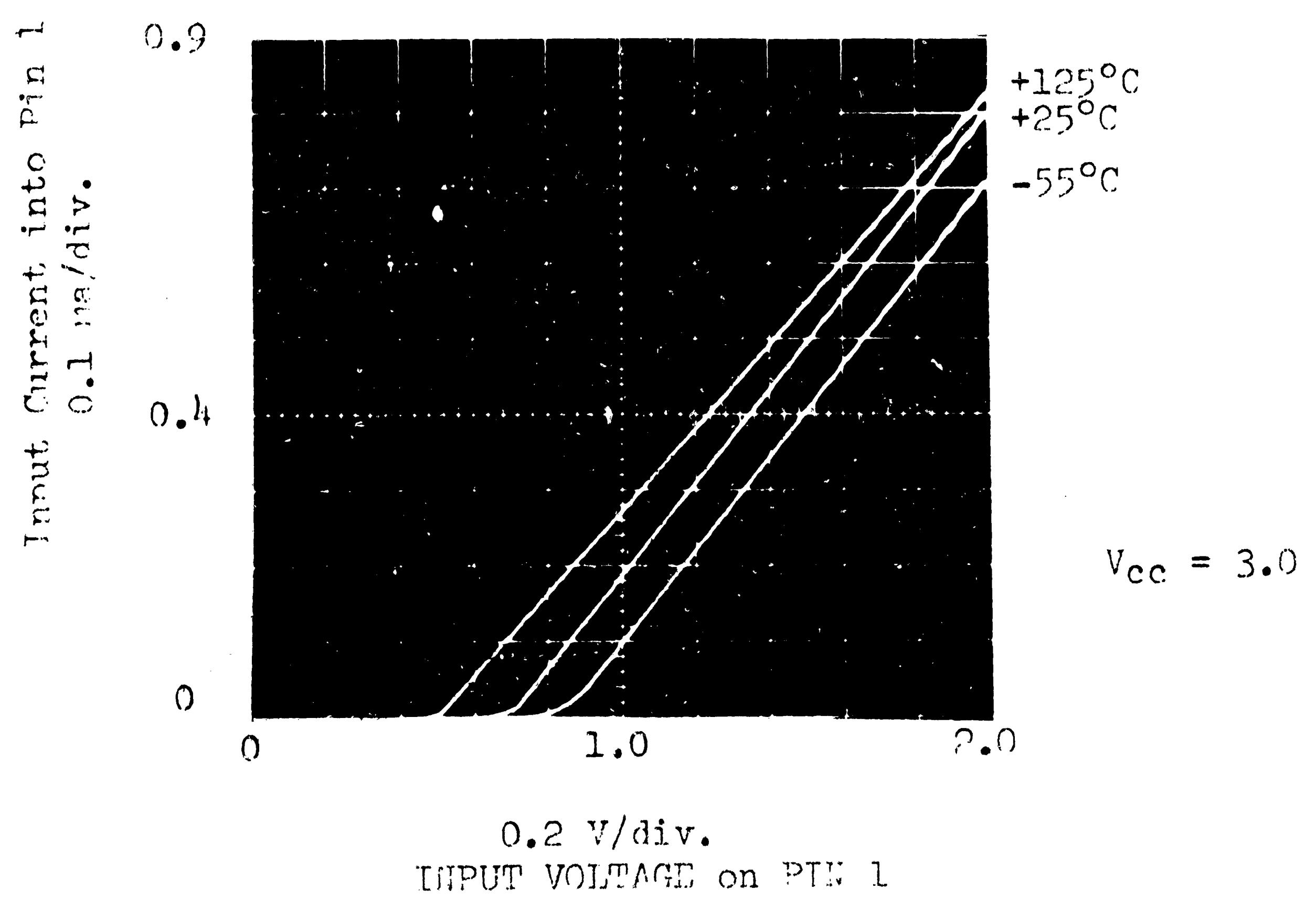


TEST CONDITIONS: Seven Low Power RTL G elements connected in a ring oscillator with a variable common supply voltage.

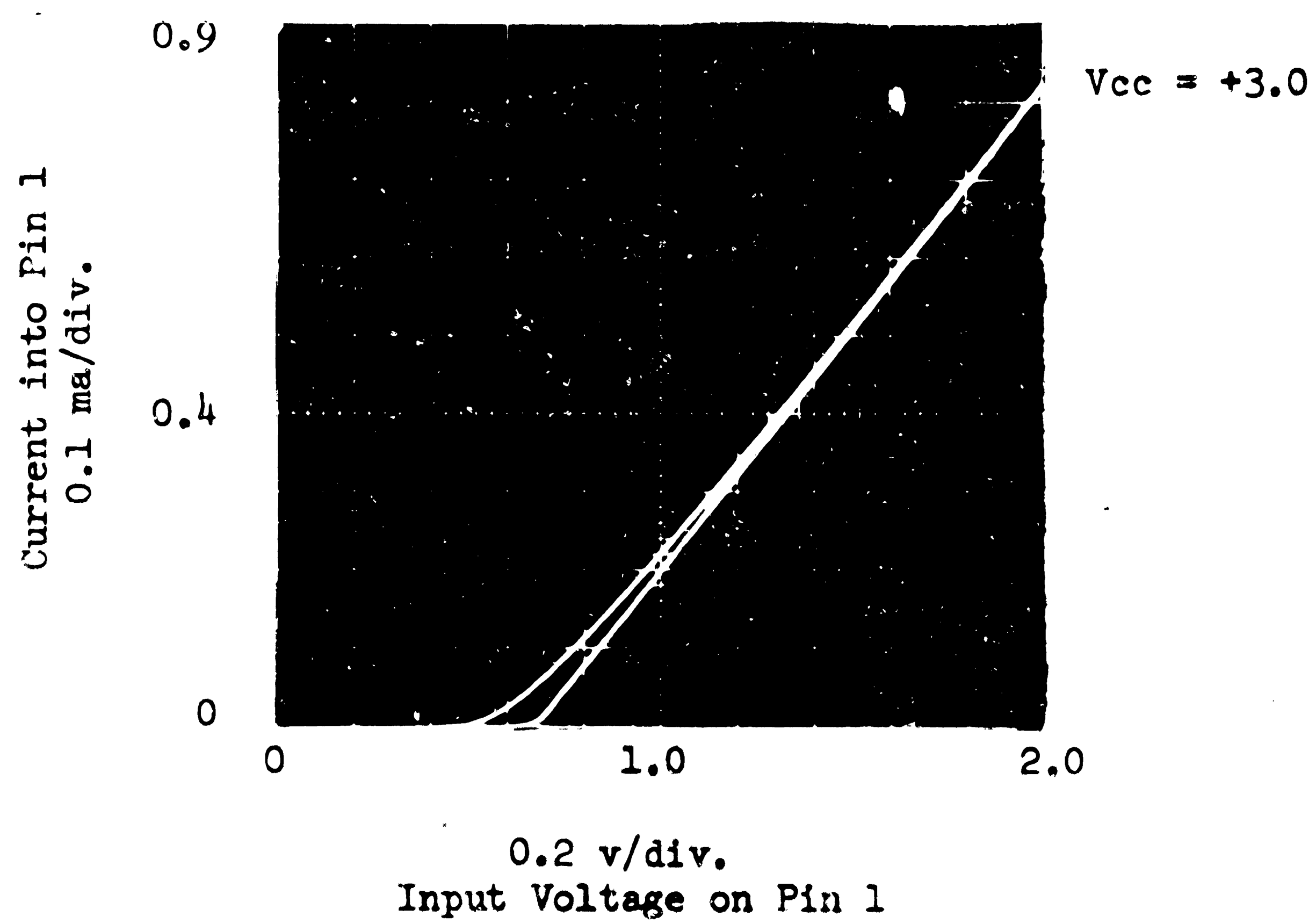


INPUT OUTPUT CHARACTERISTICS
DCTL G ELEMENT

3.2.11

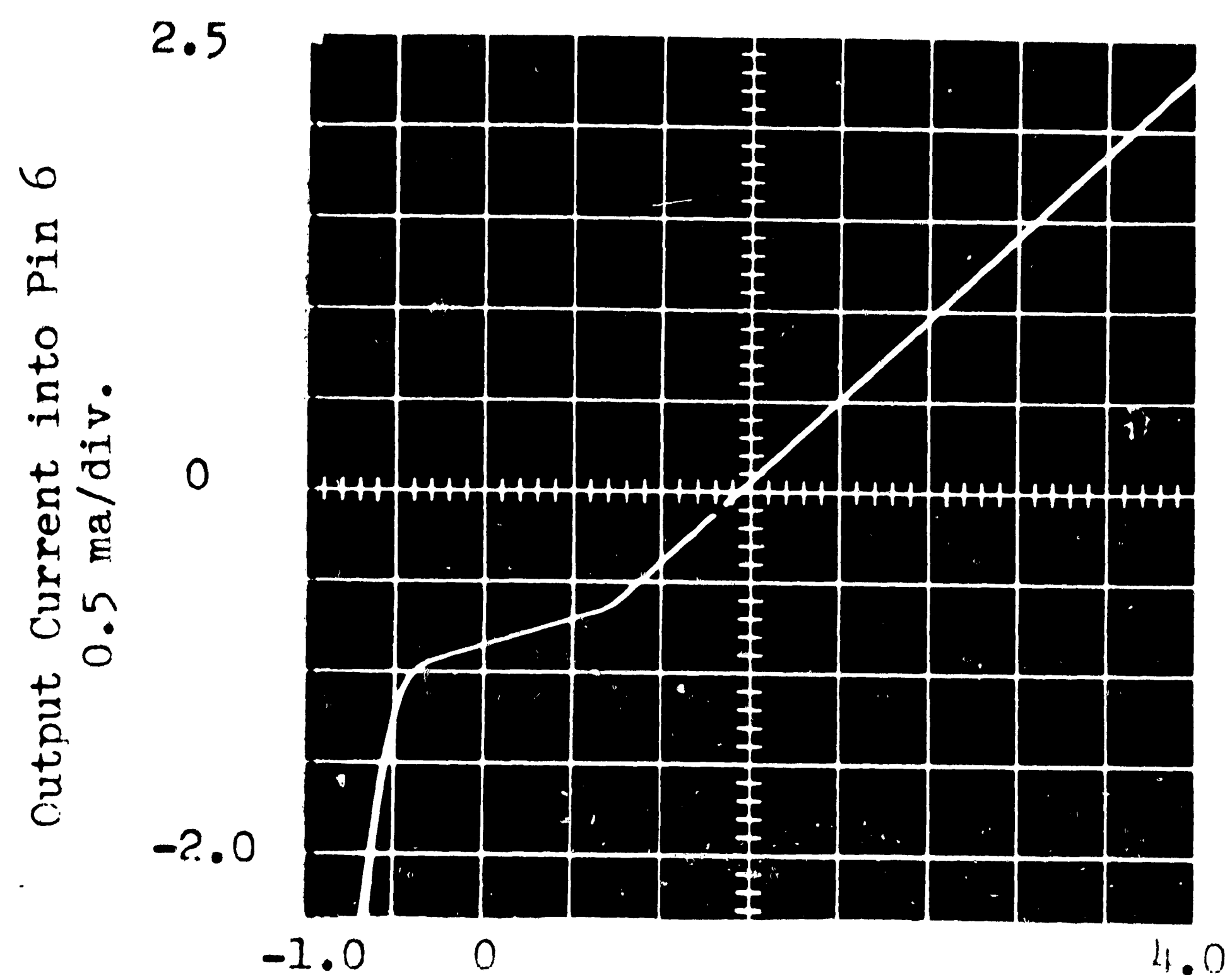


INPUT CHARACTERISTICS
DCTL 6 ELEMENT



NOTE: Bottom curve is with pins 2, 3, and 5 open.
Top curve is with pins 2, 3 and 5 at +3.0

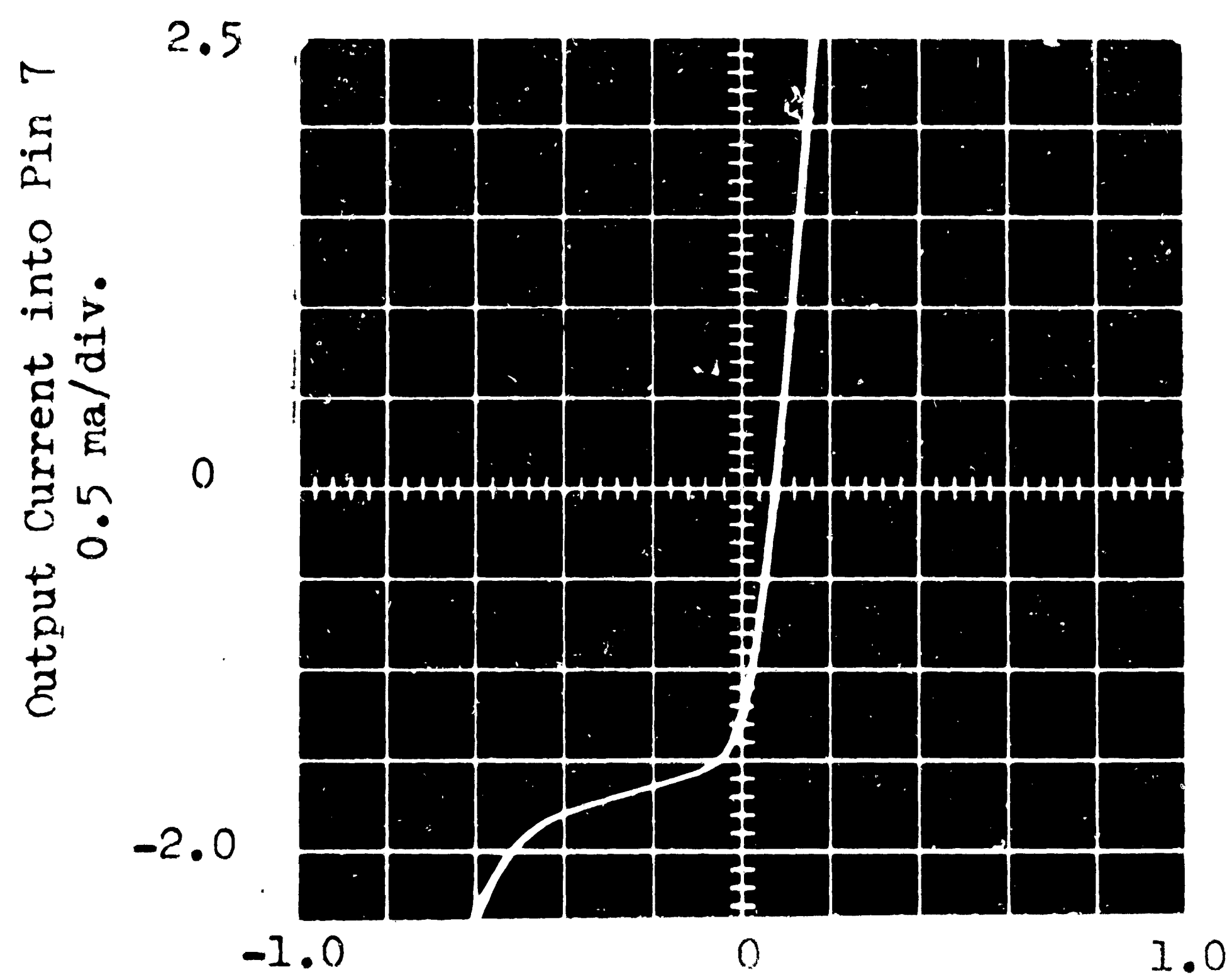
INPUT CHARACTERISTICS DCTL G ELEMENT



$V_{CC} = 3.0$

$V_i = 0$ V

0.5 V/div.
Output Voltage on Pin 6

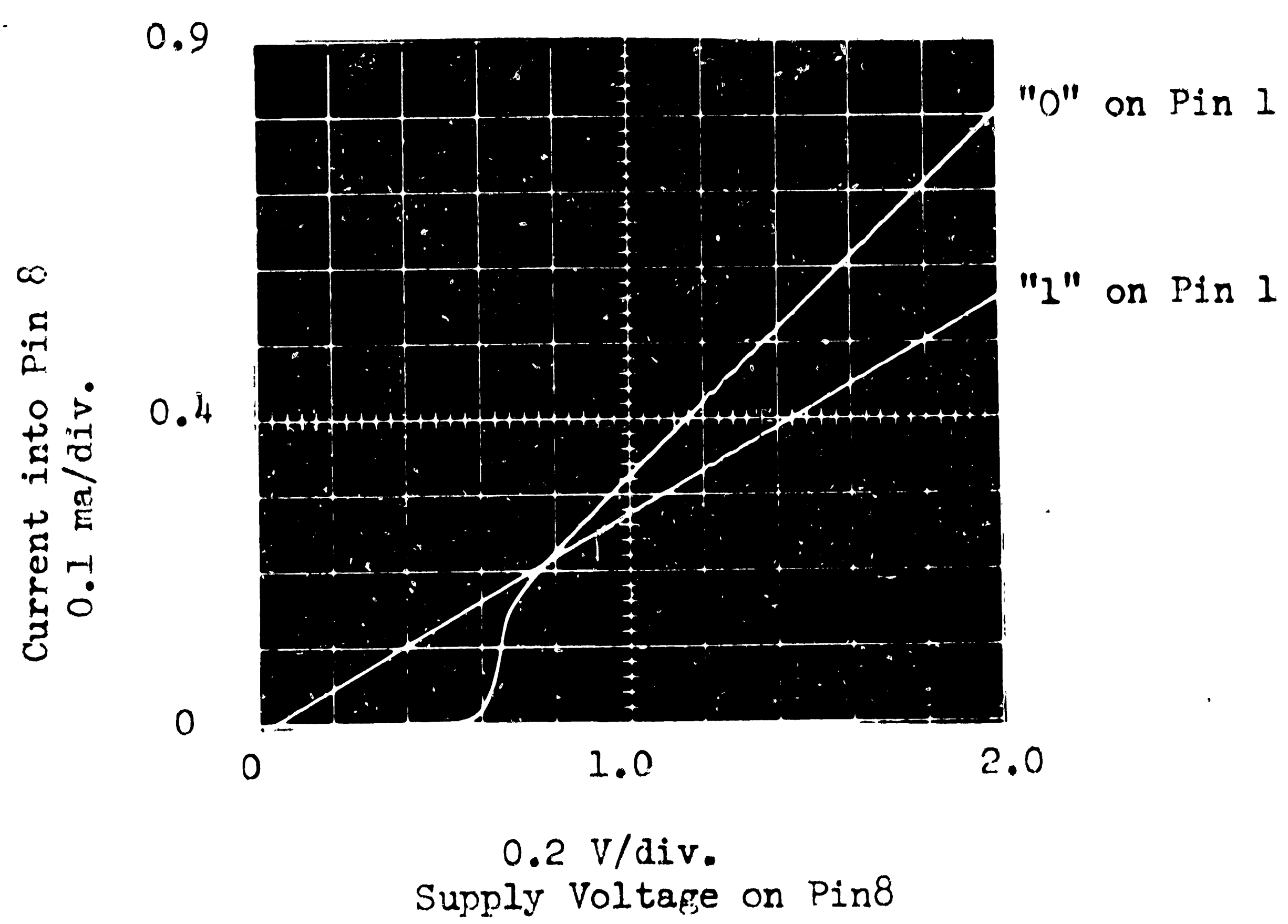


$V_{CC} = 3.0$

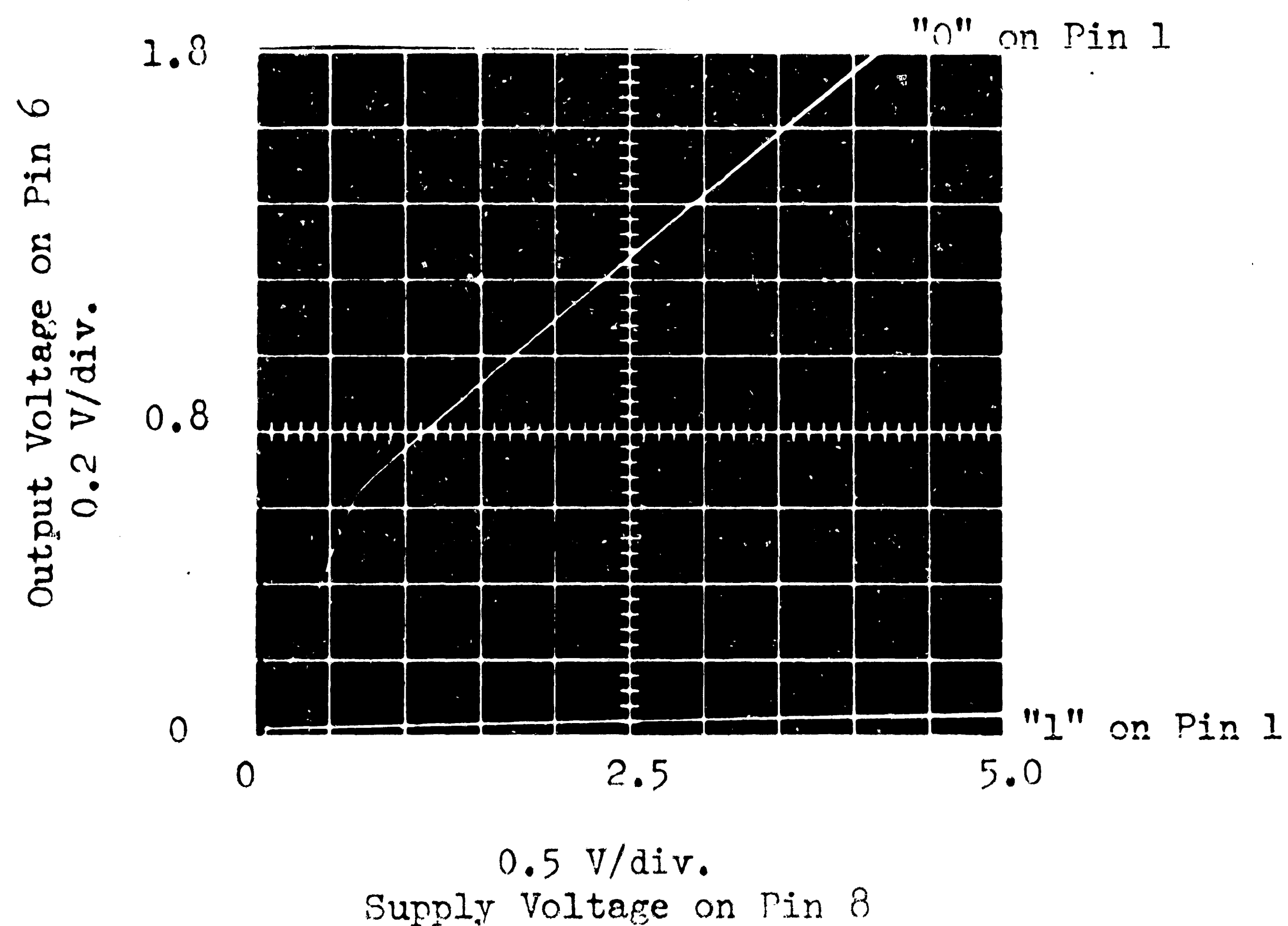
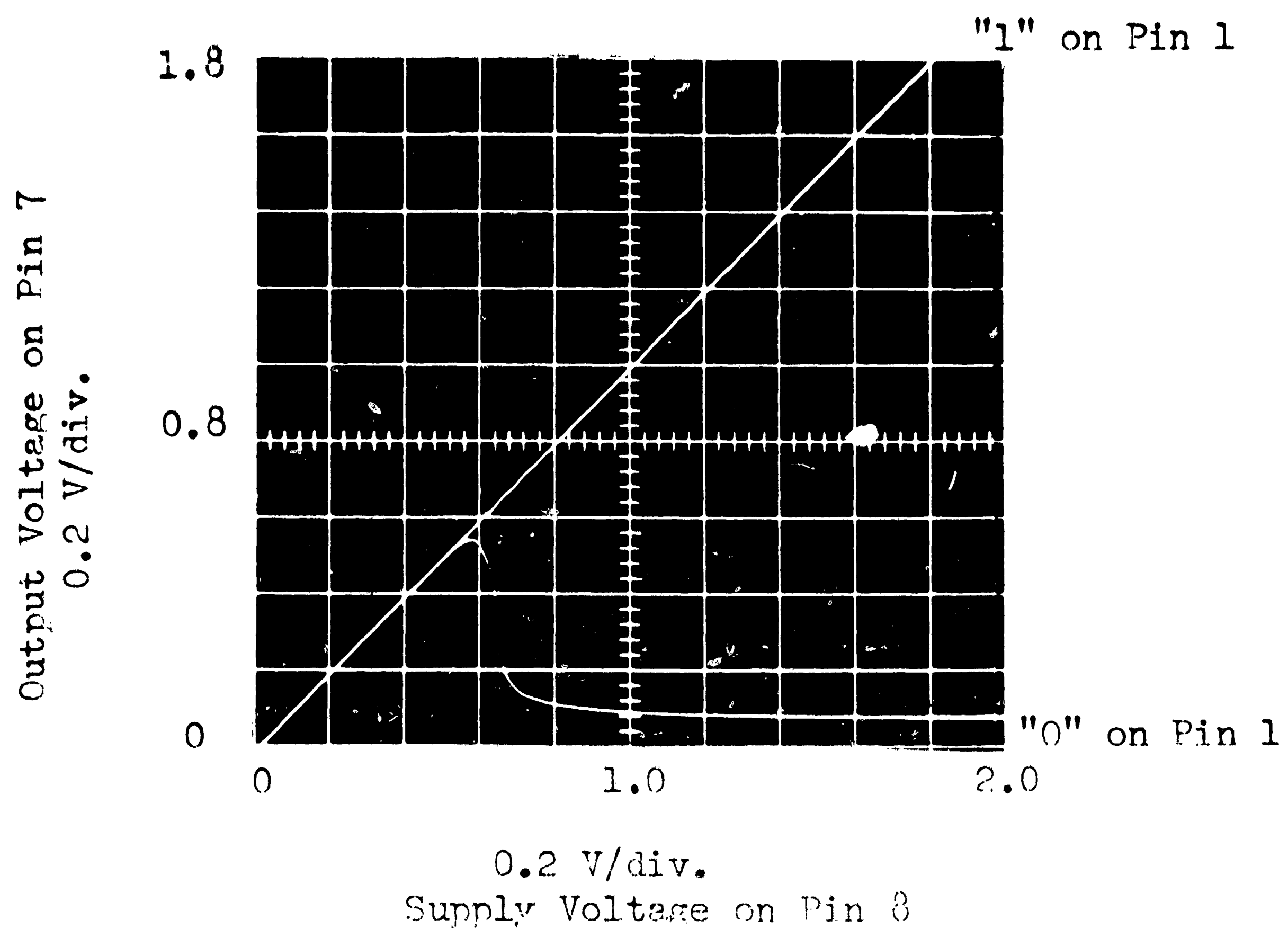
$V_i = 0$

0.2 V/div.
Output Voltage on Pin 7

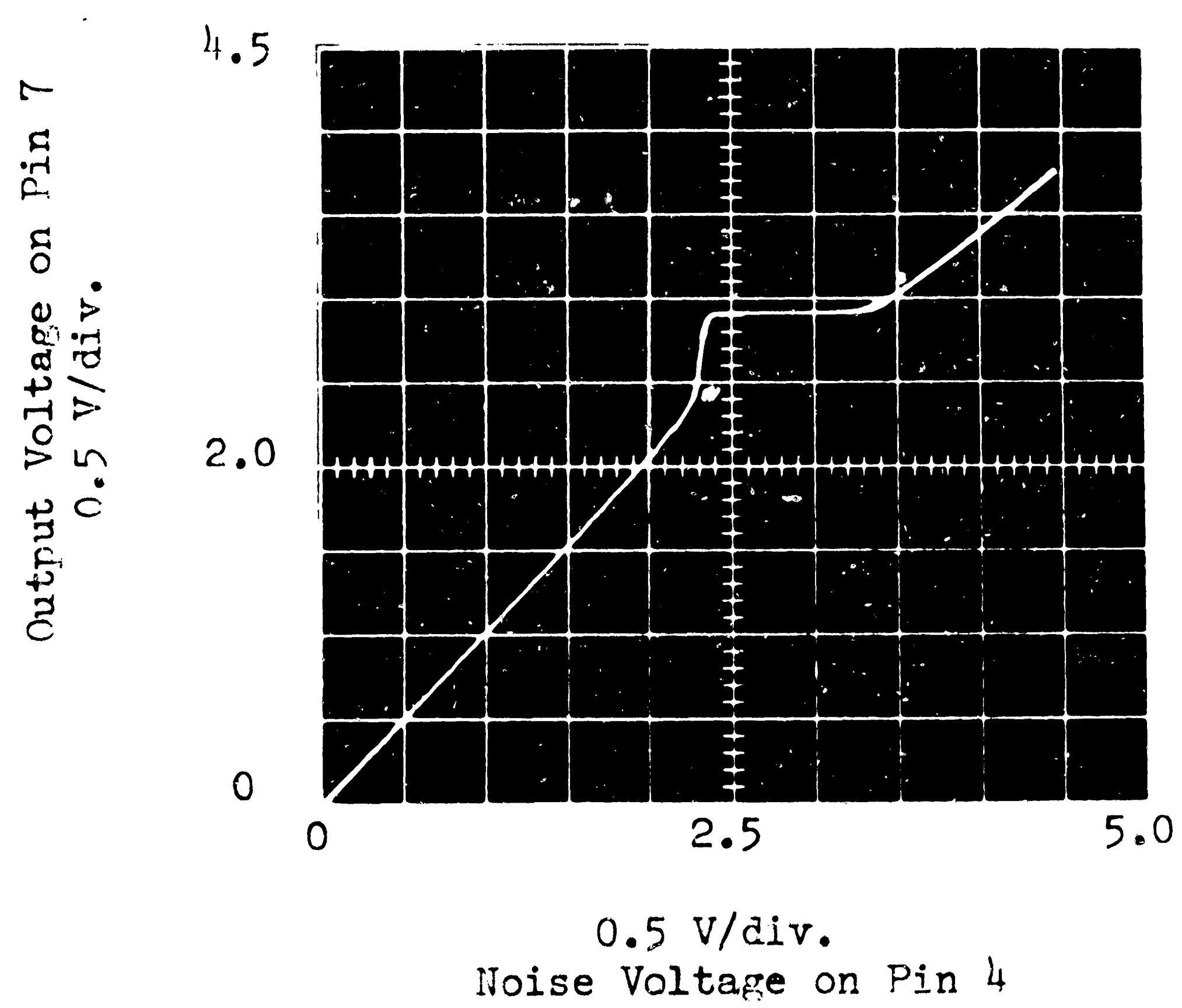
OUTPUT CHARACTERISTICS
DCTL G ELEMENT



POWER DISSIPATION
DCTL G ELEMENT

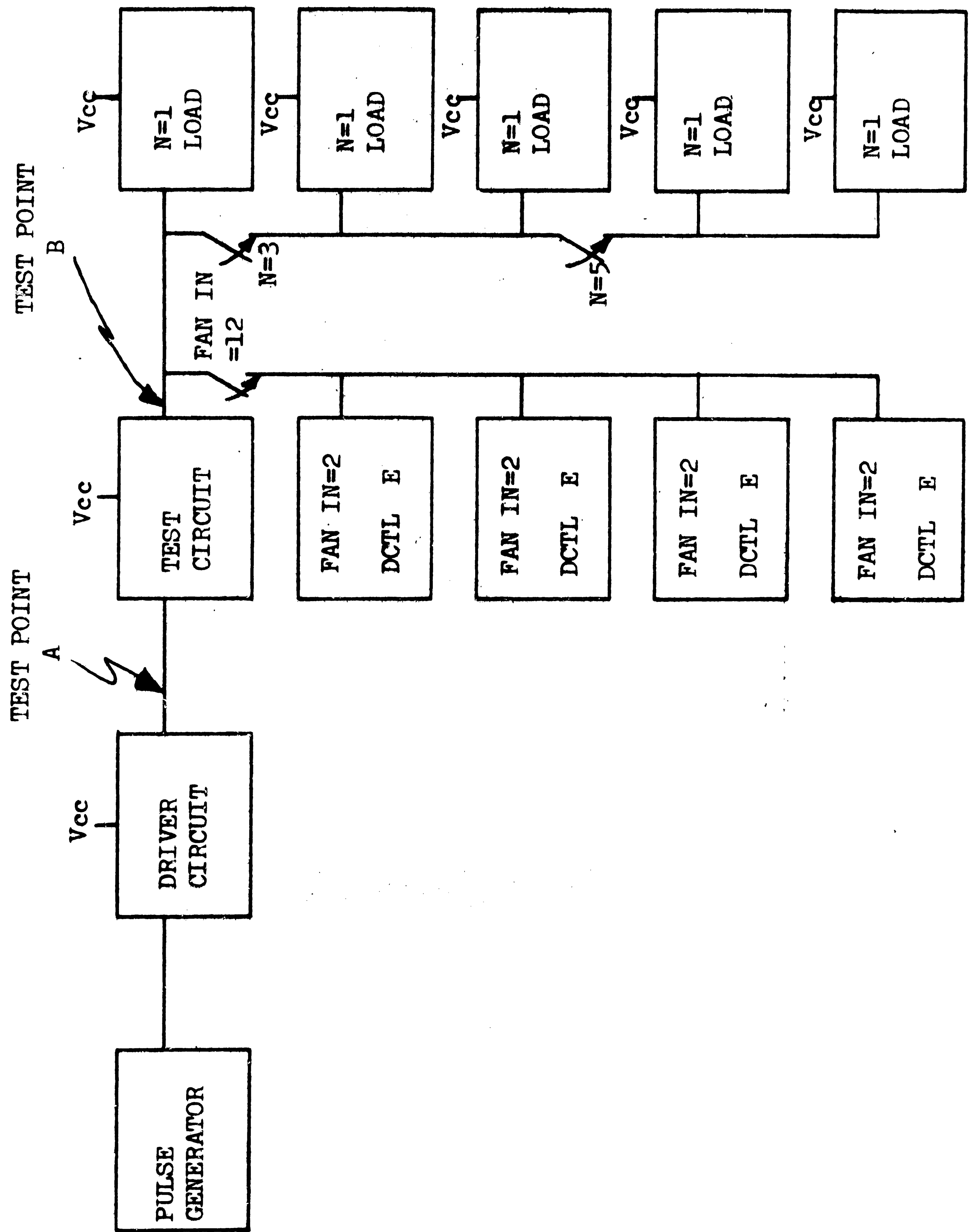


OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DCTL G ELEMENT

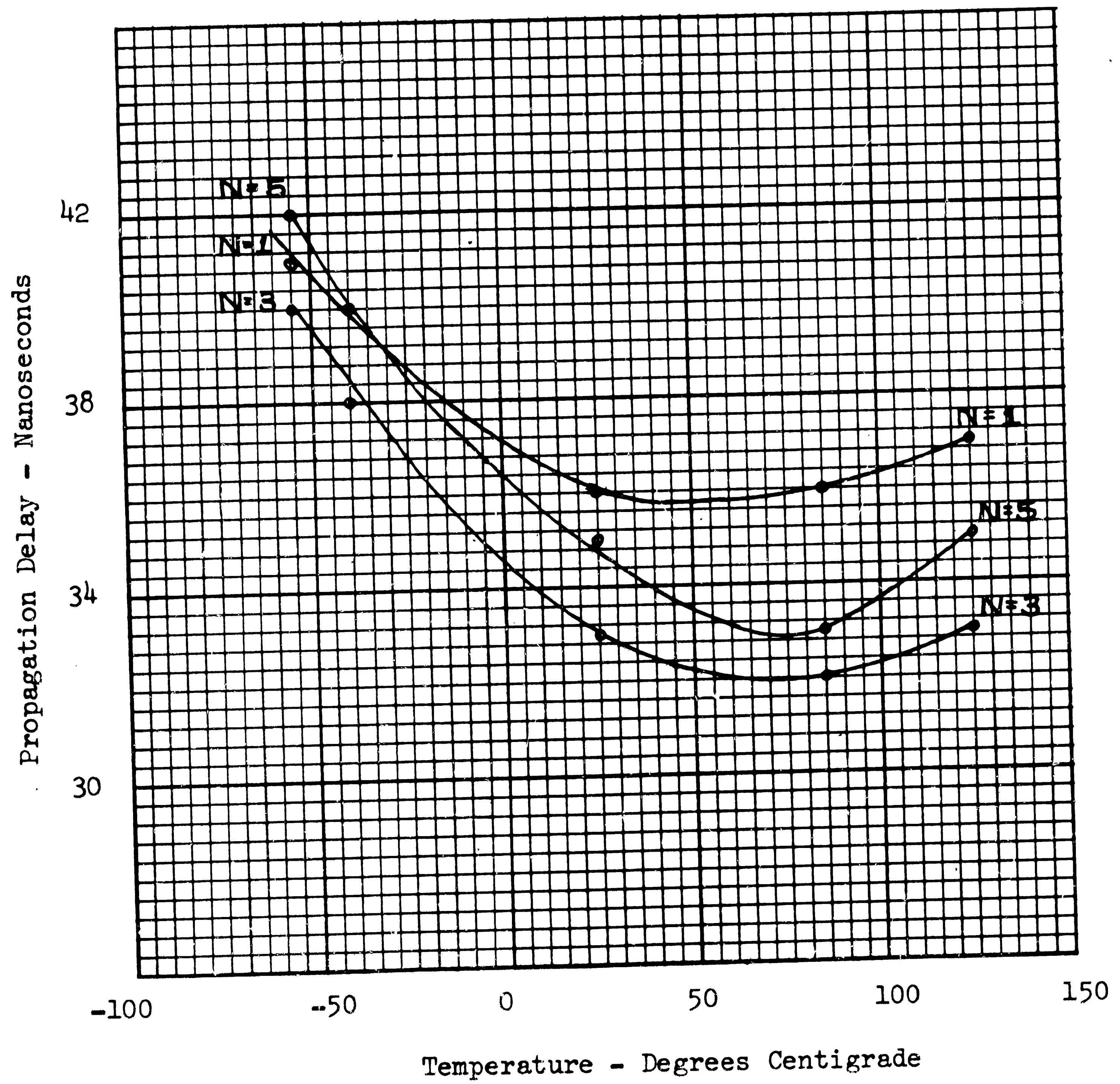


$V_{cc} = 3.0$

OUTPUT VOLTAGE versus NOISE VOLTAGE
DCTL G ELEMENT



TEST CIRCUIT FOR DCTL G GATE



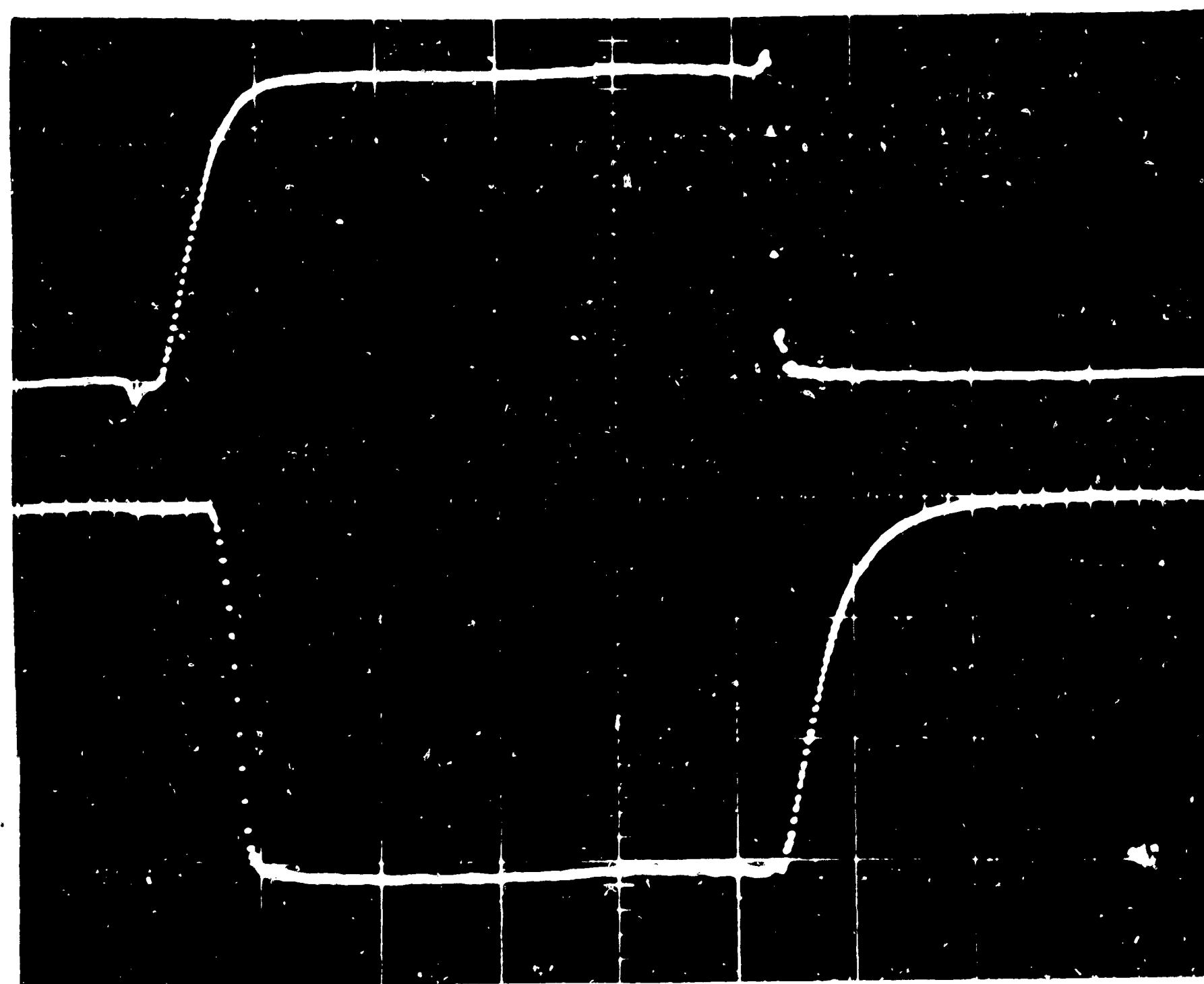
TEST CONDITIONS:
 DATA FOR GRAPH TAKEN WITH SUPPLY TO LOAD AND TEST
 CIRCUITS HELD CONSTANT AT 3.0 V

DCTL - G ELEMENT

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +25°C Vcc +3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>517.</u>	<u>506.</u>	<u>500.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.06</u>	<u>1.0</u>	<u>1.39</u>	<u>1.58</u>
T_r	<u>57.</u>	<u>98.</u>	<u>87.</u>	<u>83.</u>
T_f	<u>11.6</u>	<u>20.</u>	<u>21.</u>	<u>23.</u>
T_d		<u>44.</u>	<u>44.</u>	<u>45.</u>
T_s		<u>16.5</u>	<u>14.</u>	<u>13.</u>
T_{pd}		<u>40.</u>	<u>36.</u>	<u>35.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. -40°C Vcc +3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>508.</u>	<u>497.</u>	<u>491.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.15</u>	<u>1.08</u>	<u>1.37</u>	<u>1.66</u>
T _r	<u>58.</u>	<u>93.</u>	<u>82.</u>	<u>78.</u>
T _f	<u>11.</u>	<u>22.</u>	<u>24.</u>	<u>27.</u>
T _d		<u>51.</u>	<u>51.</u>	<u>52.</u>
T _s		<u>15.</u>	<u>13.</u>	<u>12.</u>
T _{pd}		<u>42.</u>	<u>40.</u>	<u>38.</u>

Type RTL No. G Temp. -55°C Vcc +3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>506.</u>	<u>494.</u>	<u>492.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.16</u>	<u>1.10</u>	<u>1.39</u>	<u>1.69</u>
T _r	<u>58.</u>	<u>95.</u>	<u>84.</u>	<u>79.</u>
T _f	<u>12.</u>	<u>23.</u>	<u>26.</u>	<u>28.</u>
T _d		<u>52.</u>	<u>53.</u>	<u>52.</u>
T _s		<u>14.</u>	<u>11.</u>	<u>11.</u>
T _{pd}		<u>44.</u>	<u>41.</u>	<u>38.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +85°C Vcc 3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>524.</u>	<u>513.</u>	<u>508.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.0</u>	<u>0.94</u>	<u>1.23</u>	<u>1.52</u>
T _r	<u>59.</u>	<u>100.</u>	<u>91.</u>	<u>88.</u>
T _f	<u>12.</u>	<u>21.</u>	<u>22.</u>	<u>23.</u>
T _d		<u>40.</u>	<u>41.</u>	<u>41.</u>
T _s		<u>19.</u>	<u>16.5</u>	<u>15.</u>
T _{pd}		<u>39.</u>	<u>36.</u>	<u>35.</u>

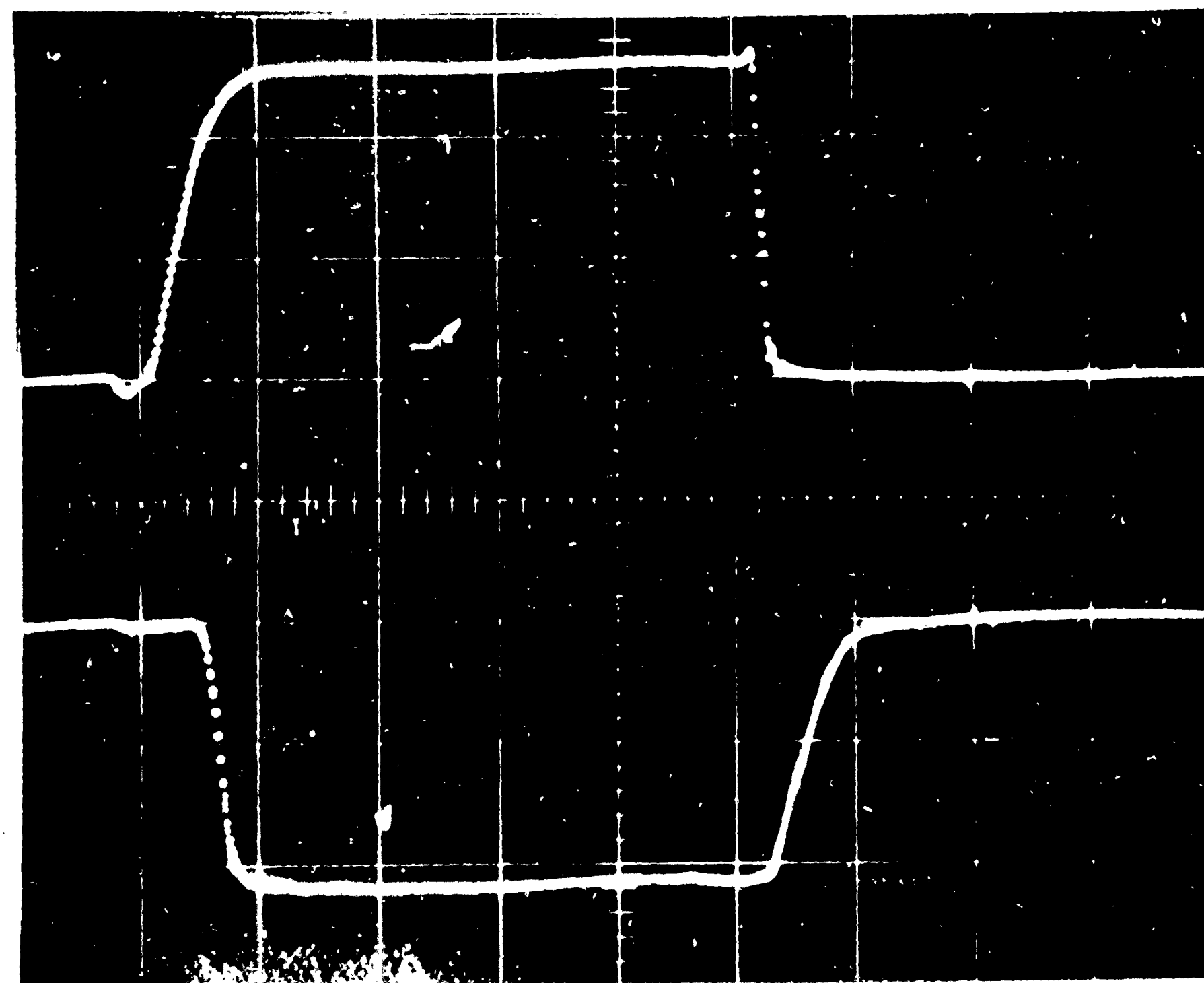
Type RTL No. G Temp. +125°C Vcc +3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>529.</u>	<u>518.</u>	<u>512.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.91</u>	<u>0.85</u>	<u>1.09</u>	<u>1.30</u>
T _r	<u>64.</u>	<u>103.</u>	<u>89.</u>	<u>82.</u>
T _f	<u>17.</u>	<u>25.</u>	<u>25.</u>	<u>25.</u>
T _d		<u>39.</u>	<u>40.</u>	<u>40.</u>
T _s		<u>23.</u>	<u>20.</u>	<u>18.</u>
T _{pd}		<u>40.</u>	<u>37.</u>	<u>35.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +25°C Vcc +3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>518.</u>	<u>503</u>	<u>497.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.08</u>	<u>0.78</u>	<u>0.90</u>	<u>1.02</u>
T_r	<u>56.</u>	<u>85.</u>	<u>62.</u>	<u>53.</u>
T_f	<u>12.</u>	<u>23.</u>	<u>24.</u>	<u>24.</u>
T_d		<u>43.</u>	<u>43.</u>	<u>43.</u>
T_s		<u>18.</u>	<u>14.</u>	<u>13.</u>
T_{pd}		<u>40.</u>	<u>33.</u>	<u>31.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. -40°C Vcc +3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>518.</u>	<u>500.</u>	<u>494.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.13</u>	<u>0.88</u>	<u>0.98</u>	<u>1.10</u>
T _r	<u>56.</u>	<u>90.</u>	<u>64.</u>	<u>54.</u>
T _f	<u>11.</u>	<u>25.</u>	<u>27.</u>	<u>27.</u>
T _d		<u>50.</u>	<u>51.</u>	<u>51.</u>
T _s		<u>16.</u>	<u>12.</u>	<u>10.</u>
T _{pd}		<u>45.</u>	<u>38.</u>	<u>35.</u>

Type RTL No. G Temp. -55°C Vcc +3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>518.</u>	<u>502.</u>	<u>495.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.18</u>	<u>0.90</u>	<u>1.02</u>	<u>1.12</u>
T _r	<u>57.</u>	<u>92.</u>	<u>65.</u>	<u>55.</u>
T _f	<u>11.</u>	<u>25.</u>	<u>26.</u>	<u>28.</u>
T _d		<u>53.</u>	<u>52.</u>	<u>53.</u>
T _s		<u>15.</u>	<u>11.</u>	<u>10.</u>
T _{pd}		<u>46.</u>	<u>40.</u>	<u>37.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +85°C Vcc +3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>524.</u>	<u>512.</u>	<u>506.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>.99</u>	<u>0.70</u>	<u>0.82</u>	<u>0.934</u>
T _r	<u>60.</u>	<u>83.</u>	<u>62.</u>	<u>55.</u>
T _f	<u>11.</u>	<u>27.</u>	<u>26.</u>	<u>26.</u>
T _d		<u>38.</u>	<u>38.</u>	<u>39.</u>
T _s		<u>18.</u>	<u>16.</u>	<u>14.</u>
T _{pd}		<u>38.</u>	<u>32.</u>	<u>31.</u>

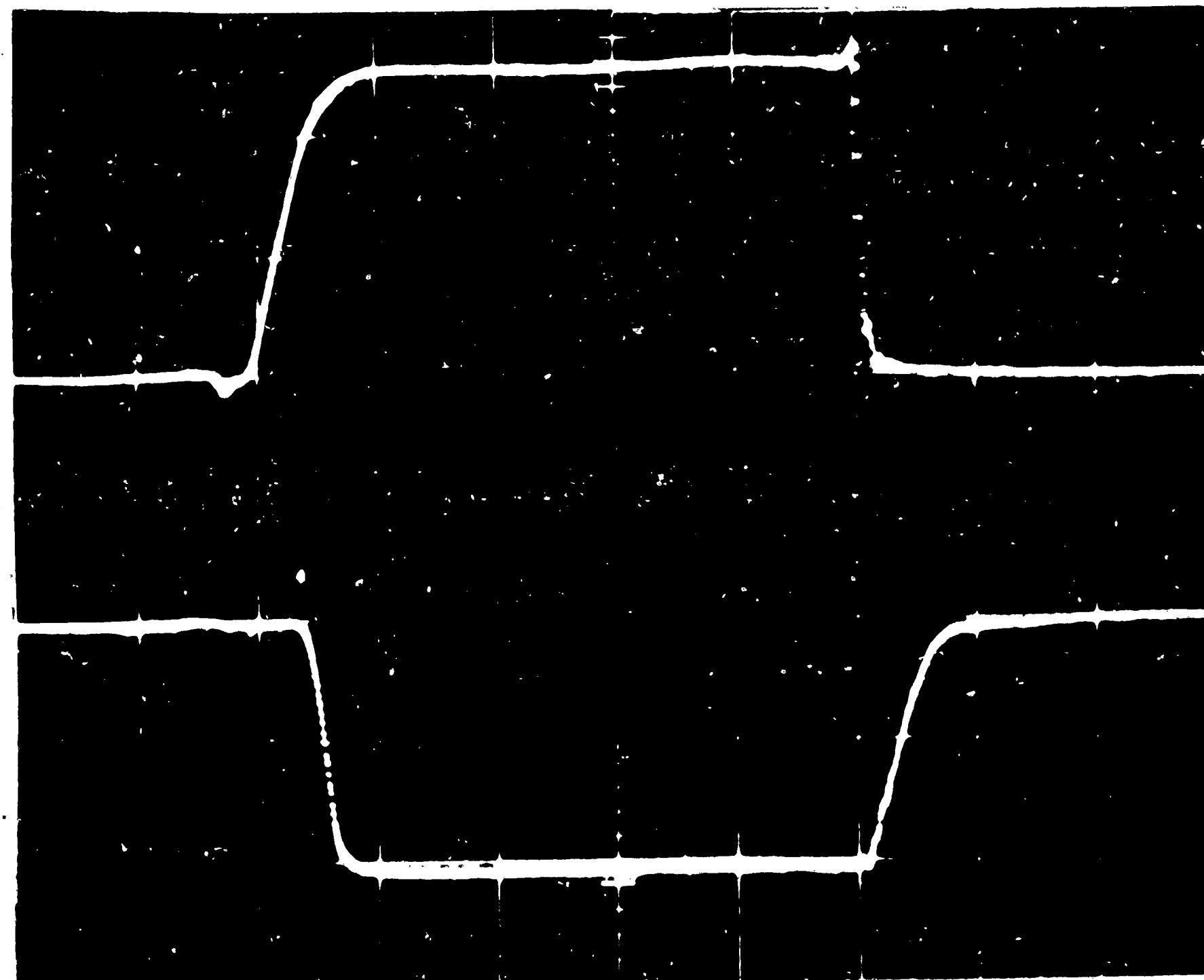
Type RTL No. G Temp. +125°C Vcc +3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>530.</u>	<u>517.</u>	<u>508.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.89</u>	<u>0.62</u>	<u>0.72</u>	<u>0.83</u>
T _r	<u>63.</u>	<u>84.</u>	<u>65.</u>	<u>58.</u>
T _f	<u>12.</u>	<u>32.</u>	<u>30.</u>	<u>29.</u>
T _d		<u>37.</u>	<u>37.</u>	<u>37.</u>
T _s		<u>22.</u>	<u>18.</u>	<u>16.</u>
T _{pd}		<u>39.</u>	<u>33.</u>	<u>31.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +25°C Vcc +3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>523.</u>	<u>506.</u>	<u>497.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.06</u>	<u>0.74</u>	<u>0.80</u>	<u>0.87</u>
T_r	<u>56.</u>	<u>95.</u>	<u>64.</u>	<u>53.</u>
T_f	<u>11.</u>	<u>26.</u>	<u>26.</u>	<u>26.</u>
T_d		<u>43.</u>	<u>43.</u>	<u>43.</u>
T_s		<u>15.</u>	<u>12.</u>	<u>10.</u>
T_{pd}		<u>43.</u>	<u>35.</u>	<u>32.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. -40°C Vcc +3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>518.</u>	<u>500.</u>	<u>490.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.16</u>	<u>0.86</u>	<u>0.93</u>	<u>1.0</u>
T _r	<u>58.</u>	<u>107.</u>	<u>72.</u>	<u>58.</u>
T _f	<u>14.</u>	<u>29.</u>	<u>29.</u>	<u>29.</u>
T _d		<u>49.</u>	<u>49.</u>	<u>50.</u>
T _s		<u>18.</u>	<u>11.</u>	<u>10.</u>
T _{pd}		<u>50.</u>	<u>40.</u>	<u>37.</u>

Type RTL No. G Temp. -55°C Vcc +3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>515.</u>	<u>496.</u>	<u>487.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.18</u>	<u>0.88</u>	<u>0.95</u>	<u>1.02</u>
T _r	<u>59.</u>	<u>113.</u>	<u>77.</u>	<u>60.</u>
T _f	<u>12.</u>	<u>29.</u>	<u>30.</u>	<u>32.</u>
T _d		<u>51.</u>	<u>51.</u>	<u>51.</u>
T _s		<u>16.</u>	<u>10.</u>	<u>9.</u>
T _{pd}		<u>52.</u>	<u>42.</u>	<u>38.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +85°C Vcc +3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>527.</u>	<u>510.</u>	<u>503.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.98</u>	<u>0.64</u>	<u>0.71</u>	<u>0.78</u>
T _r	<u>59.</u>	<u>97.</u>	<u>63.</u>	<u>51.</u>
T _f	<u>12.</u>	<u>40.</u>	<u>37.</u>	<u>36.</u>
T _d		<u>40.</u>	<u>40.</u>	<u>40.</u>
T _s		<u>17.</u>	<u>15.</u>	<u>12.</u>
T _{pd}		<u>42.</u>	<u>33.</u>	<u>31.</u>

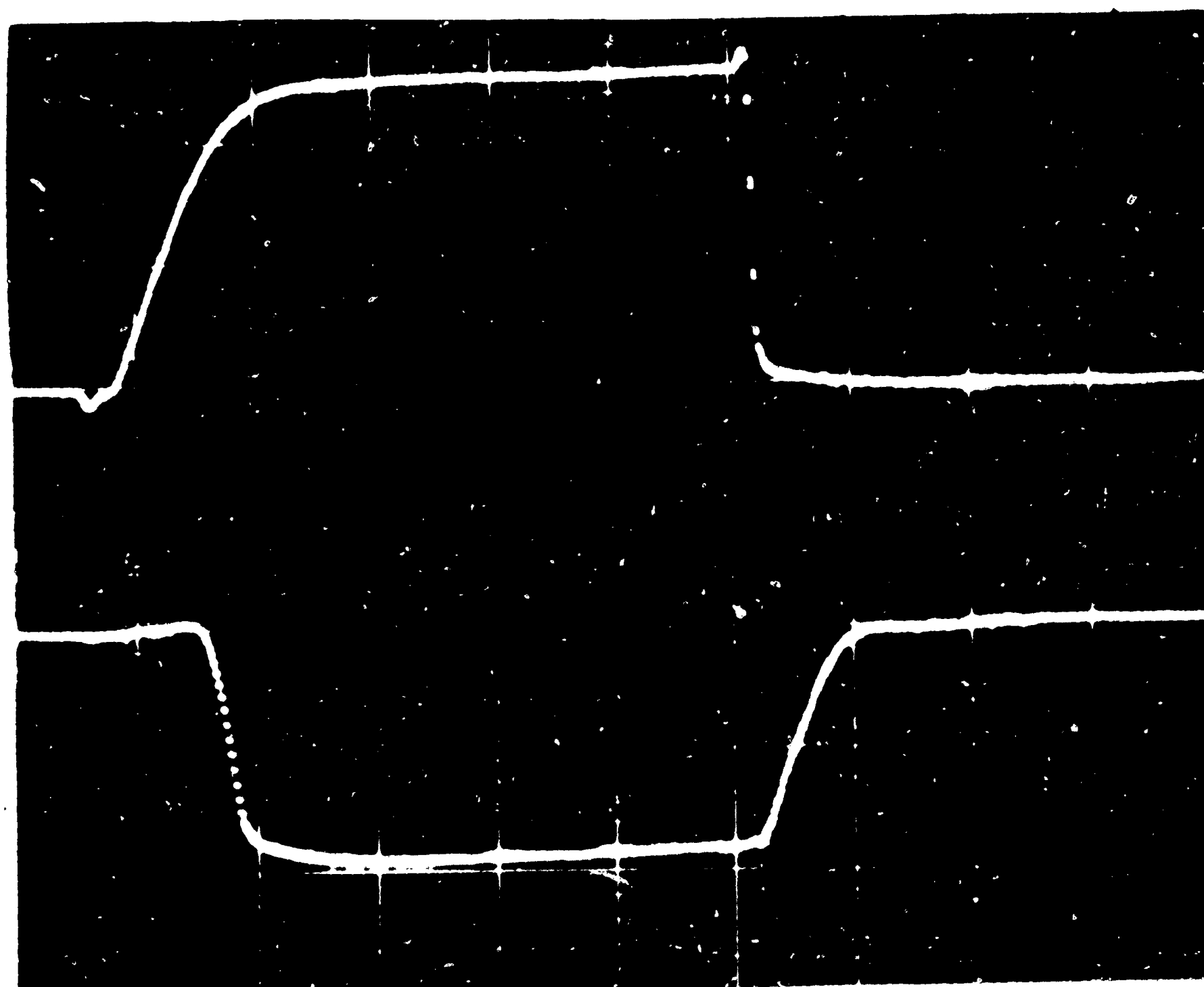
Type RTL No. G Temp. +125°C Vcc +3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>527.</u>	<u>513.</u>	<u>507.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.91</u>	<u>0.56</u>	<u>0.62</u>	<u>0.79</u>
T _r	<u>63.</u>	<u>92.</u>	<u>68.</u>	<u>54.</u>
T _f	<u>17.</u>	<u>50.</u>	<u>44.</u>	<u>42.</u>
T _d		<u>39.</u>	<u>39.</u>	<u>39.</u>
T _s		<u>18.</u>	<u>16.</u>	<u>16.</u>
T _{pd}		<u>40</u>	<u>35</u>	<u>32</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +25°C Vcc 3.0 N = 5 FAN IN = 12

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>508.</u>	<u>492.</u>	<u>484.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.08</u>	<u>0.73</u>	<u>0.80</u>	<u>0.87</u>
T_r	<u>97.</u>	<u>97.</u>	<u>67.</u>	<u>53.</u>
T_f	<u>13.</u>	<u>34.</u>	<u>34.</u>	<u>35.</u>
T_d		<u>67.</u>	<u>67.</u>	<u>67.</u>
T_s		<u>15.</u>	<u>11.</u>	<u>10.</u>
T_{pd}		<u>49.</u>	<u>41.</u>	<u>38.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. -40°C Vcc 3.0 N = 5 FAN IN = 12

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>499.</u>	<u>481.</u>	<u>473.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.19</u>	<u>0.85</u>	<u>0.918</u>	<u>0.98</u>
T _r	<u>97.</u>	<u>106.</u>	<u>71.</u>	<u>56.</u>
T _f	<u>12.</u>	<u>33.</u>	<u>35.</u>	<u>36.</u>
T _d		<u>76.</u>	<u>75.</u>	<u>76.</u>
T _s		<u>15.</u>	<u>10.</u>	<u>9.</u>
T _{pd}		<u>56.</u>	<u>47.</u>	<u>44.</u>

Type RTL No. G Temp. -55°C Vcc 3.0 N = 5 FAN IN = 12

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>498.</u>	<u>477.</u>	<u>468.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.18</u>	<u>0.87</u>	<u>0.94</u>	<u>1.01</u>
T _r	<u>97.</u>	<u>115.</u>	<u>73.</u>	<u>57.</u>
T _f	<u>12.</u>	<u>35.</u>	<u>37.</u>	<u>40.</u>
T _d		<u>80.</u>	<u>79.</u>	<u>78.</u>
T _s		<u>15.</u>	<u>10.</u>	<u>9.</u>
T _{pd}		<u>60.</u>	<u>50.</u>	<u>46.</u>

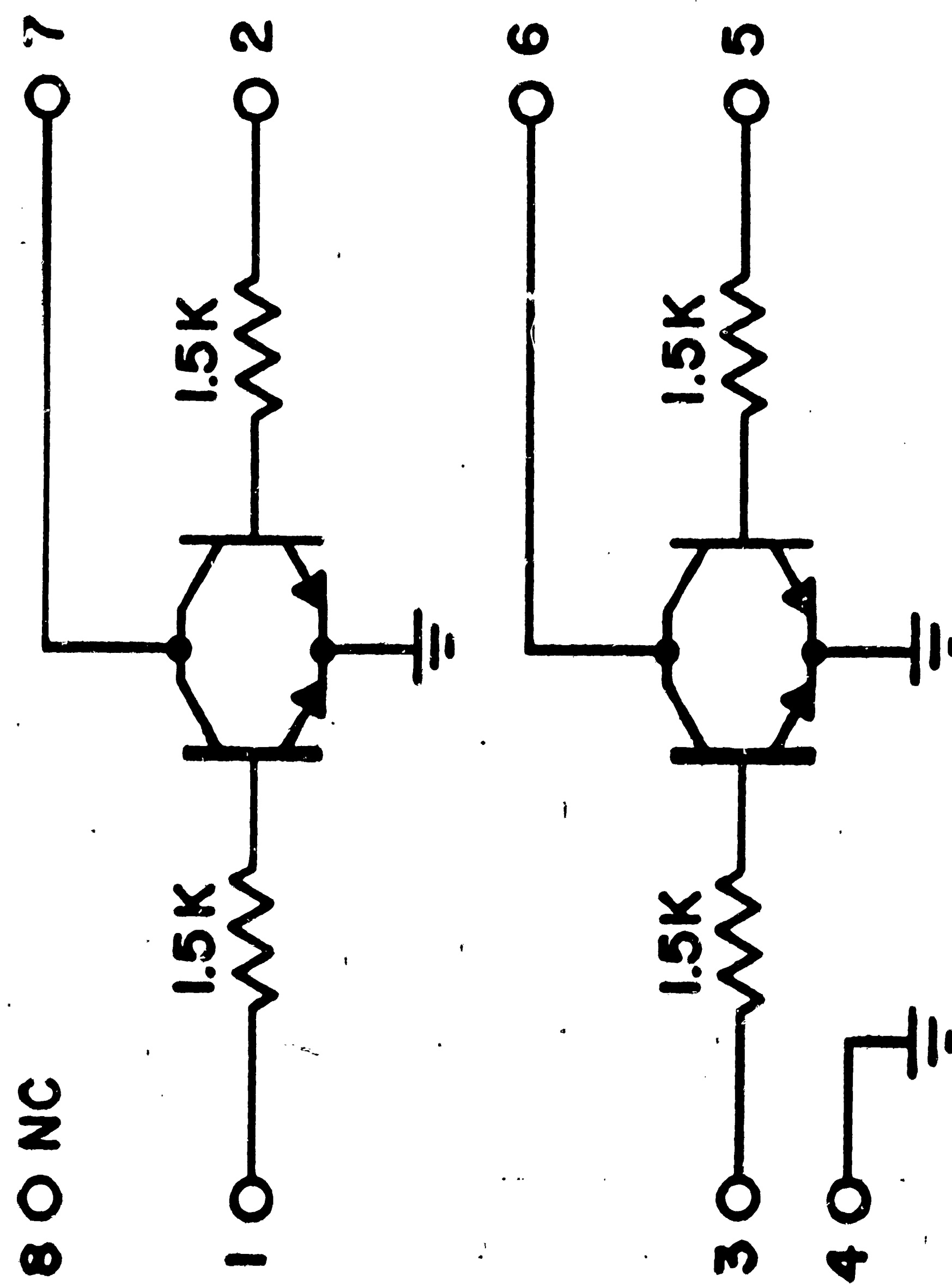
GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +85°C Vcc 3.0 N = 5 FAN IN = 12

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>517.</u>	<u>502.</u>	<u>495.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.99</u>	<u>0.62</u>	<u>0.69</u>	<u>0.76</u>
T_r	<u>106.</u>	<u>95.</u>	<u>65.</u>	<u>52.</u>
T_f	<u>14.</u>	<u>44.</u>	<u>42.</u>	<u>41.</u>
T_d		<u>60.</u>	<u>60.</u>	<u>60.</u>
T_s		<u>18.</u>	<u>15.</u>	<u>13.</u>
T_{pd}		<u>45.</u>	<u>38.</u>	<u>35</u>

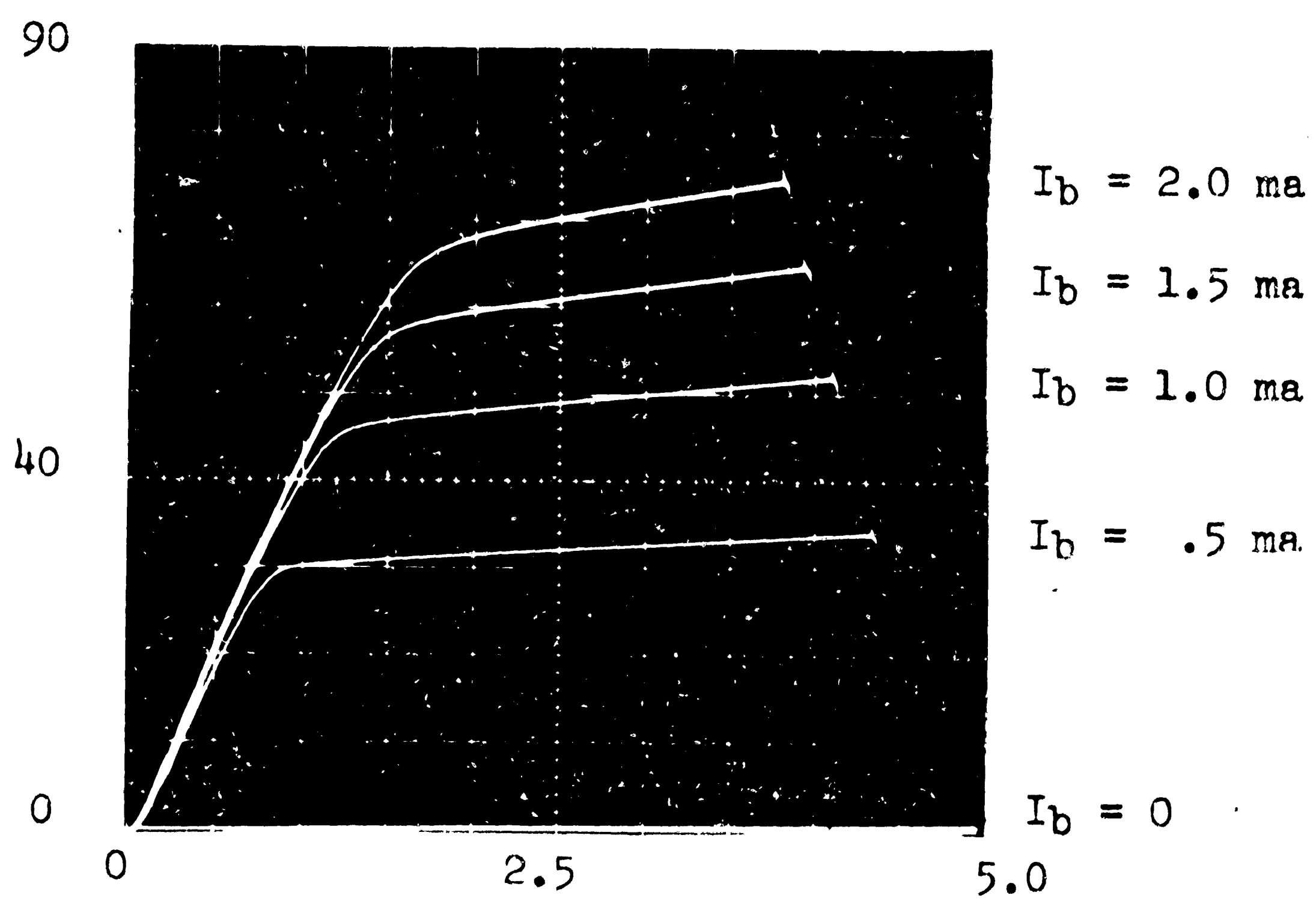
Type RTL No. G Temp. +125°C Vcc 3.0 N = 5 FAN IN = 12

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>522.</u>	<u>507.</u>	<u>499.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.90</u>	<u>0.54</u>	<u>0.60</u>	<u>0.67</u>
T_r	<u>118.</u>	<u>98.</u>	<u>67.</u>	<u>54.</u>
T_f	<u>16.</u>	<u>55.</u>	<u>53.</u>	<u>52.</u>
T_d		<u>59.</u>	<u>59.</u>	<u>54.</u>
T_s		<u>21.</u>	<u>17.</u>	<u>15.</u>
T_{pd}		<u>45.</u>	<u>37.</u>	<u>35.</u>



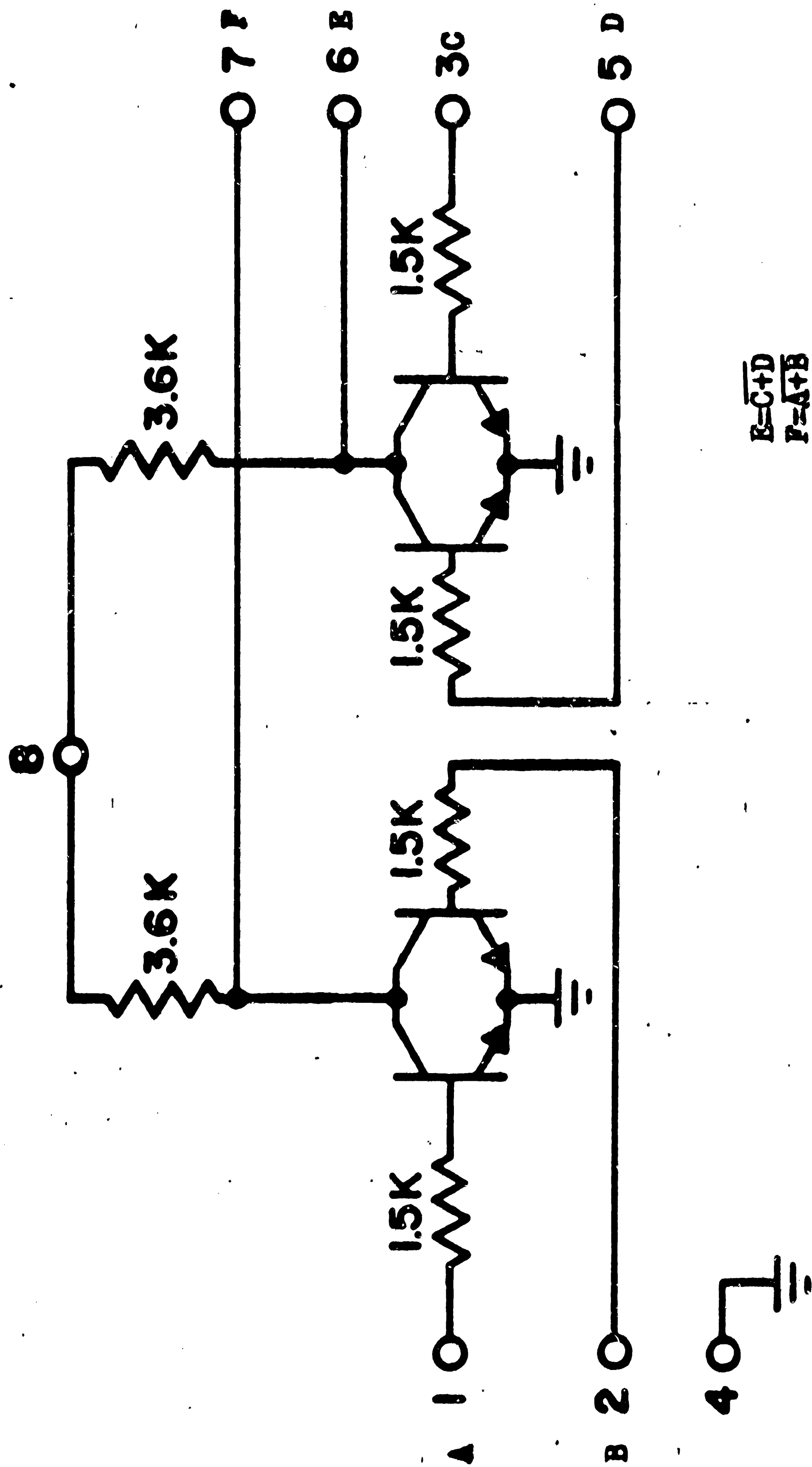
DUAL 2 - INPUT DCTL EXPANDER GATE, E

Collector Current into Pin 7
10 ma/div

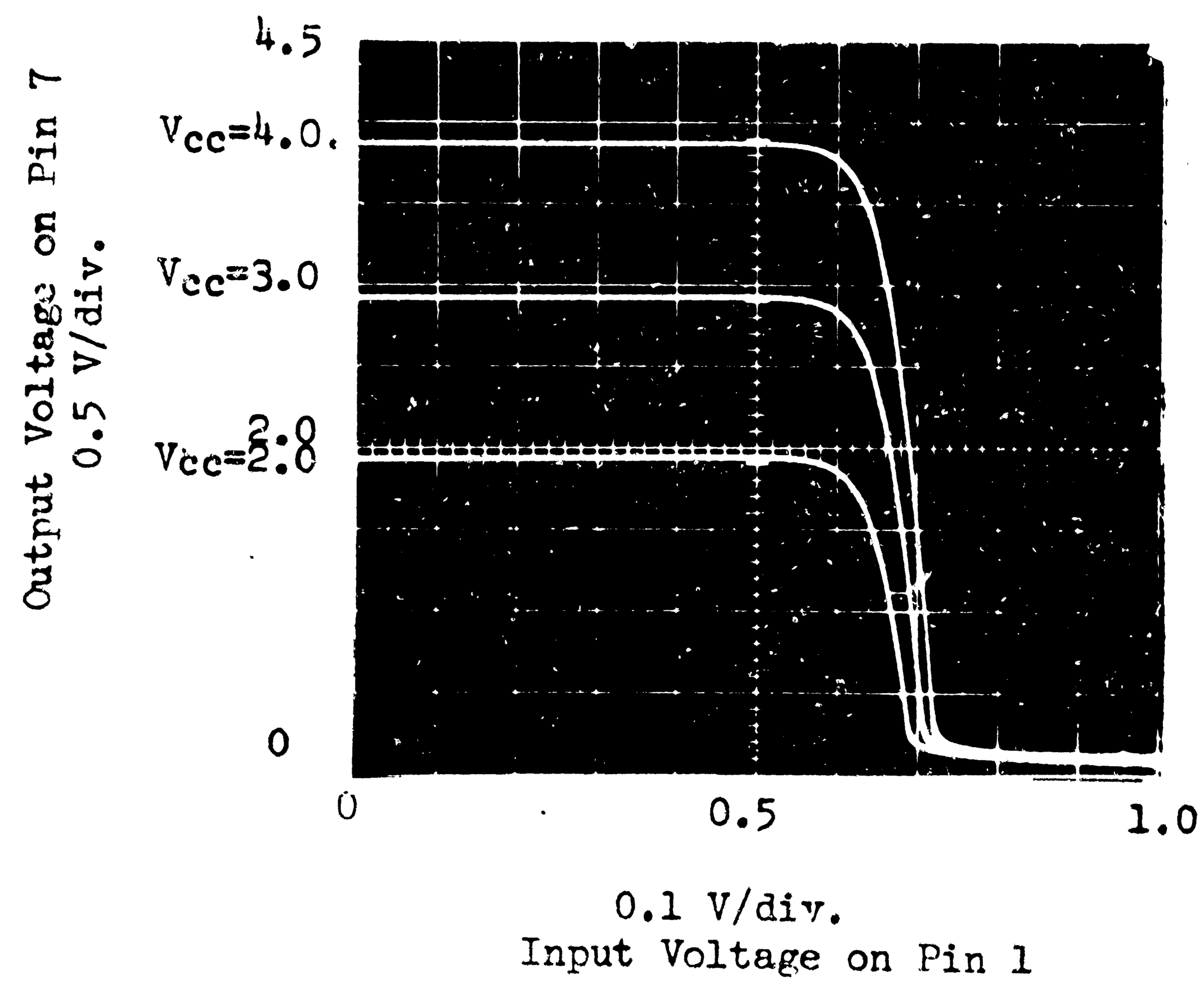


0.5 V/div.
Collector voltage on Pin 7

TRANSISTOR CHARACTERISTICS
DCTL E ELEMENT

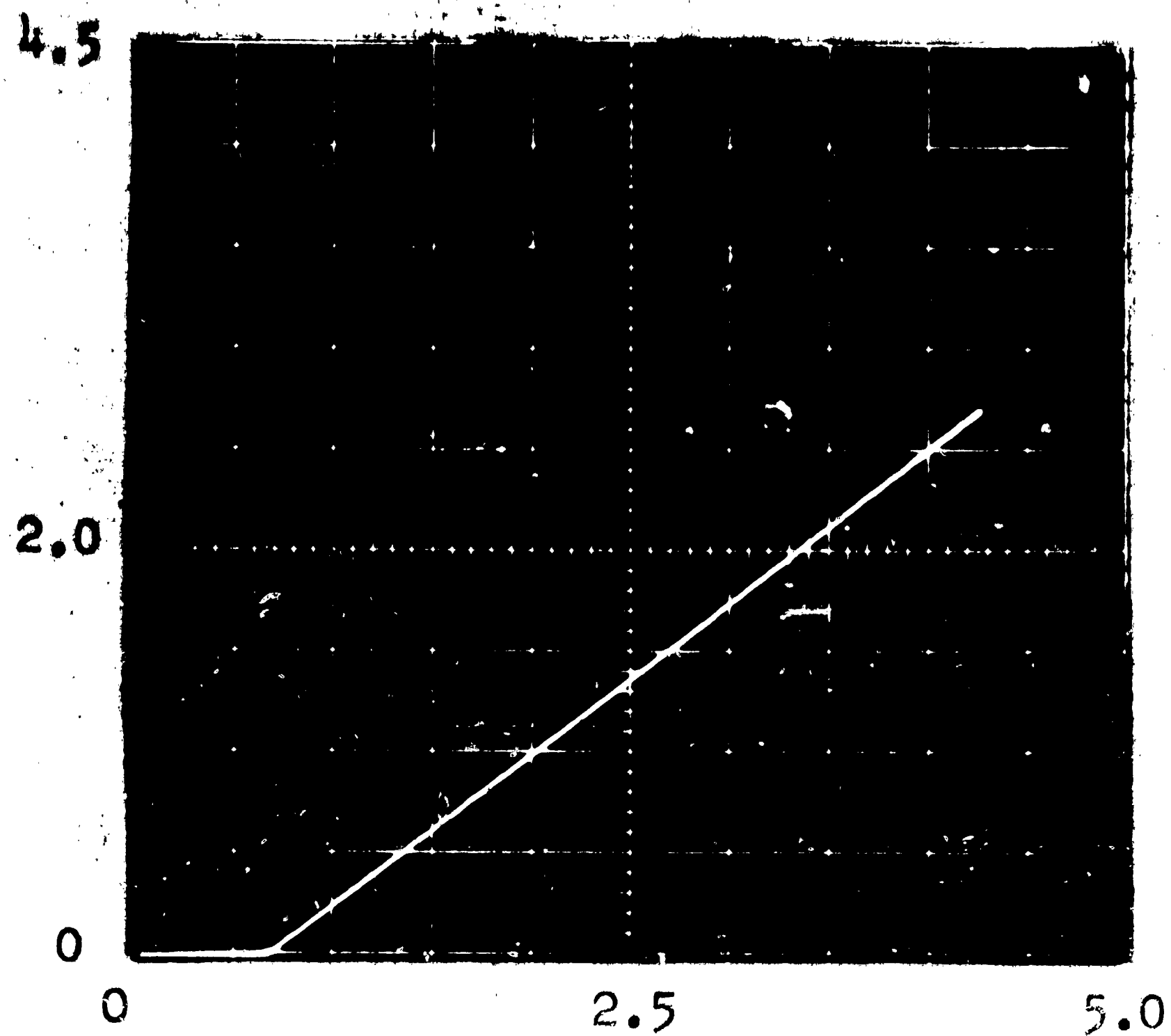


DUAL 2 - INPUT DCTL GATE, D₂



INPUT OUTPUT CHARACTERISTICS
DCTL D₂ ELEMENT

Input Current into Pin 1
0.5 ma/div.

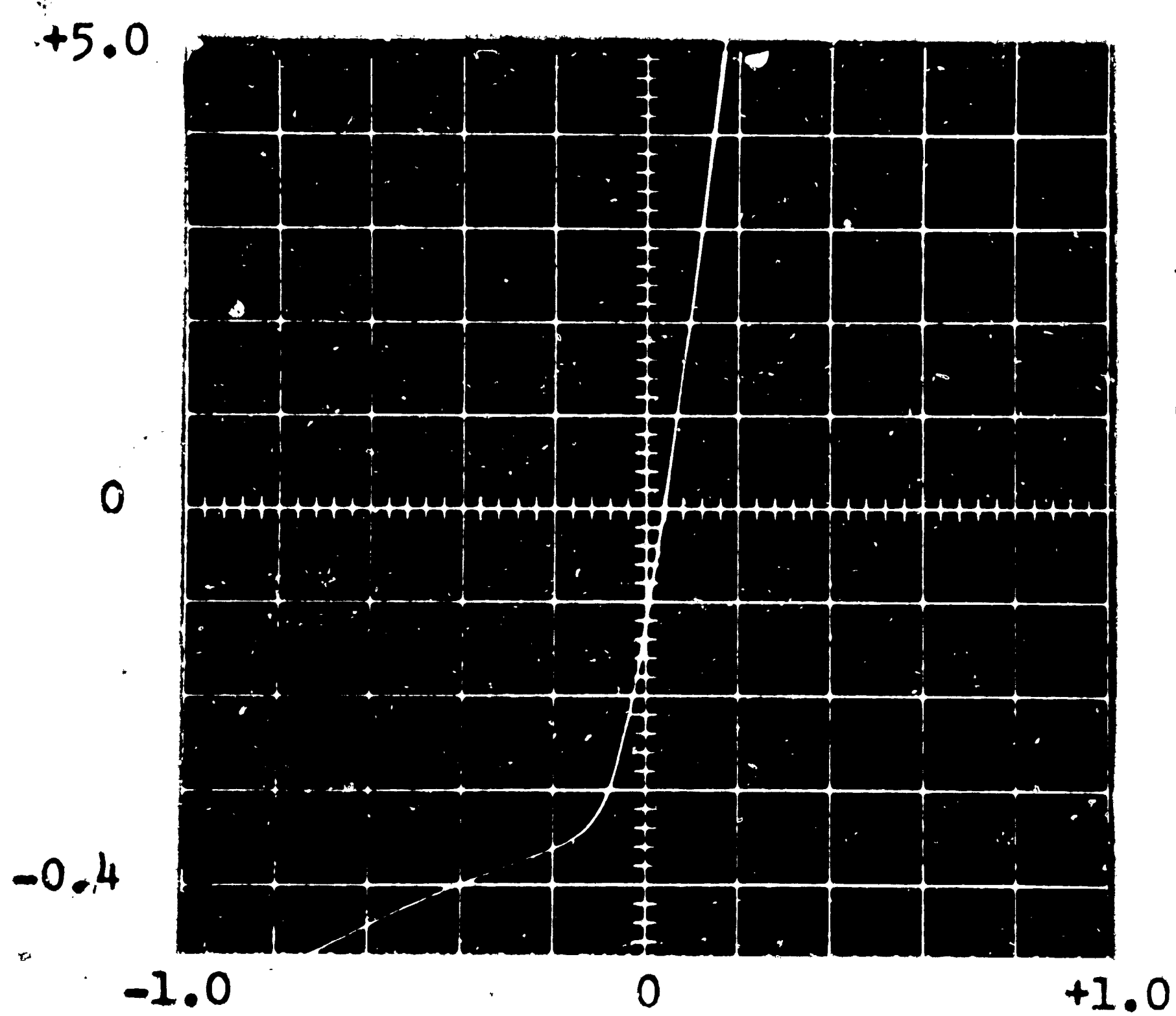


$V_{CC} = +3.0$

0.5 V/div.
Input Voltage on Pin 1

INPUT CHARACTERISTICS

Output Current into Pin 7
1.0 ma/div.



$V_{CC} = +3.0$

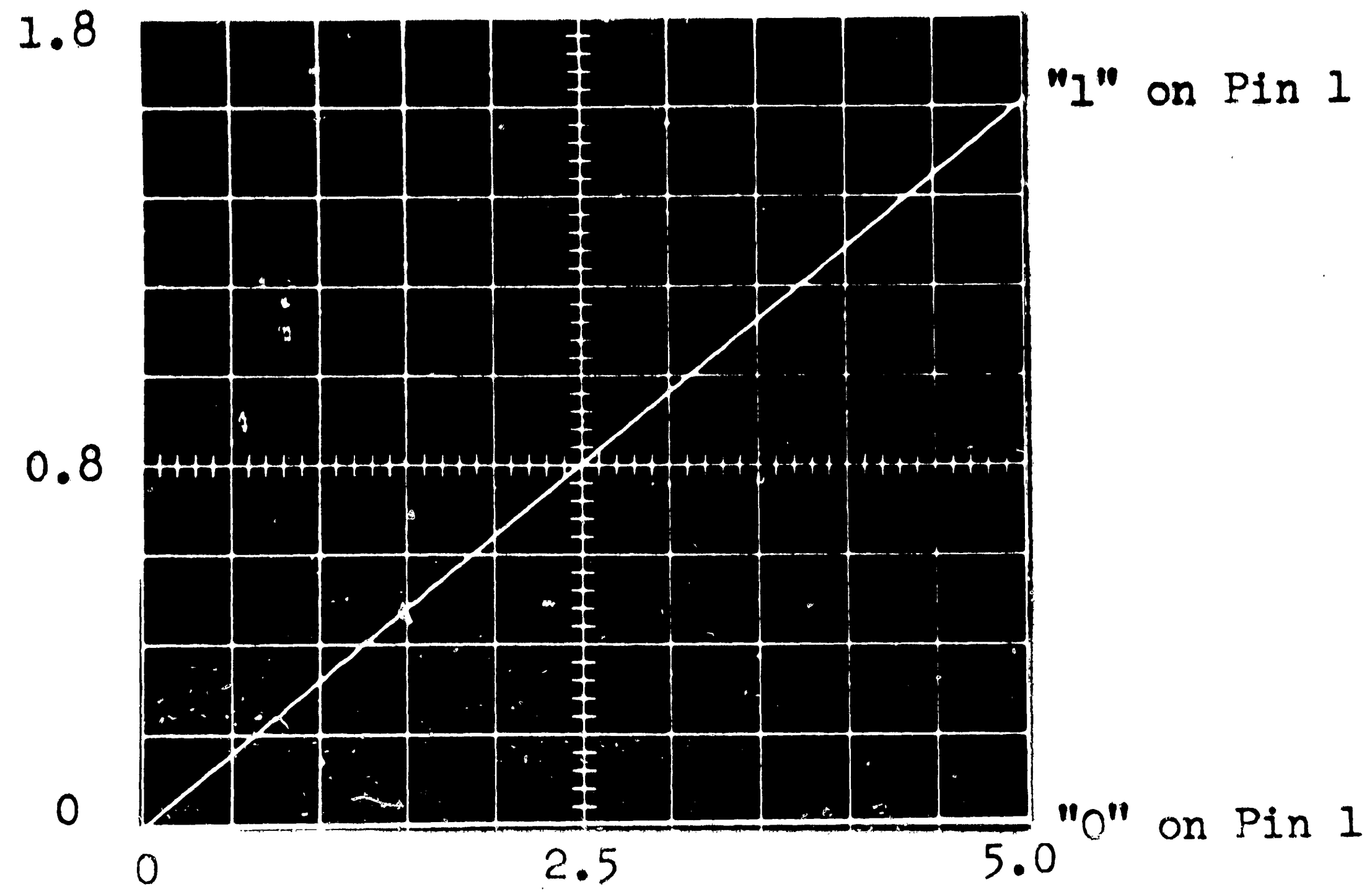
"1" on Pin

0.2 V/div.
Output Voltage on Pin 7

OUTPUT CHARACTERISTICS
DCTL D₂ ELEMENT

3.2.36

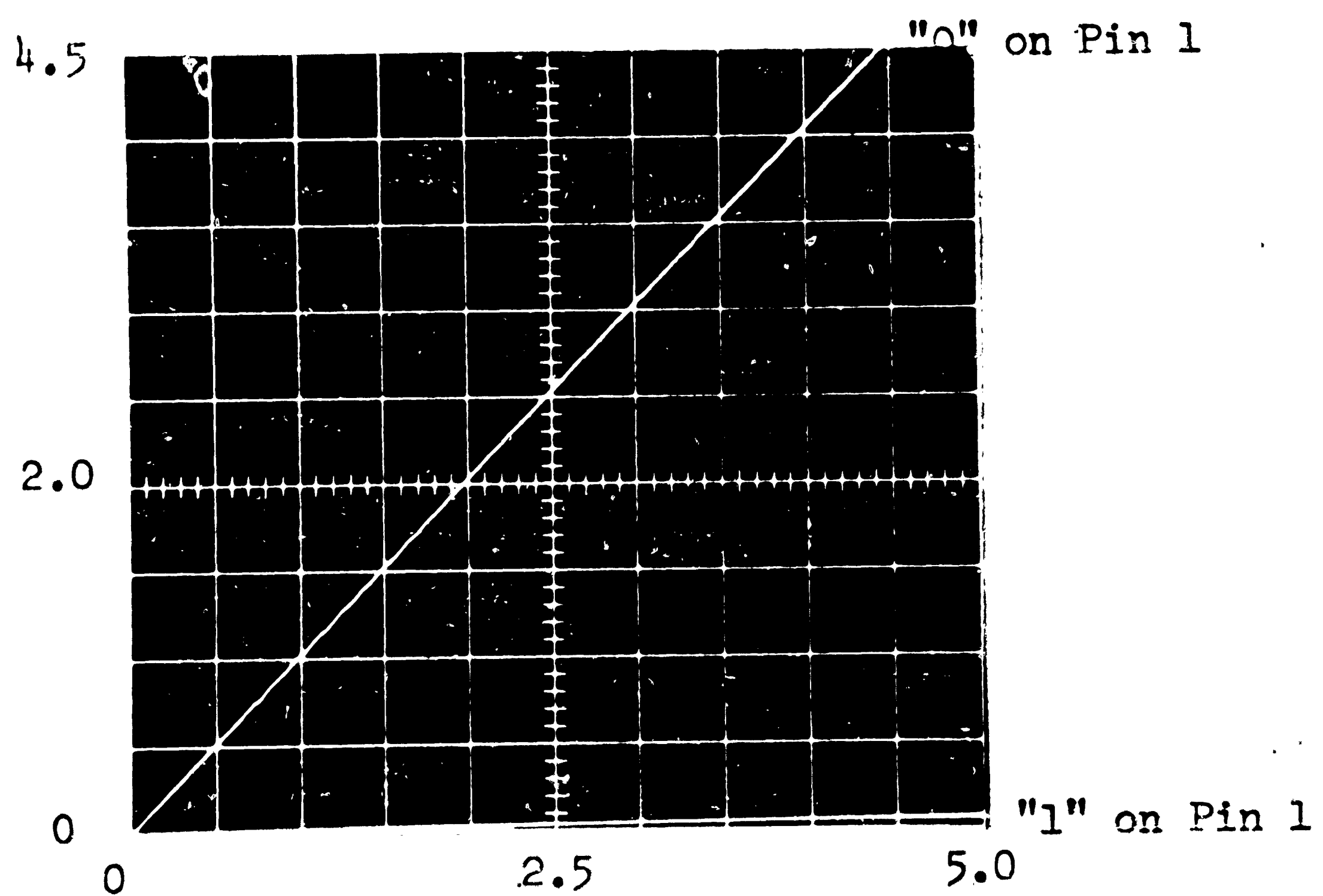
Current into Pin 8
0.2 ma/div.



0.5 V/div.
Supply Voltage on Pin 8

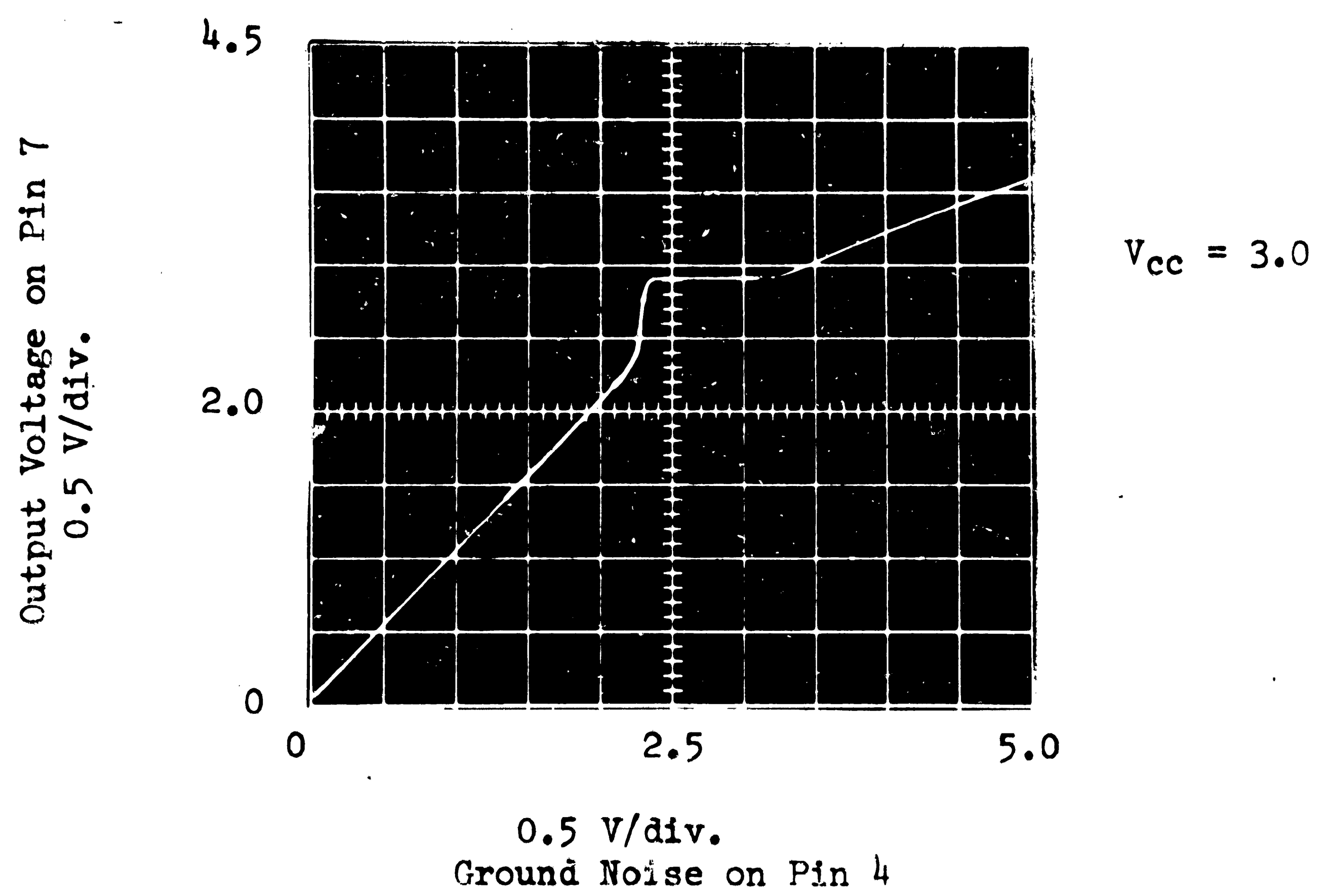
POWER DISSIPATION

Output Voltage on Pin 7
0.5 V/div.

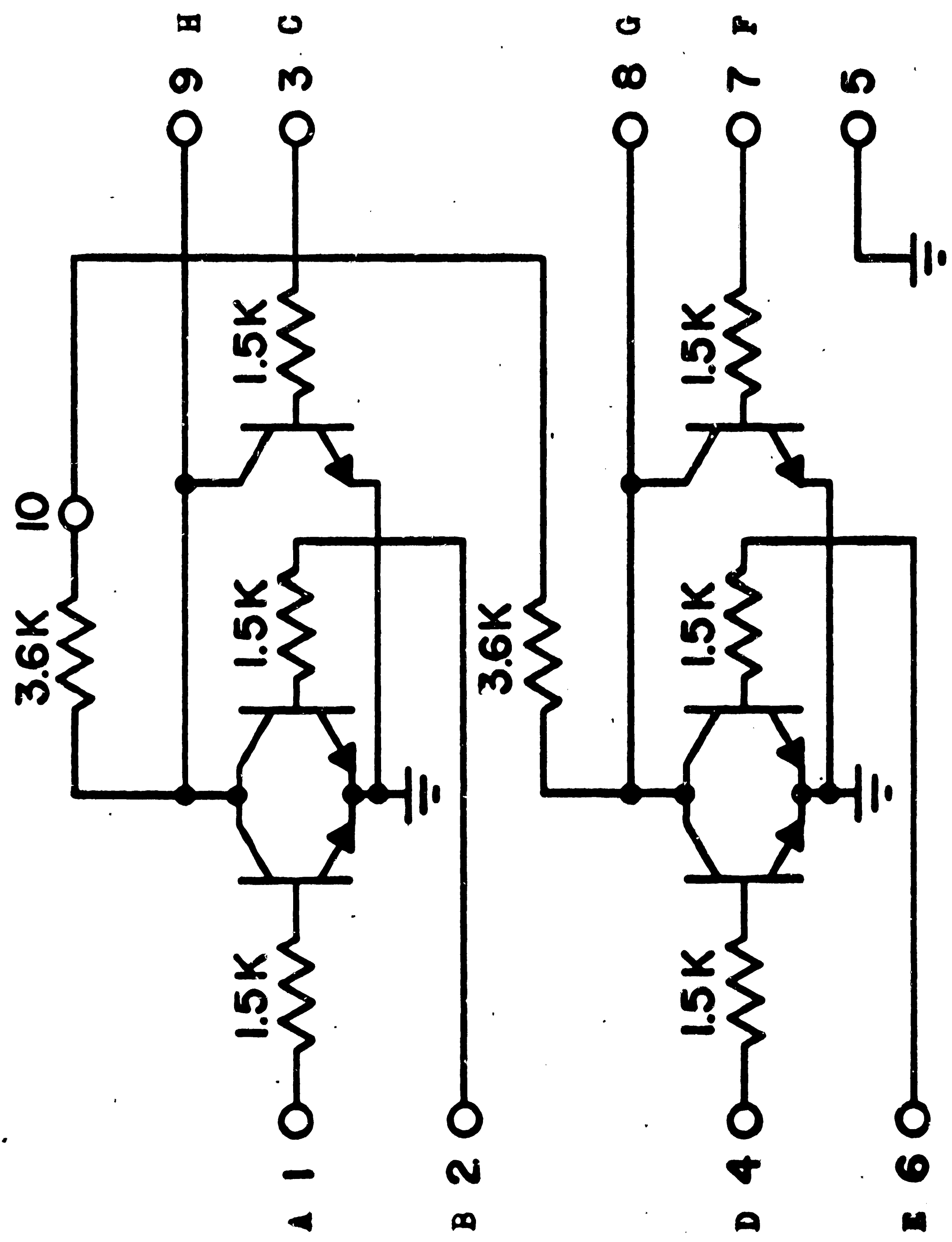


0.5 V/div.
Supply Voltage on Pin 8

OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DCTL D₂ ELEMENT



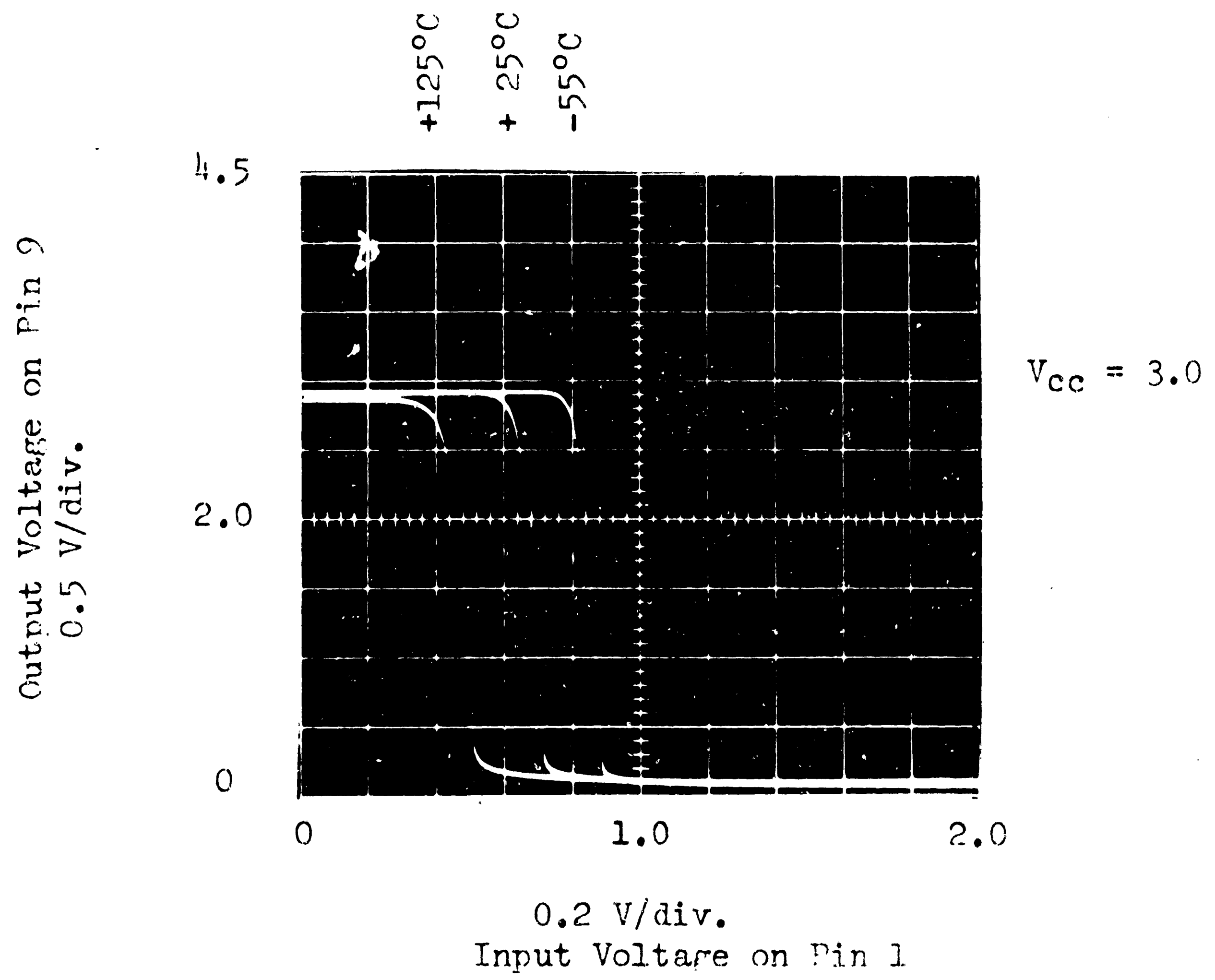
OUTPUT VOLTAGE versus NOISE VOLTAGE
DCTL D₂ ELEMENT



$$H = \overline{A+B+C}$$

$$G = \overline{D+E+F}$$

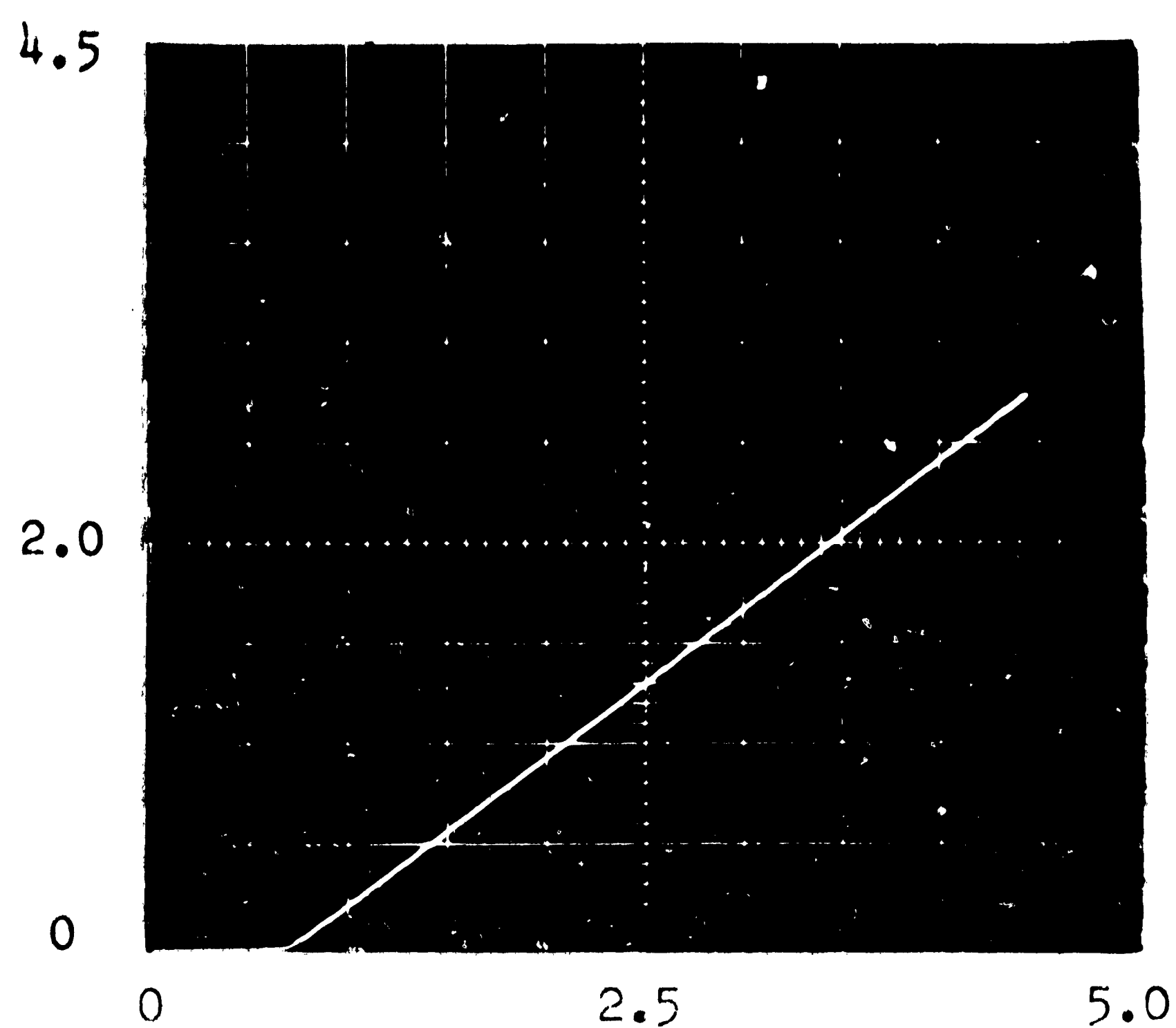
DUAL 3 - INPUT DCTL GATE, D3



INPUT OUTPUT CHARACTERISTICS
DCTL D₃ ELEMENT

3.2.40

Input current into Pin 1
0.5 ma/div.

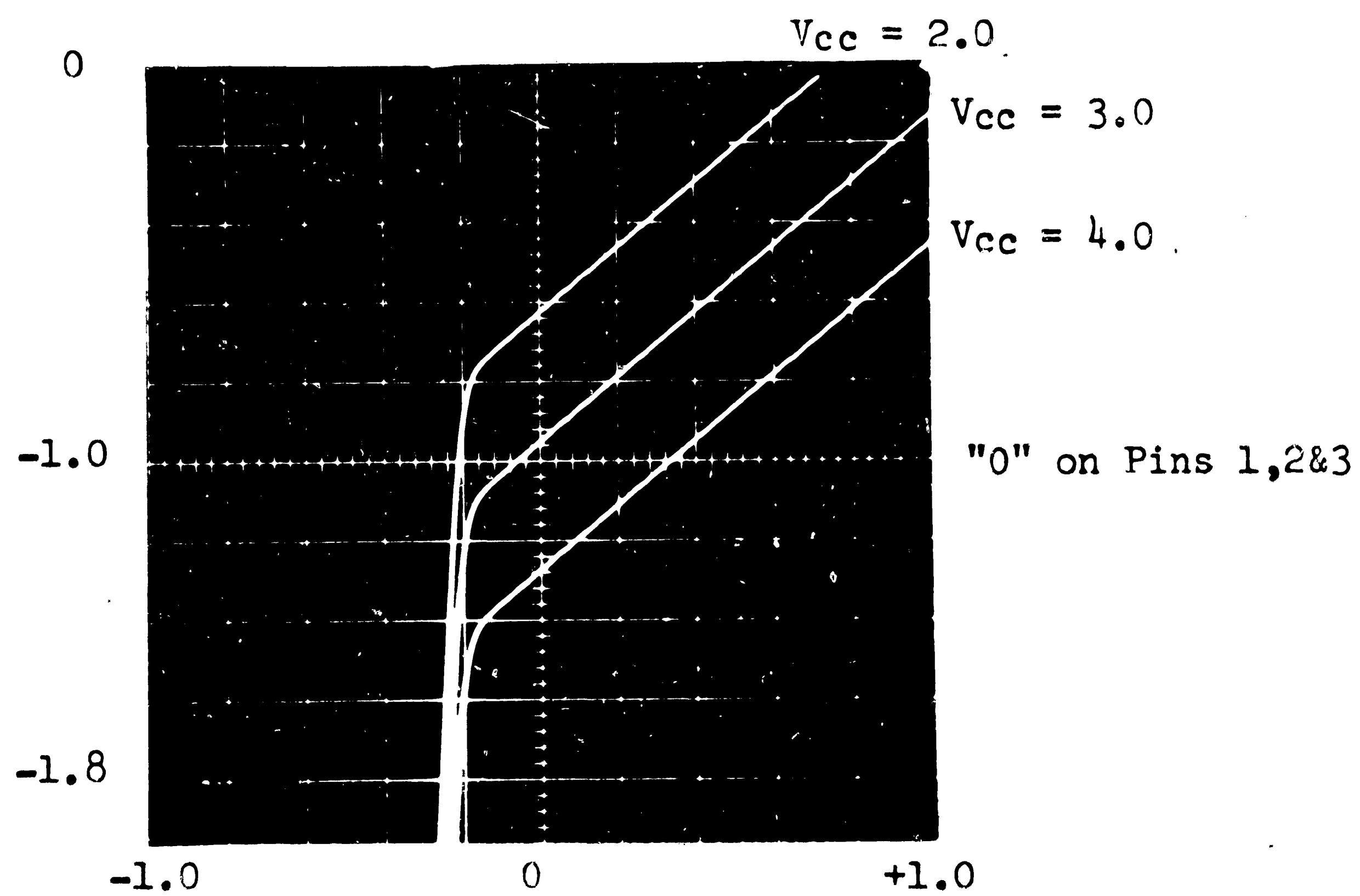


$V_{cc} = 3.0$

0.5 V/div.
Input Voltage on Pin 1

INPUT CHARACTERISTICS

Output Current into Pin 9
0.2 ma/div.



$V_{cc} = 2.0$

$V_{cc} = 3.0$

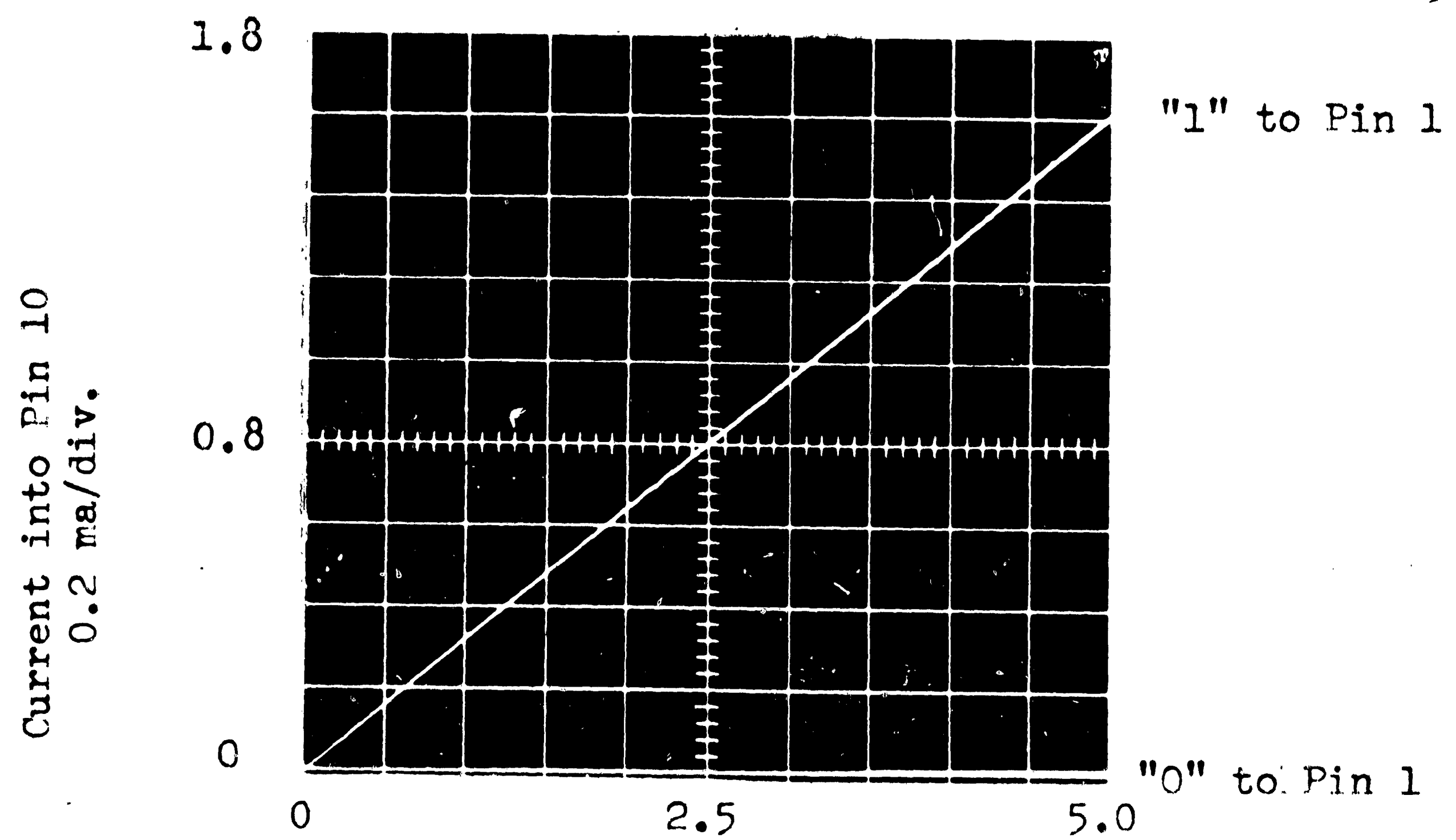
$V_{cc} = 4.0$

"0" on Pins 1,2&3

0.5 V/div.
Output Voltage on Pin 9

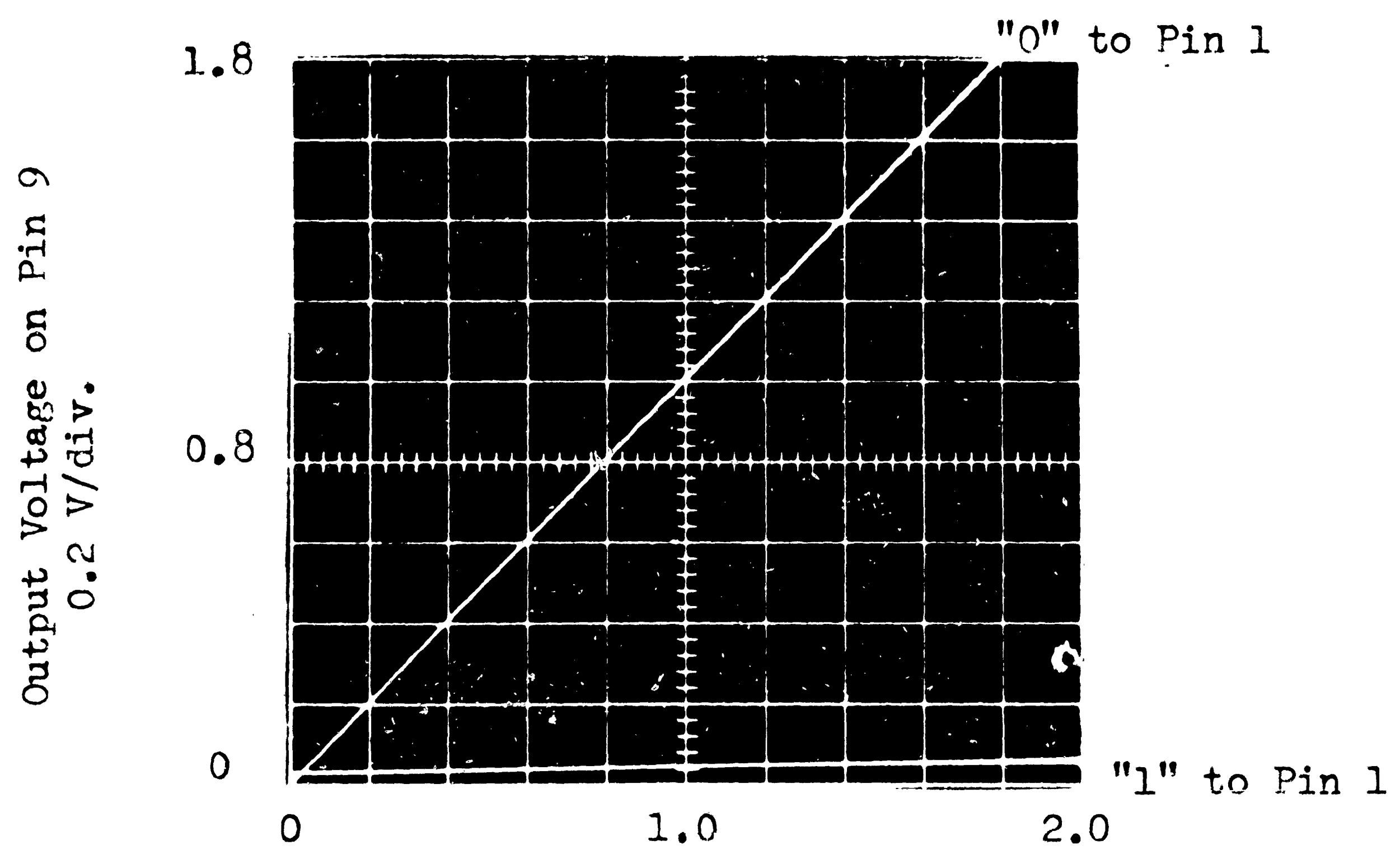
OUTPUT CHARACTERISTICS
DCTL D₃ ELEMENT

3.2.41



0.5 V/div.
Supply Voltage on Pin 10

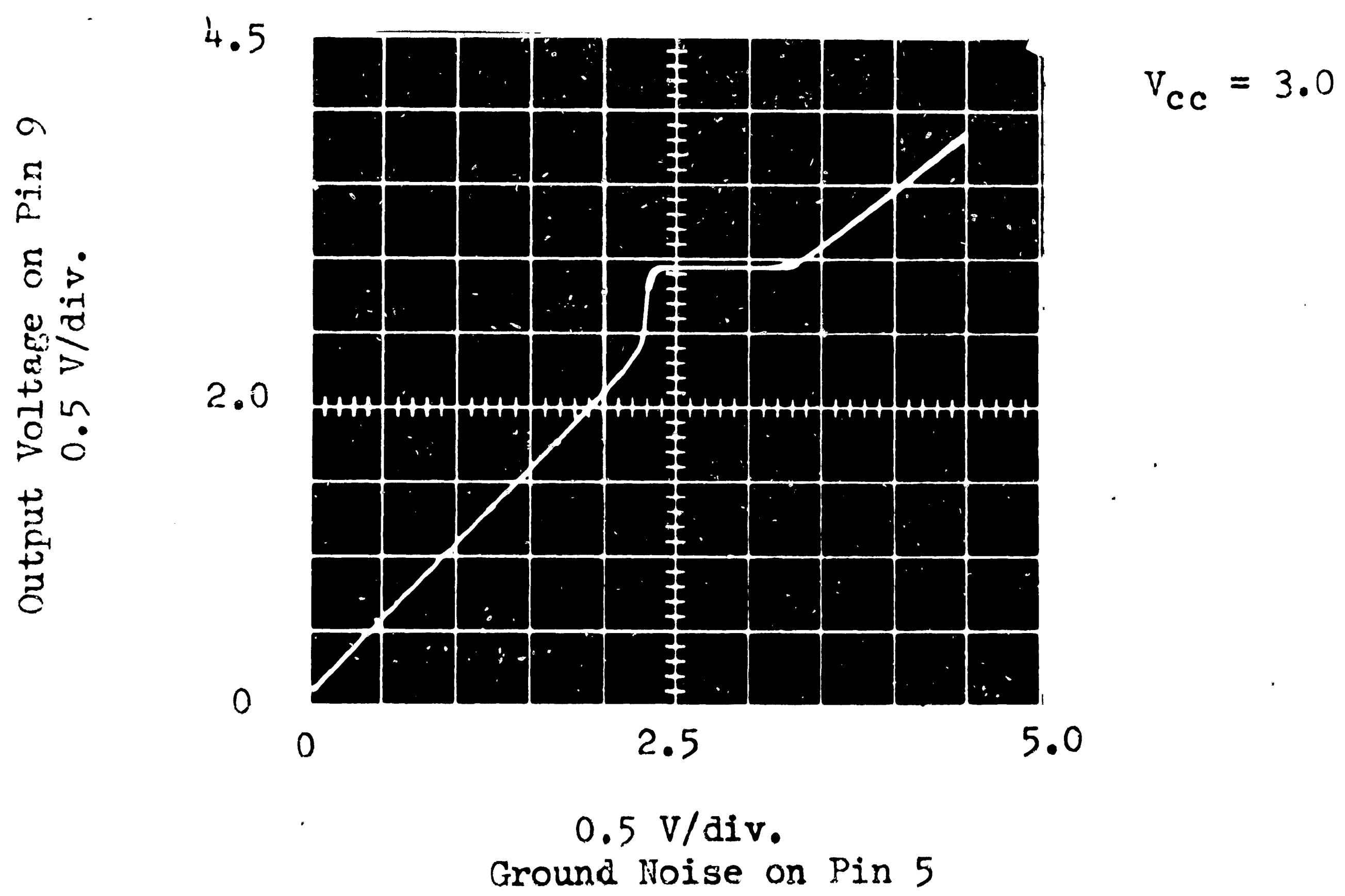
POWER DISSIPATION



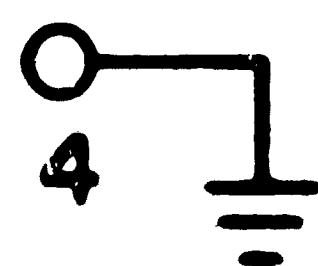
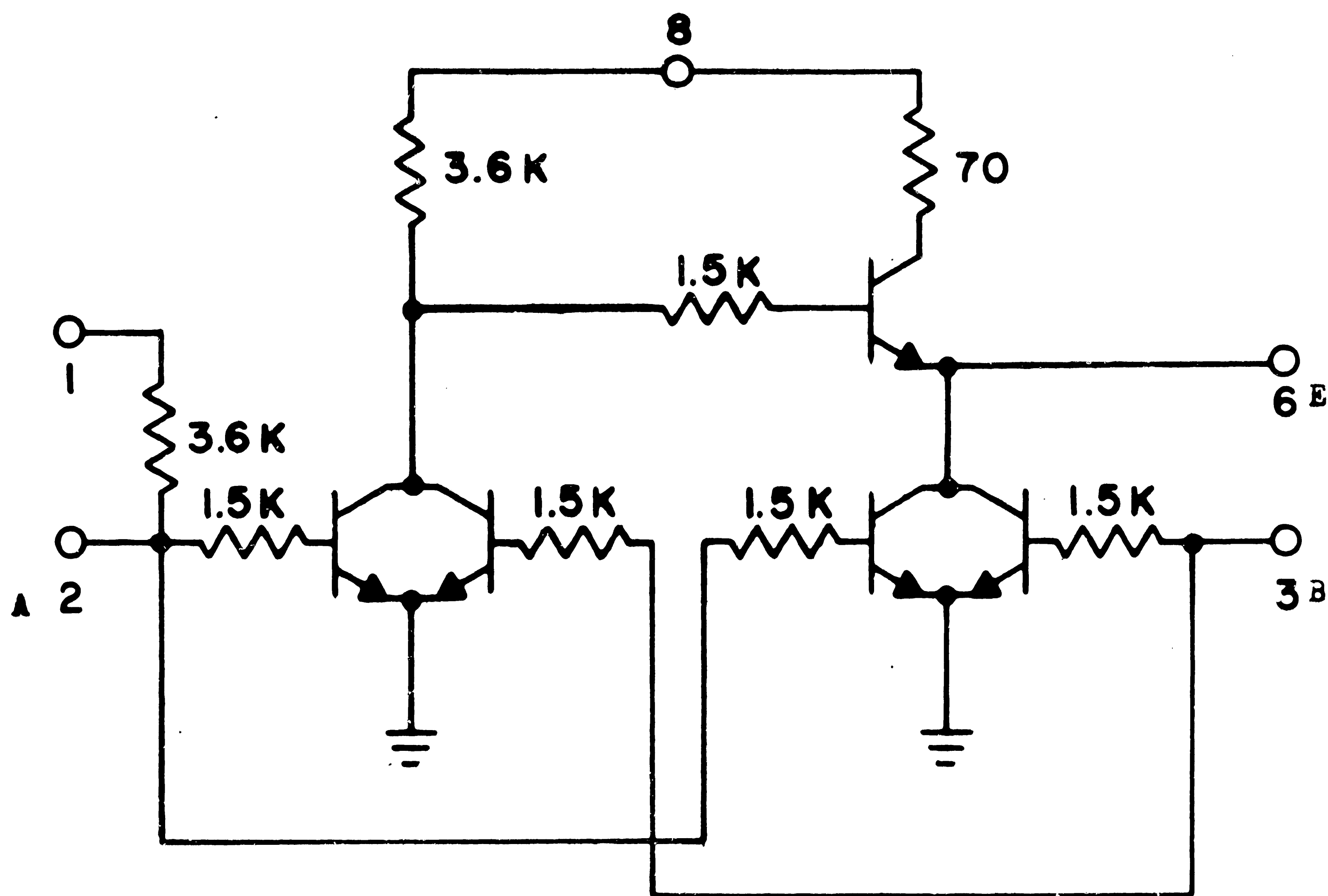
0.2 V/div.
Supply Voltage on Pin 10

OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DCTL D₃ ELEMENT

3.2.42



OUTPUT VOLTAGE versus GROUND NOISE VOLTAGE
DCTL D₃ ELEMENT

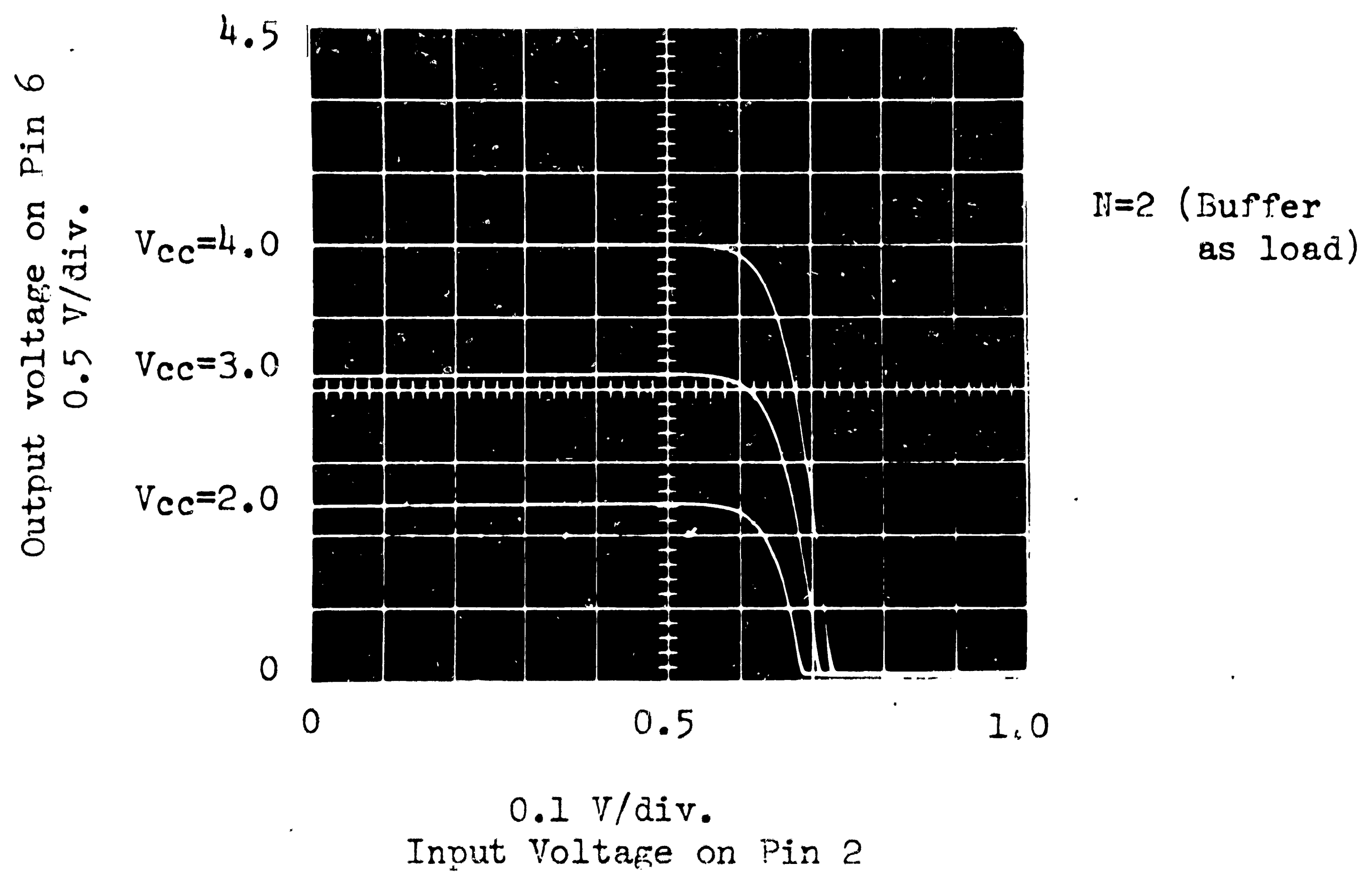


○ NC
5

○ NC
7

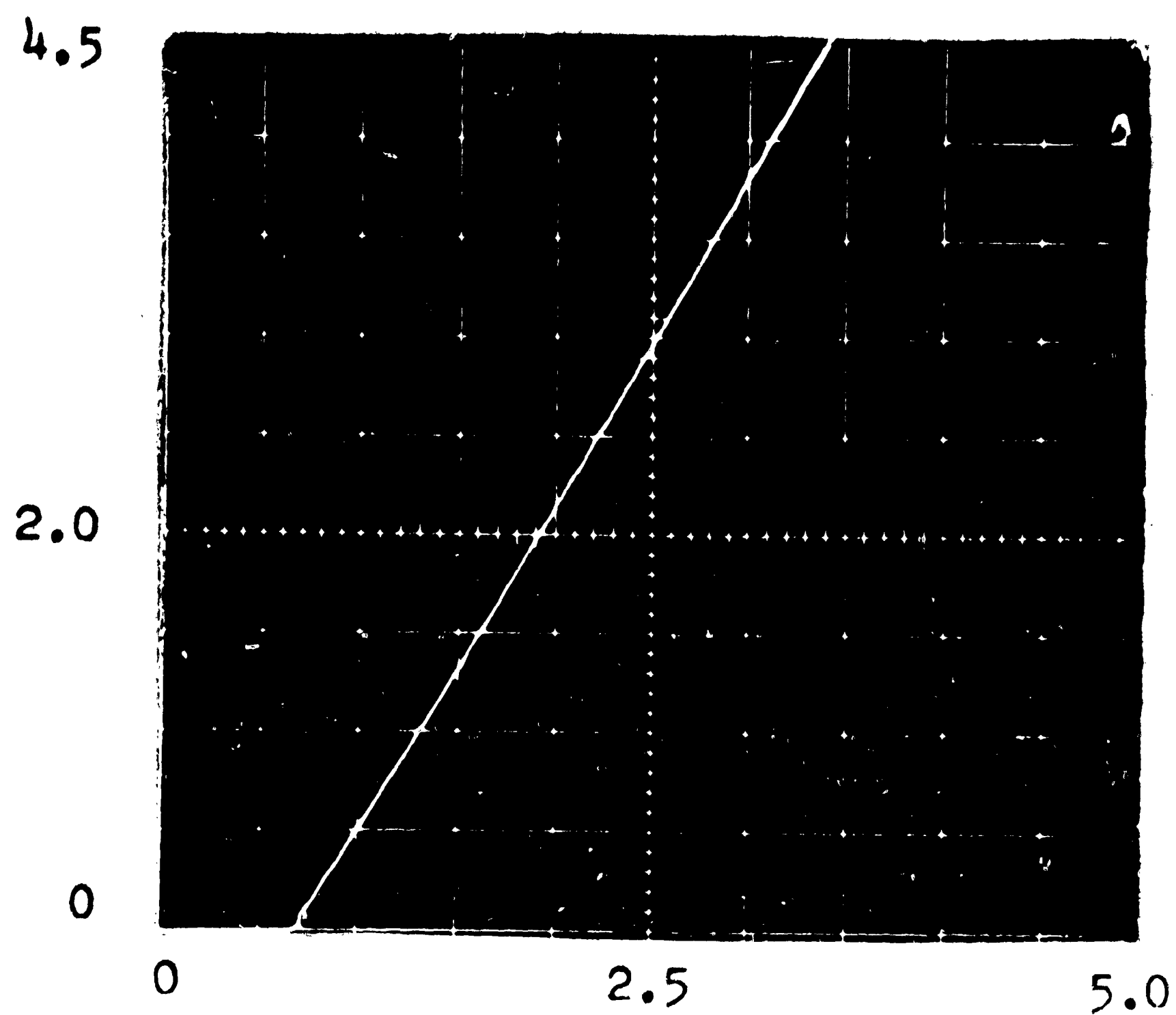
$$E = \overline{A+B} = \overline{A} \overline{B}$$

DCTL BUFFER ELEMENT, B



INPUT OUTPUT CHARACTERISTICS
DCTL B ELEMENT

Input current into pin 2
0.5 ma/div.

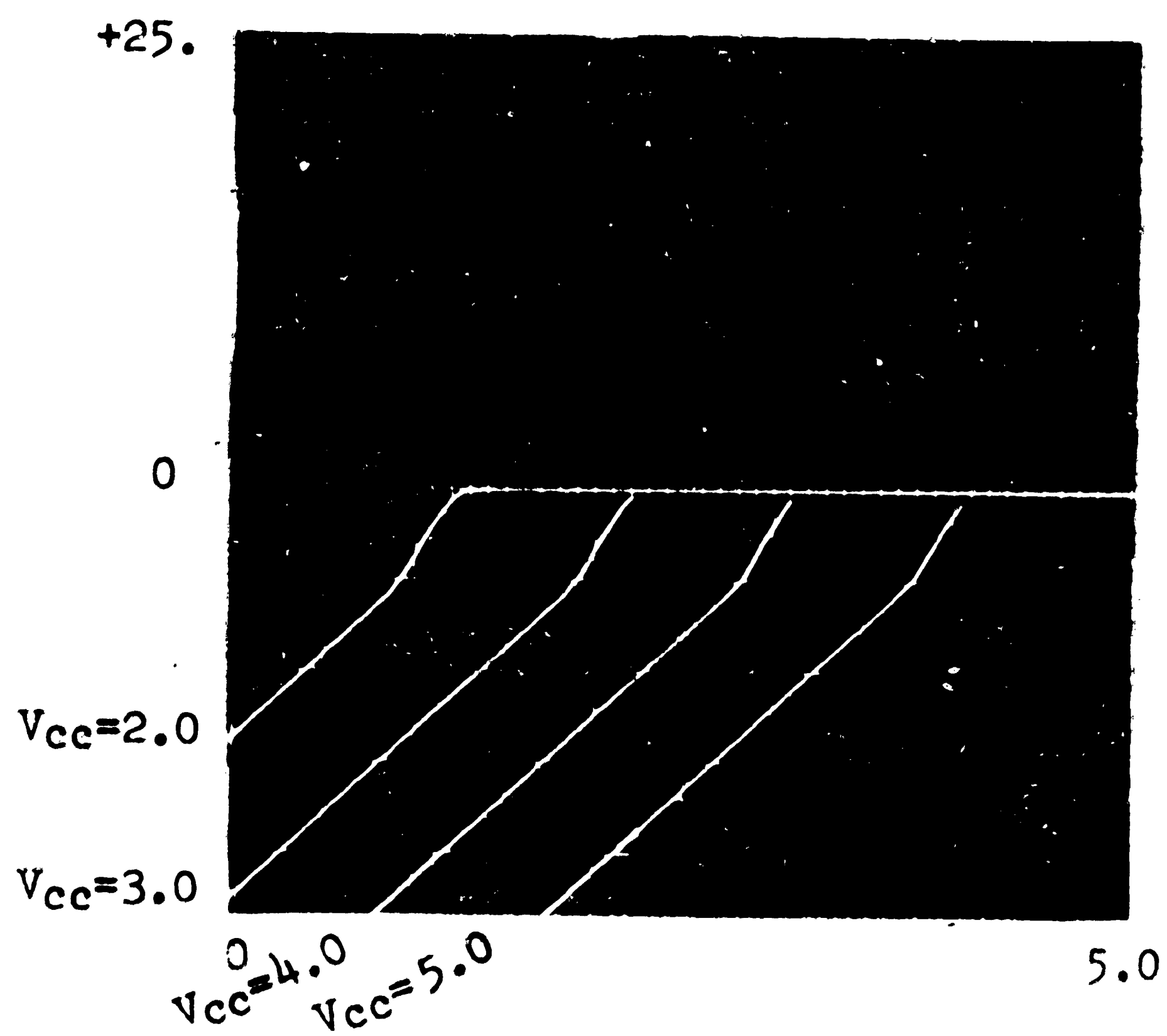


$V_{cc} = 3.0$
 $N = 2$ (Buffer
as Load)

0.5 V/div.
Input Voltage to Pin 2

INPUT CHARACTERISTICS

Output current into Pin 6
5.0 ma/div.

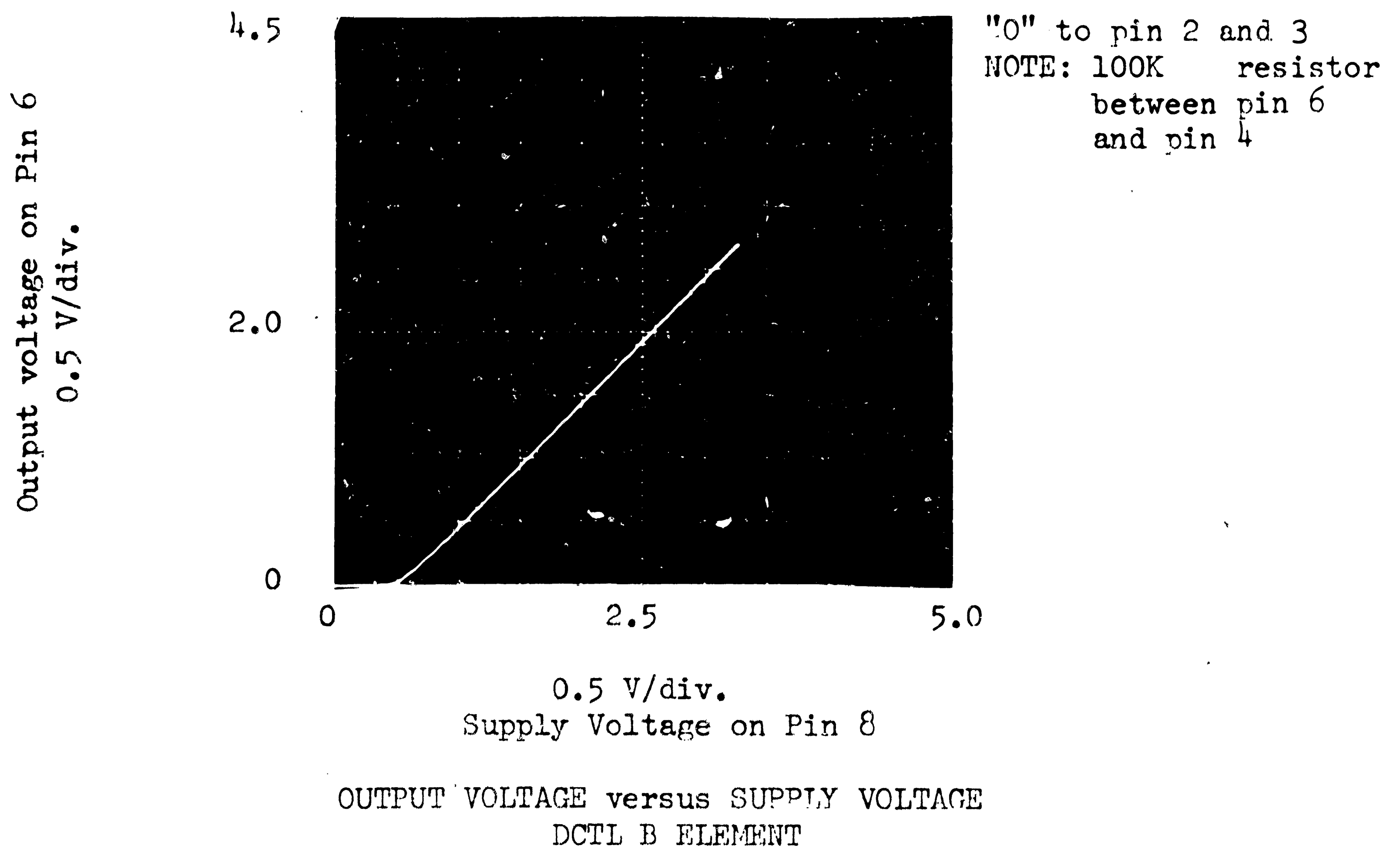
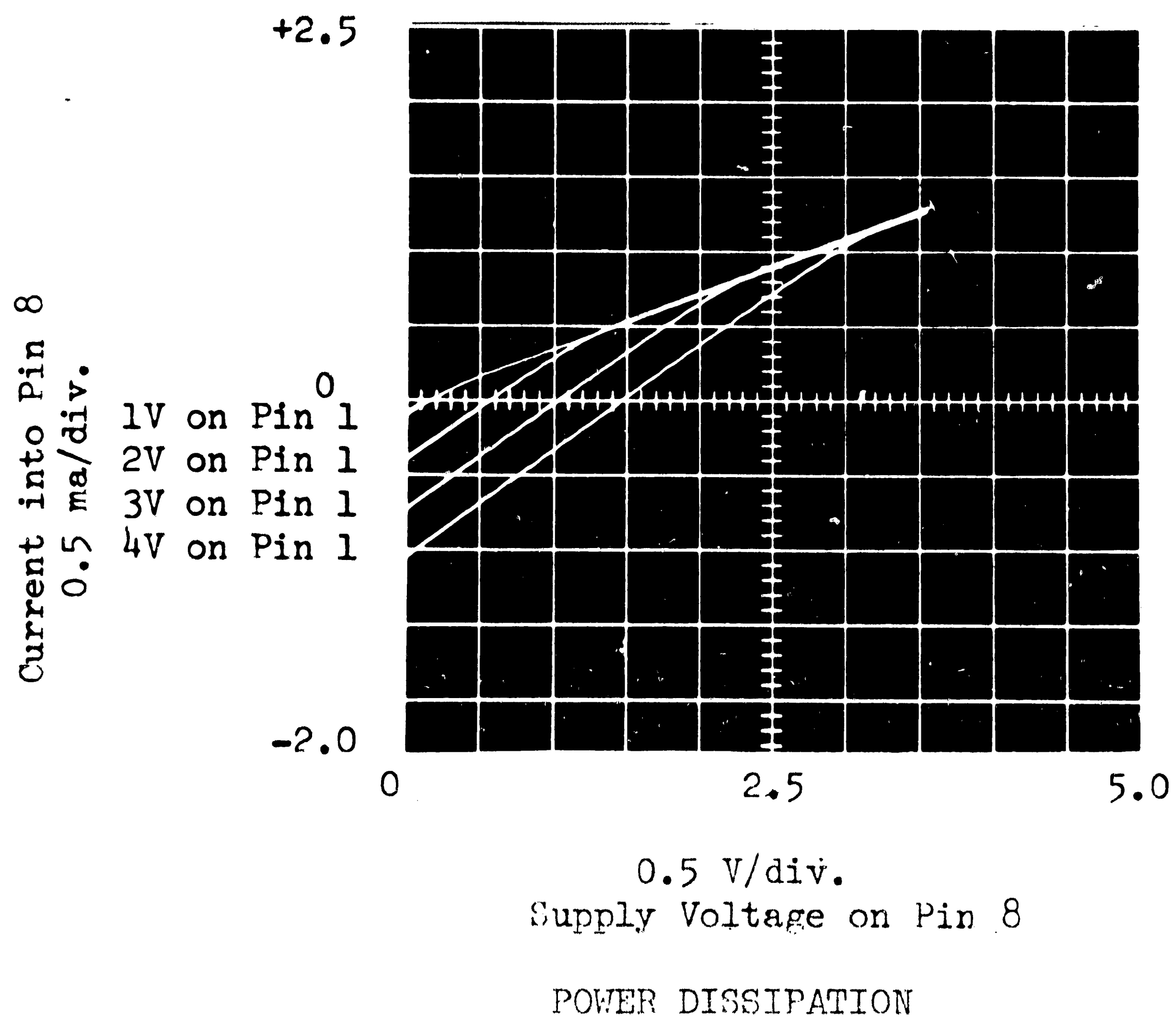


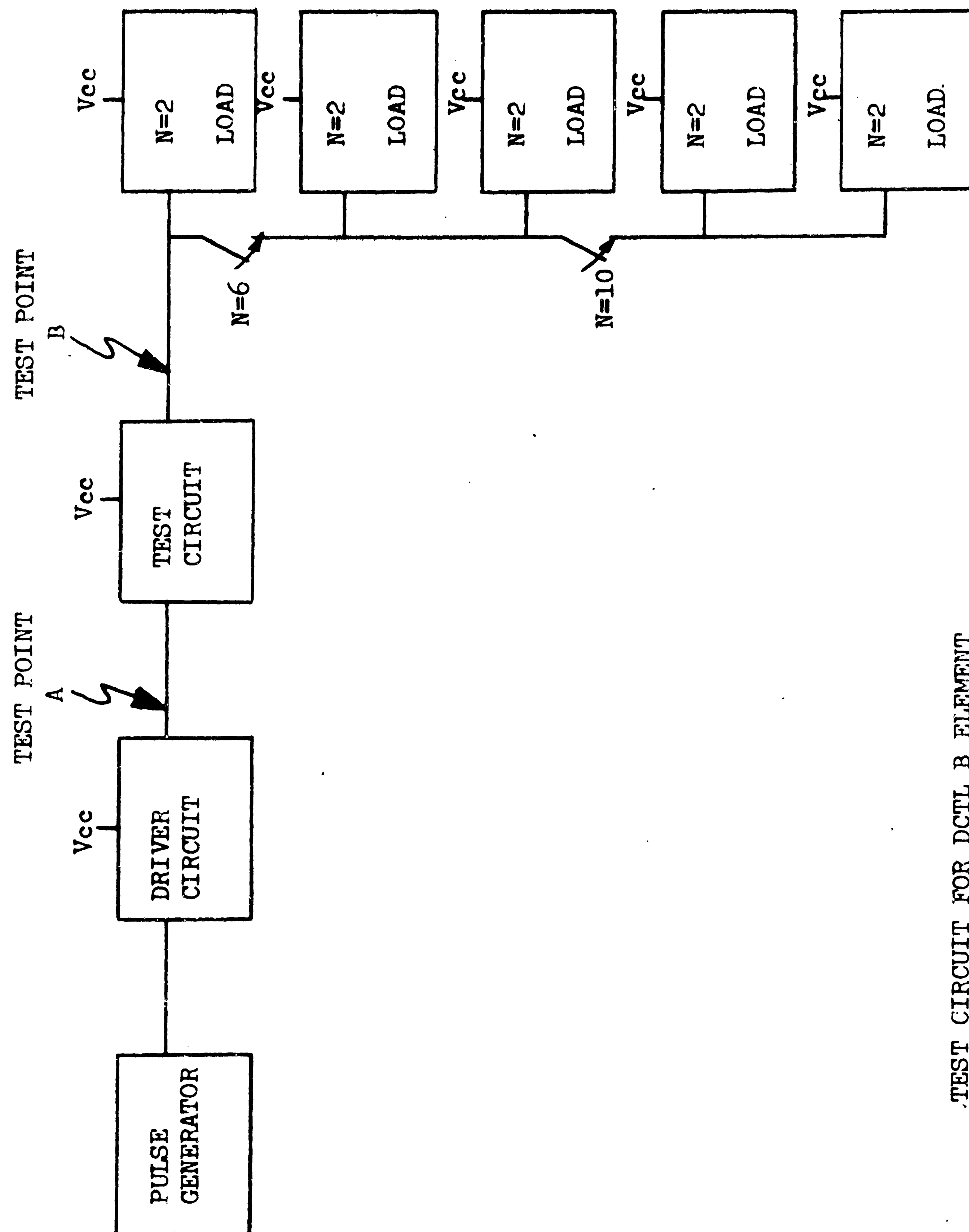
"0" on pin 2 and 3

0.5 V/div.
Output Voltage on Pin 6

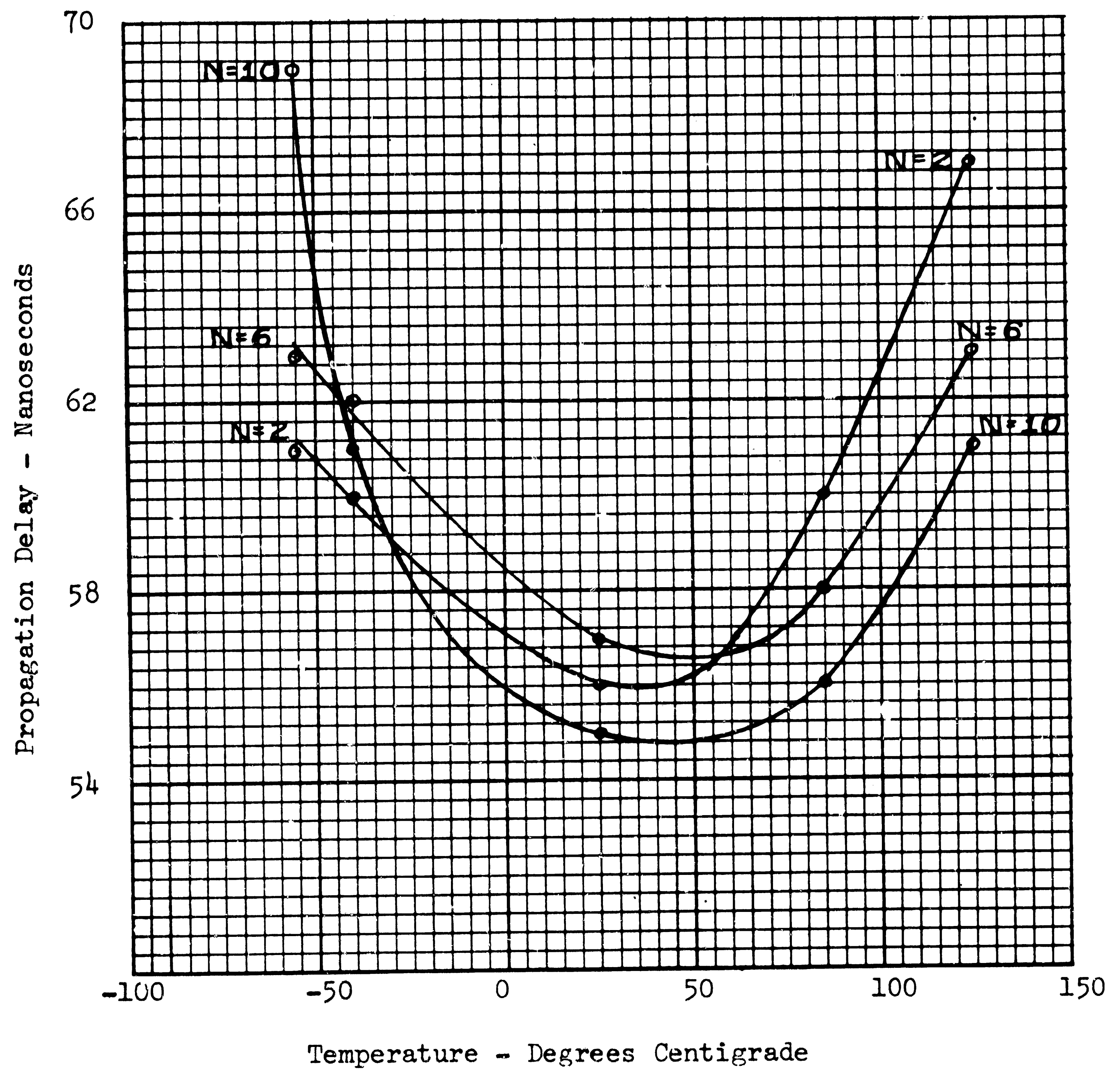
OUTPUT CHARACTERISTICS DCTL B ELEMENT

3.2.46





TEST CIRCUIT FOR DCTL B ELEMENT



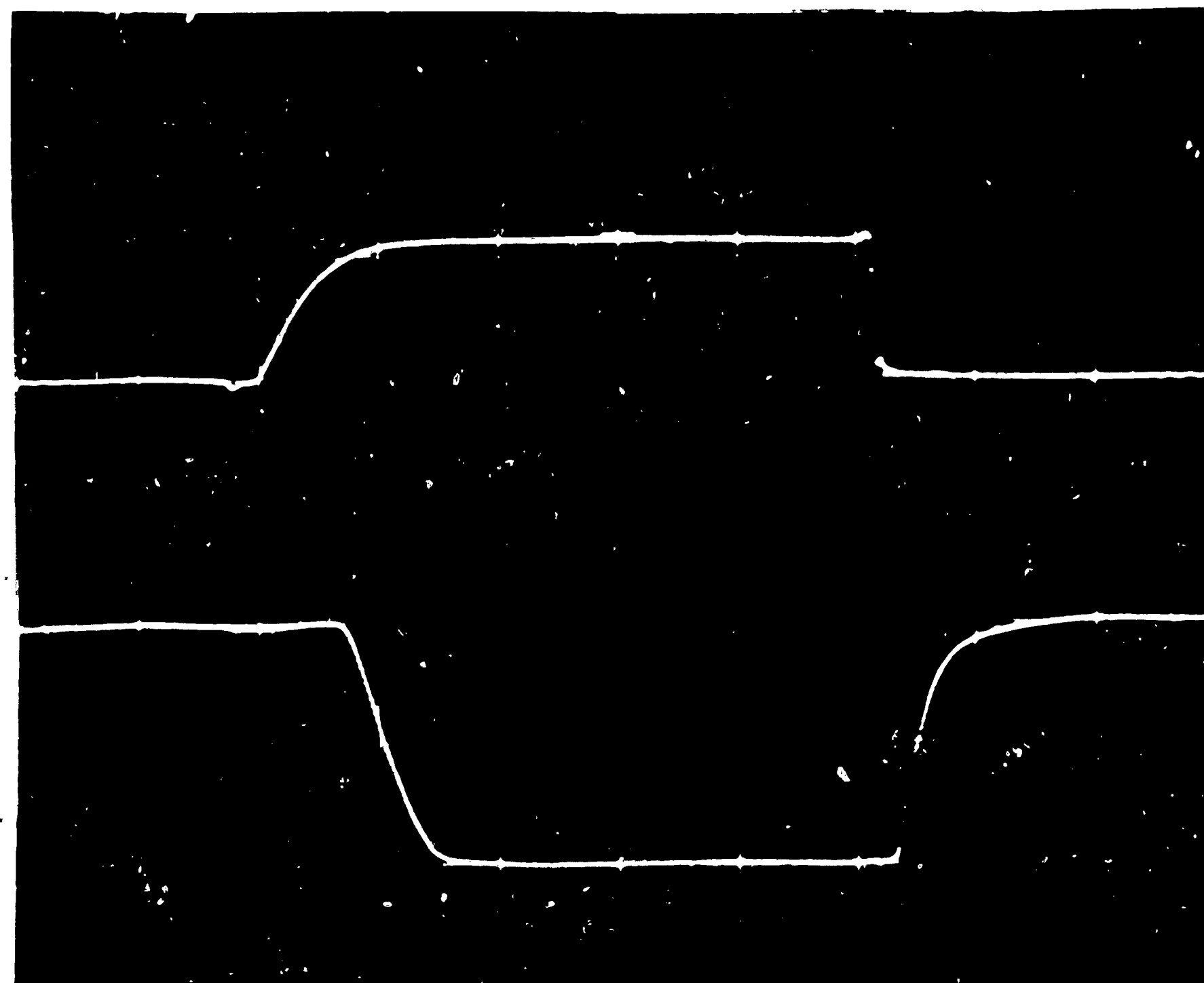
READINGS TAKEN WITH SUPPLY VOLTAGES AT +3.0

DCTL B ELEMENT

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +25°C Vcc 3.0 N = 2

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>469.</u>	<u>462.</u>	<u>458.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.20</u>	<u>1.12</u>	<u>2.06</u>	<u>3.0</u>
T_r	<u>71.</u>	<u>48.</u>	<u>58.</u>	<u>64.</u>
T_f	<u>11.</u>	<u>46.</u>	<u>60.</u>	<u>76.</u>
T_d		<u>75.</u>	<u>75.</u>	<u>76.</u>
T_s		<u>28.</u>	<u>23.</u>	<u>21.</u>
T_{pd}		<u>55.</u>	<u>56.</u>	<u>62.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. -40°C Vcc 3.0 N = 2

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>456.</u>	<u>446.</u>	<u>438.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.27</u>	<u>1.02</u>	<u>1.88</u>	<u>2.79</u>
T _r	<u>74.</u>	<u>42.</u>	<u>45.</u>	<u>49.</u>
T _f	<u>11.</u>	<u>50.</u>	<u>67.</u>	<u>89.</u>
T _d		<u>85.</u>	<u>85.</u>	<u>88.</u>
T _s		<u>28.</u>	<u>23.</u>	<u>21.</u>
T _{pd}		<u>61.</u>	<u>60.</u>	<u>65</u>

Type RTL No. B Temp. -55°C Vcc 3.0 N = 2

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>451.</u>	<u>440.</u>	<u>430.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.28</u>	<u>0.97</u>	<u>1.85</u>	<u>2.74</u>
T _r	<u>76.</u>	<u>41.</u>	<u>45.</u>	<u>48.</u>
T _f	<u>11.</u>	<u>52.</u>	<u>71.</u>	<u>96.</u>
T _d		<u>89.</u>	<u>88.</u>	<u>90.</u>
T _s		<u>29.</u>	<u>24.</u>	<u>19.</u>
T _{pd}		<u>64.</u>	<u>61.</u>	<u>66.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +85 Vcc 3.0 N = 2

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc <u>2.0</u> Vcc <u>3.0</u> Vcc <u>4.0</u>		
Pulse Width	<u>500.</u>	<u>476.</u>	<u>472.</u>	<u>468.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.11</u>	<u>1.20</u>	<u>2.08</u>	<u>2.98</u>
T _r	<u>77.</u>	<u>54.</u>	<u>63.</u>	<u>68.</u>
T _f	<u>11.</u>	<u>46.</u>	<u>57.</u>	<u>71.</u>
T _d		<u>73.</u>	<u>74.</u>	<u>75.</u>
T _s		<u>30.</u>	<u>26.</u>	<u>24.</u>
T _{pd}		<u>55.</u>	<u>60.</u>	<u>65.</u>

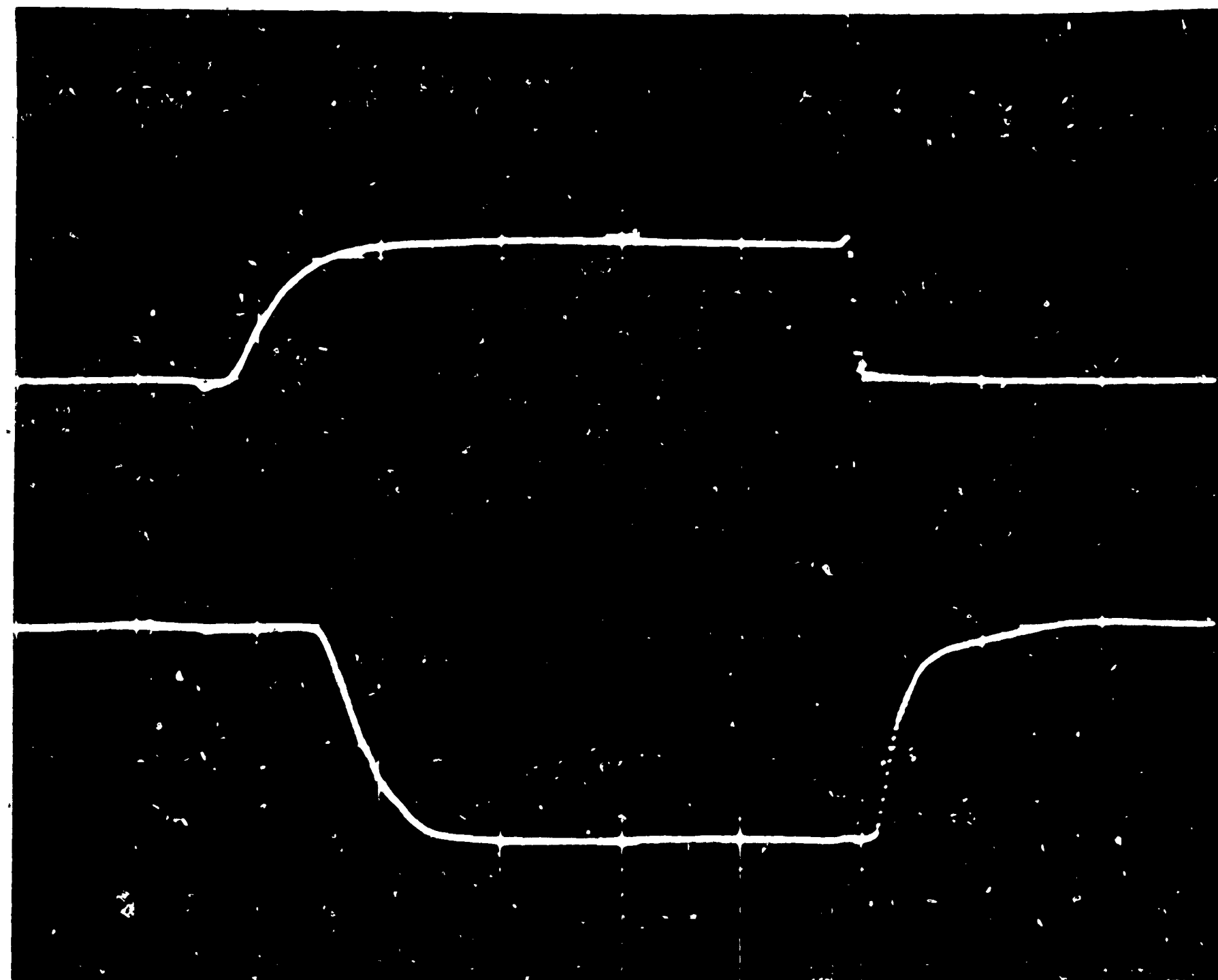
Type RTL No. B Temp. +125°C Vcc 3.0 N = 2

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc <u>2.0</u> Vcc <u>3.0</u> Vcc <u>4.0</u>		
Pulse Width	<u>500.</u>	<u>477.</u>	<u>477.</u>	<u>475.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.03</u>	<u>1.24</u>	<u>2.22</u>	<u>3.11</u>
T _r	<u>83.</u>	<u>69.</u>	<u>84.</u>	<u>90.</u>
T _f	<u>11.</u>	<u>54.</u>	<u>71.</u>	<u>86.</u>
T _d		<u>75.</u>	<u>73.</u>	<u>74.</u>
T _s		<u>31.</u>	<u>27.</u>	<u>25.</u>
T _{pd}		<u>60.</u>	<u>67.</u>	<u>73.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +25°C Vcc 3.0 N = 6 . .

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>467.</u>	<u>459.</u>	<u>453.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.19</u>	<u>1.06</u>	<u>1.82</u>	<u>2.52</u>
T _r	<u>74.</u>	<u>54.</u>	<u>68.</u>	<u>61.</u>
T _f	<u>11.</u>	<u>59.</u>	<u>69.</u>	<u>79.</u>
T _d		<u>76.</u>	<u>77.</u>	<u>79.</u>
T _s		<u>29.</u>	<u>24.</u>	<u>22.</u>
T _{pd}		<u>57.</u>	<u>57.</u>	<u>61.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. -40°C Vcc 3.0 N = 6

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>446.</u>	<u>444.</u>	<u>434.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.27</u>	<u>0.93</u>	<u>1.65</u>	<u>2.38</u>
T _r	<u>77.</u>	<u>40.</u>	<u>53.</u>	<u>64.</u>
T _f	<u>11.</u>	<u>68.</u>	<u>82.</u>	<u>98.</u>
T _d		<u>86.</u>	<u>87.</u>	<u>88.</u>
T _s		<u>29.</u>	<u>24.</u>	<u>21.</u>
T _{pd}		<u>67.</u>	<u>62.</u>	<u>65.</u>

Type RTL No. B Temp. -55°C Vcc 3.0 N = 6

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>438.</u>	<u>439.</u>	<u>427.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.30</u>	<u>0.92</u>	<u>1.62</u>	<u>2.35</u>
T _r	<u>77.</u>	<u>41.</u>	<u>50.</u>	<u>60.</u>
T _f	<u>11.</u>	<u>74.</u>	<u>88.</u>	<u>105.</u>
T _d		<u>91.</u>	<u>90.</u>	<u>92.</u>
T _s		<u>30.</u>	<u>24.</u>	<u>19.</u>
T _{pd}		<u>73.</u>	<u>63.</u>	<u>65.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +85°C Vcc 3.0 N = 6

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>476.</u>	<u>469.</u>	<u>464.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.11</u>	<u>1.12</u>	<u>1.84</u>	<u>2.51</u>
T _r	<u>76.</u>	<u>63.</u>	<u>60.</u>	<u>66.</u>
T _f	<u>11.</u>	<u>64.</u>	<u>67.</u>	<u>74.</u>
T _d		<u>72.</u>	<u>74.</u>	<u>75.</u>
T _s		<u>30.</u>	<u>26.</u>	<u>23.</u>
T _{pd}		<u>55.</u>	<u>58.</u>	<u>62.</u>

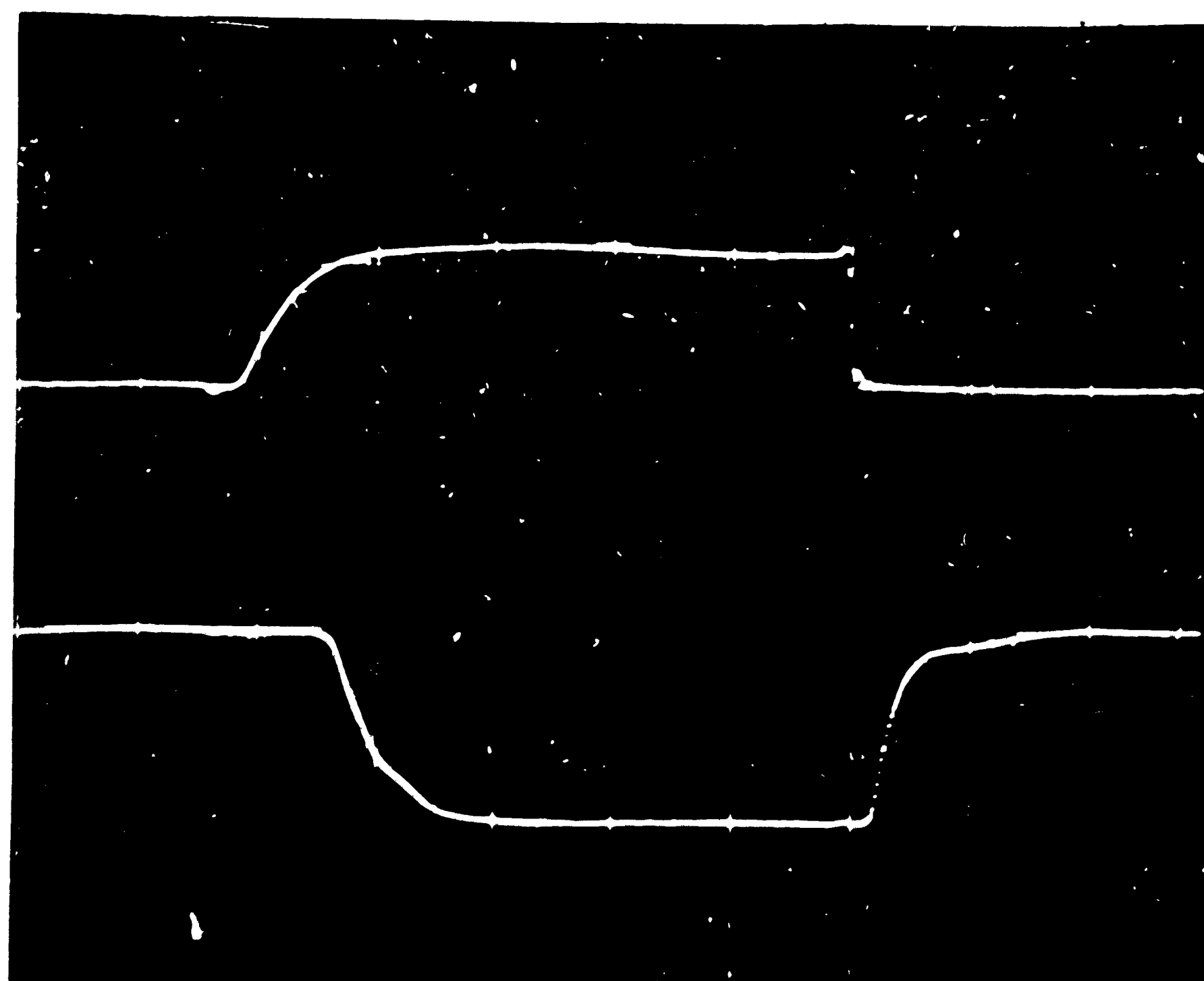
Type RTL No. B Temp. +125°C Vcc 3.0 N = 6

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>478.</u>	<u>473.</u>	<u>469.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.02</u>	<u>1.12</u>	<u>1.78</u>	<u>2.46</u>
T _r	<u>82.</u>	<u>70.</u>	<u>76.</u>	<u>87.</u>
T _f	<u>11.</u>	<u>78.</u>	<u>75.</u>	<u>82.</u>
T _d		<u>74.</u>	<u>75.</u>	<u>75.</u>
T _s		<u>32.</u>	<u>27.</u>	<u>25.</u>
T _{pd}		<u>60.</u>	<u>63.</u>	<u>69.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +25°C Vcc +3.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>464.</u>	<u>458.</u>	<u>451.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.20</u>	<u>0.98</u>	<u>1.64</u>	<u>2.20</u>
T_r	<u>76.</u>	<u>48.</u>	<u>55.</u>	<u>69.</u>
T_f	<u>11.</u>	<u>72.</u>	<u>79.</u>	<u>87.</u>
T_d		<u>77.</u>	<u>78.</u>	<u>79.</u>
T_s		<u>29.</u>	<u>24.</u>	<u>22.</u>
T_{pd}		<u>58.</u>	<u>55.</u>	<u>59.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. -40°C Vcc 3.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>430.</u>	<u>443.</u>	<u>433.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.29</u>	<u>0.86</u>	<u>1.52</u>	<u>212.</u>
T _r	<u>80.</u>	<u>34.</u>	<u>48.</u>	<u>69.</u>
T _f	<u>12.</u>	<u>84.</u>	<u>94.</u>	<u>109.</u>
T _d		<u>88.</u>	<u>86.</u>	<u>87.</u>
T _s		<u>30.</u>	<u>24.</u>	<u>22.</u>
T _{pd}		<u>75.</u>	<u>61.</u>	<u>63.</u>

Type RTL No. B Temp. -55°C Vcc 3.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>419.</u>	<u>438.</u>	<u>426.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.31</u>	<u>0.86</u>	<u>1.47</u>	<u>2.03</u>
T _r	<u>83.</u>	<u>34.</u>	<u>42.</u>	<u>61.</u>
T _f	<u>12.</u>	<u>90.</u>	<u>103.</u>	<u>116.</u>
T _d		<u>92.</u>	<u>92.</u>	<u>92.</u>
T _s		<u>31.</u>	<u>25.</u>	<u>21.</u>
T _{pd}		<u>81.</u>	<u>69.</u>	<u>65.</u>

GENERAL MICRO-ELECTRONICS

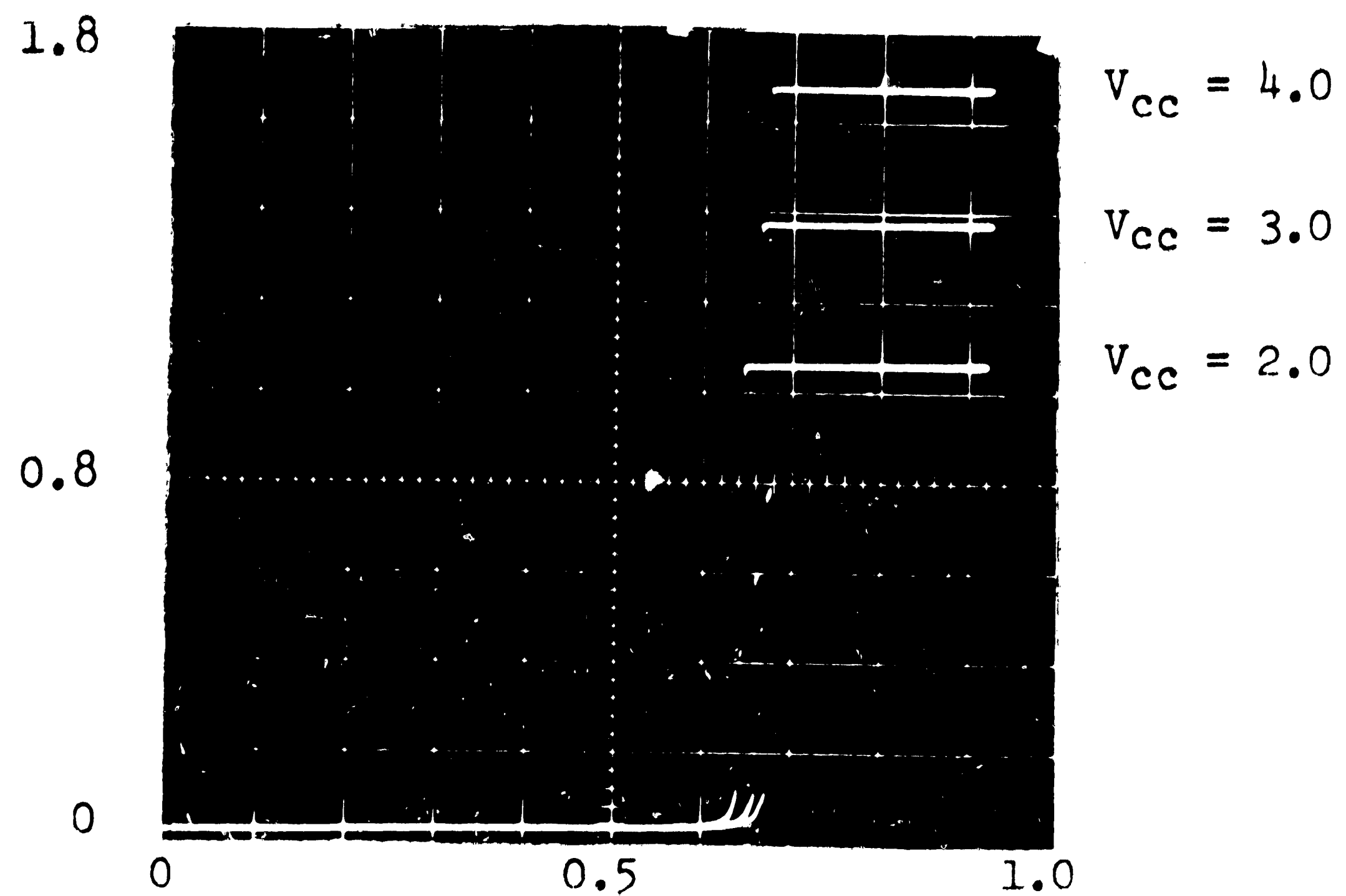
Type RTL No. B Temp. +85°C Vcc 3.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>477.</u>	<u>468.</u>	<u>464.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.10</u>	<u>1.02</u>	<u>1.60</u>	<u>2.15</u>
T_r	<u>80.</u>	<u>54.</u>	<u>65.</u>	<u>90.</u>
T_f	<u>11.</u>	<u>81.</u>	<u>83.</u>	<u>85.</u>
T_d		<u>72.</u>	<u>73.</u>	<u>73.</u>
T_s		<u>31.</u>	<u>26.</u>	<u>23.</u>
T_{pd}		<u>55.</u>	<u>56.</u>	<u>65.</u>

Type RTL No. B Temp. +125°C Vcc 3.0 N = 10

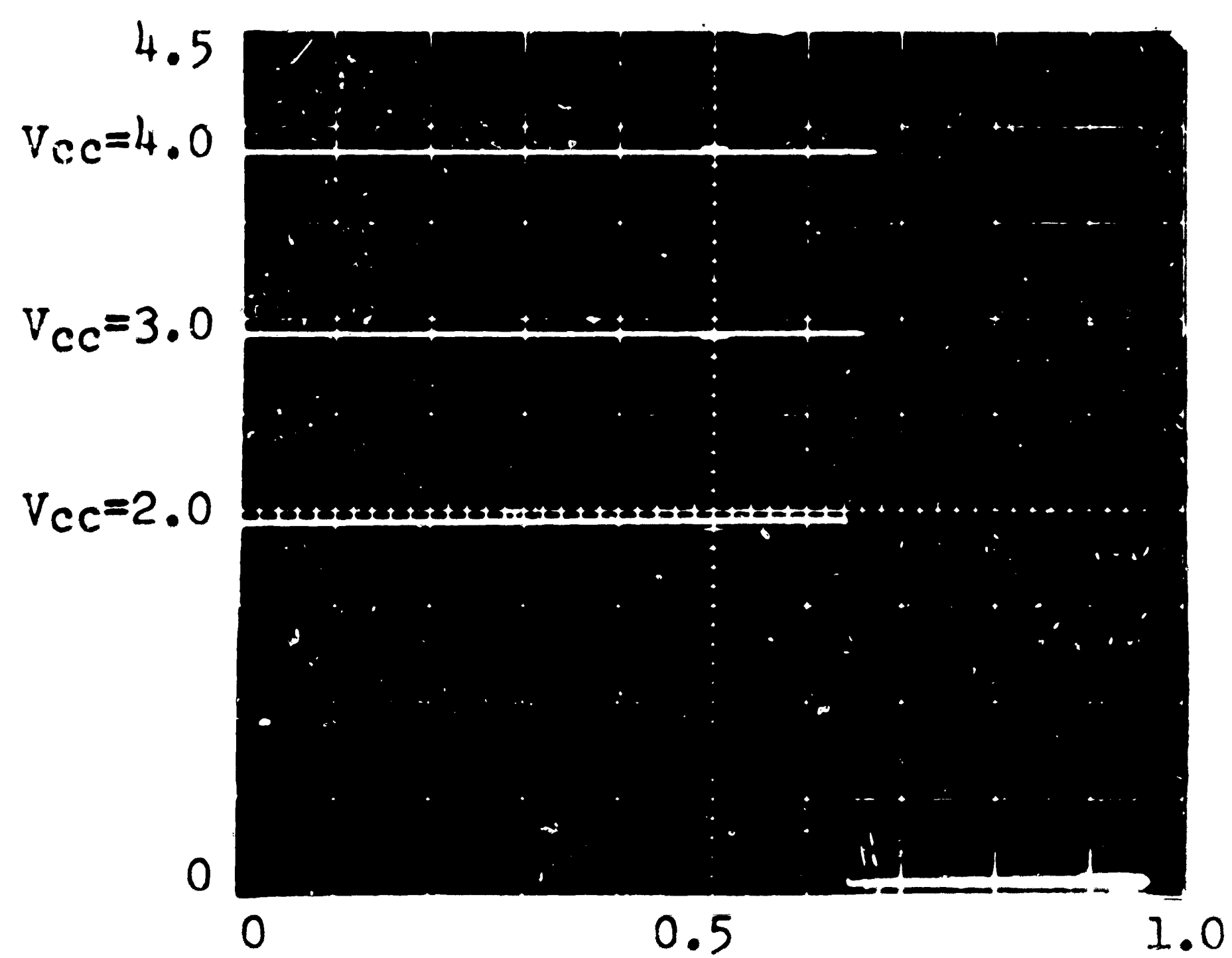
	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>476.</u>	<u>469.</u>	<u>467.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>51.</u>	<u>0.98</u>	<u>1.54</u>	<u>2.10</u>
T_r	<u>87.</u>	<u>61.</u>	<u>82.</u>	<u>102.</u>
T_f	<u>11.</u>	<u>99.</u>	<u>97.</u>	<u>91.</u>
T_d		<u>74.</u>	<u>73.</u>	<u>73.</u>
T_s		<u>32.</u>	<u>27.</u>	<u>25.</u>
T_{pd}		<u>58.</u>	<u>61.</u>	<u>66.</u>

Output voltage on Pin 7
0.2 V/div.



0.1 V/div.
Input Voltage on Pins 1 and 3

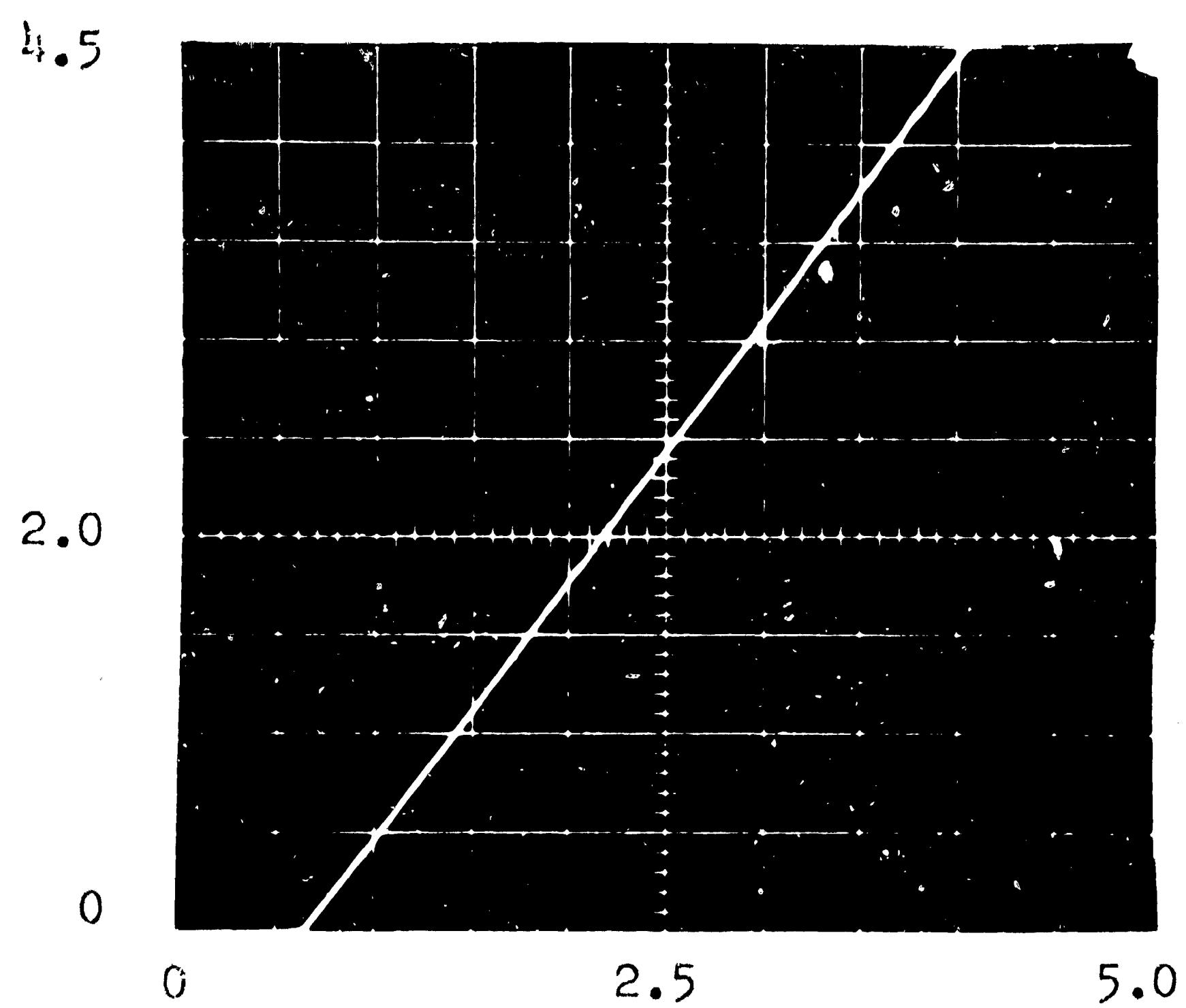
Output Voltage on Pin 6
0.5 V/div.



0.1 V/div.
Input Voltage on Pins 1 and 3

INPUT - OUTPUT CHARACTERISTICS
DCTL H ELEMENT

Input current into Pins 1 and 3
0.5 ma/div.

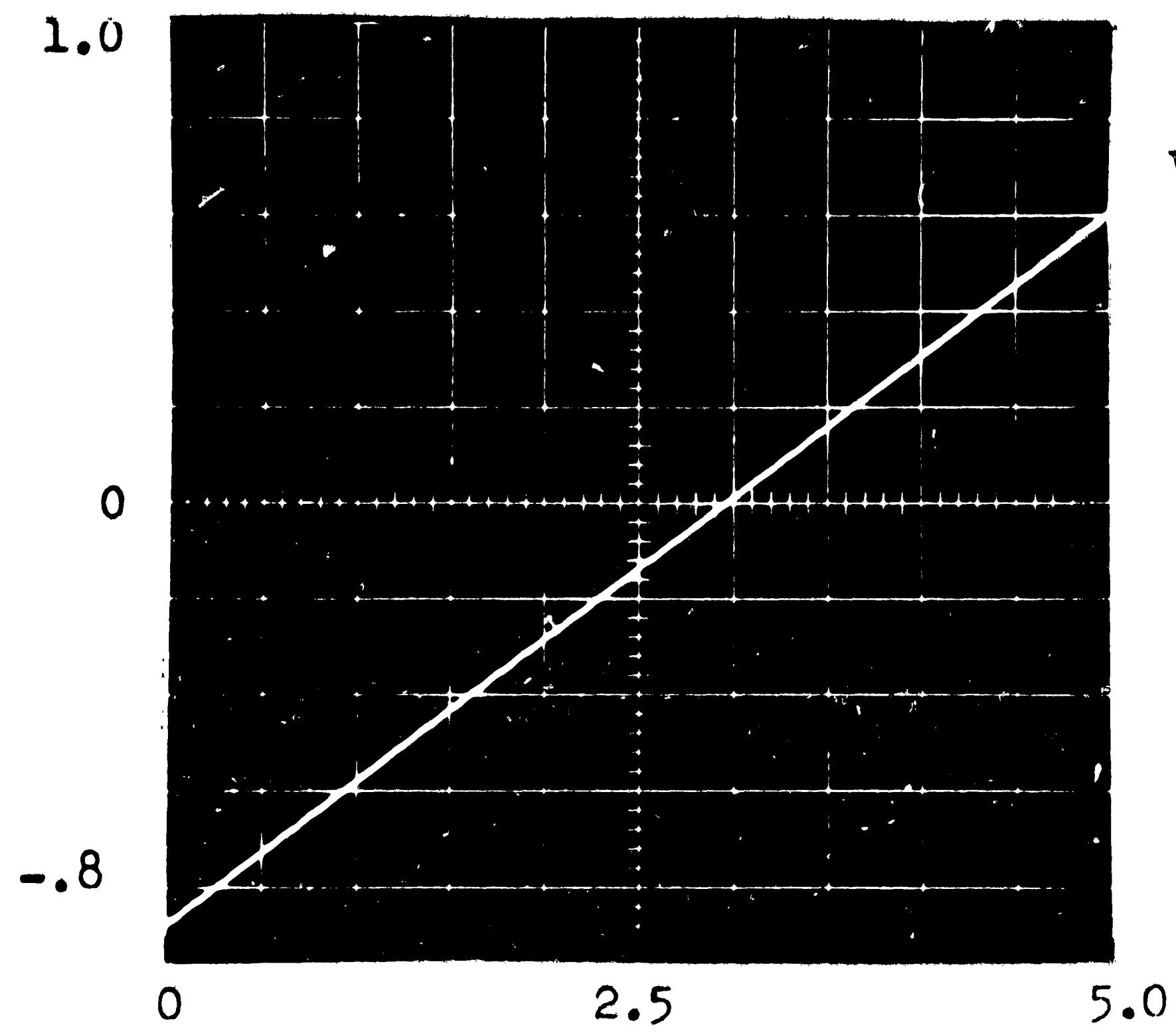


$V_{cc} = 3.0$

0.5 V/div.
Input Voltage to Pins 1 and 3

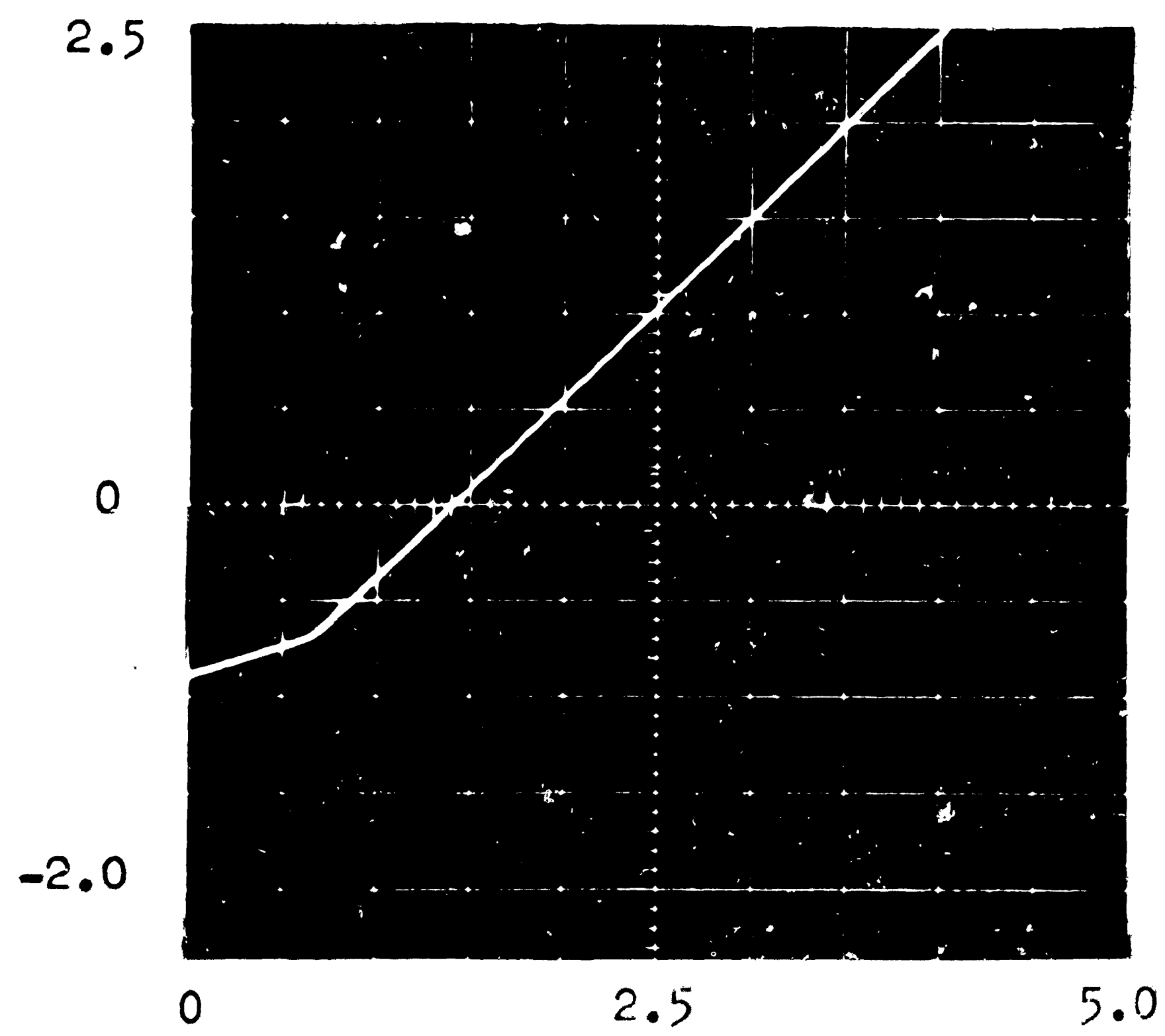
INPUT CHARACTERISTICS
DCTL H ELEMENT

Output current into Pin 6
0.2 ma/div.



0.5 V/div
Output Voltage on Pin 6

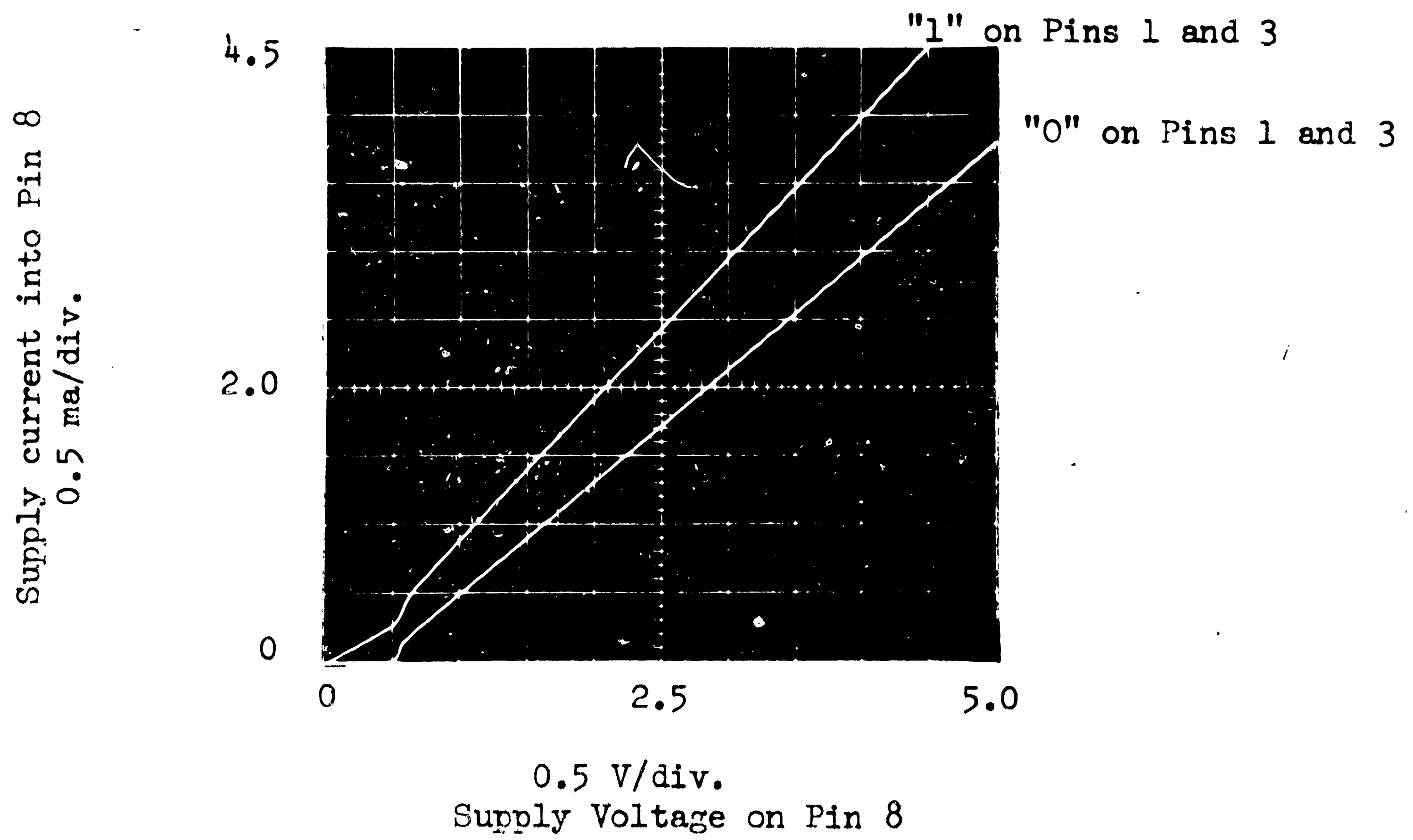
Output current into Pin 7
0.5 ma/div.



0.5 V/div.
Output Voltage on Pin 7

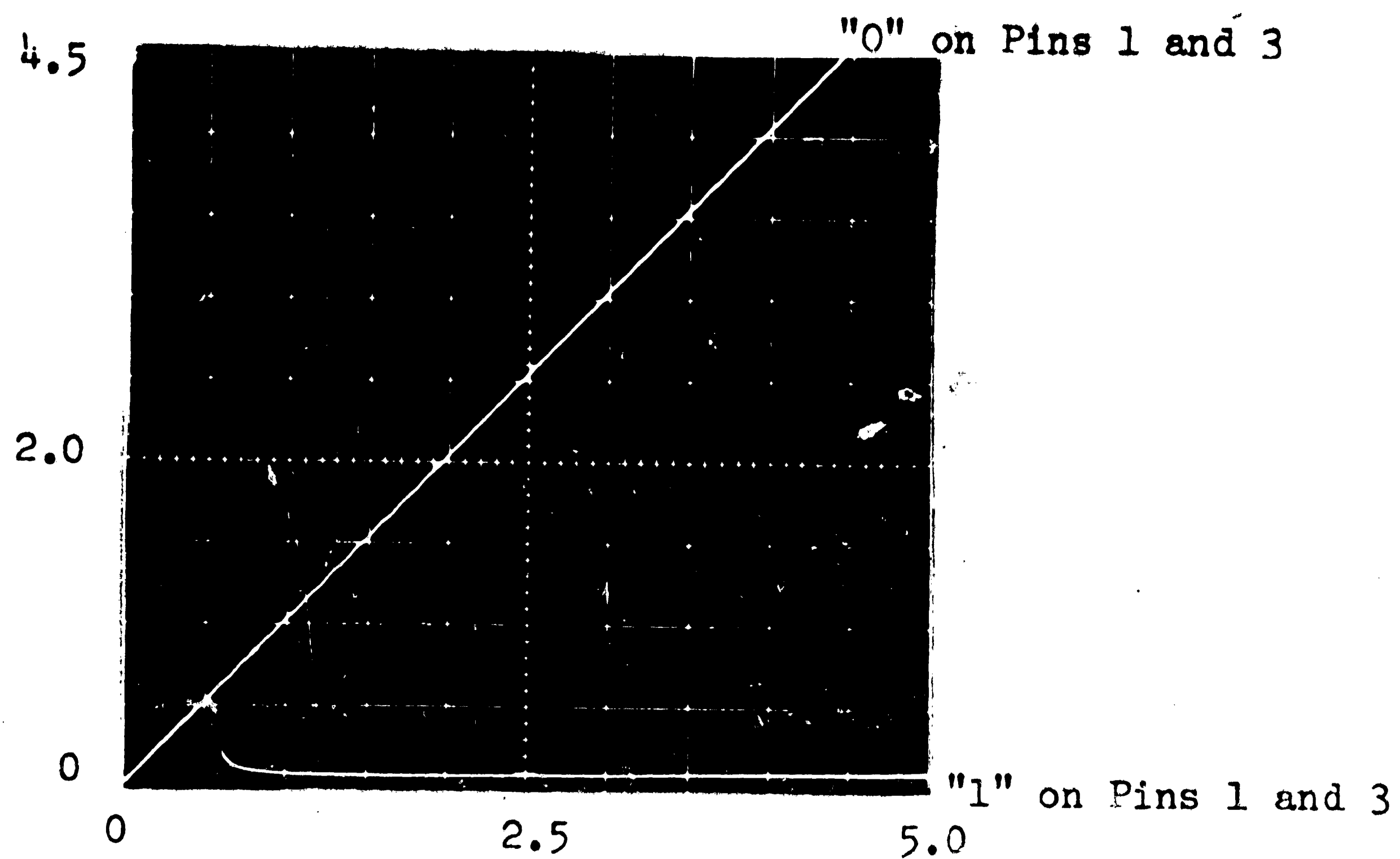
OUTPUT CHARACTERISTICS
DCTL H ELEMENT

3.2.62



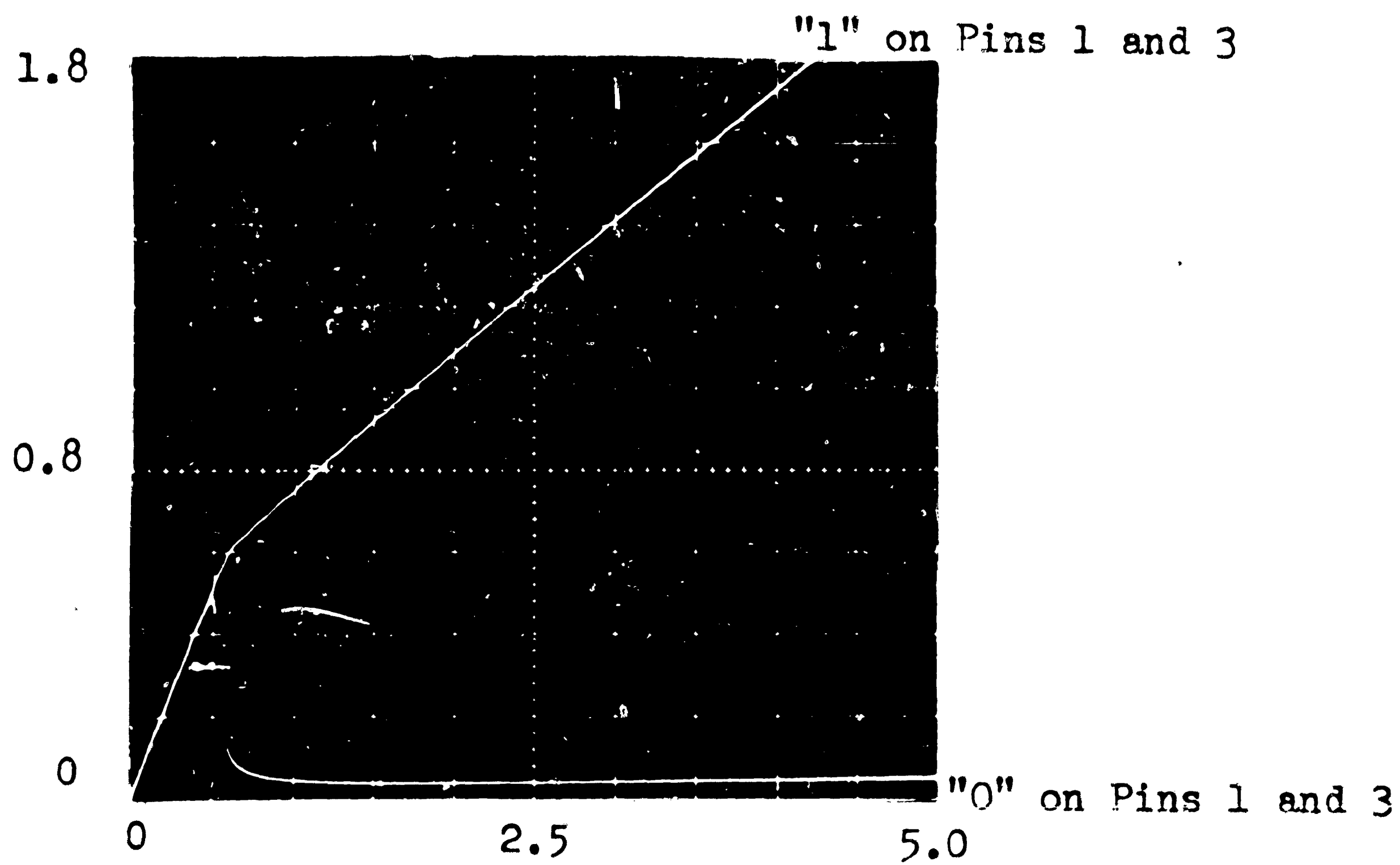
POWER DISSIPATION
DCTL H ELEMENT

Output voltage on Pin 6
0.5 V/div.



0.5 V/div.
Supply Voltage on Pin 8

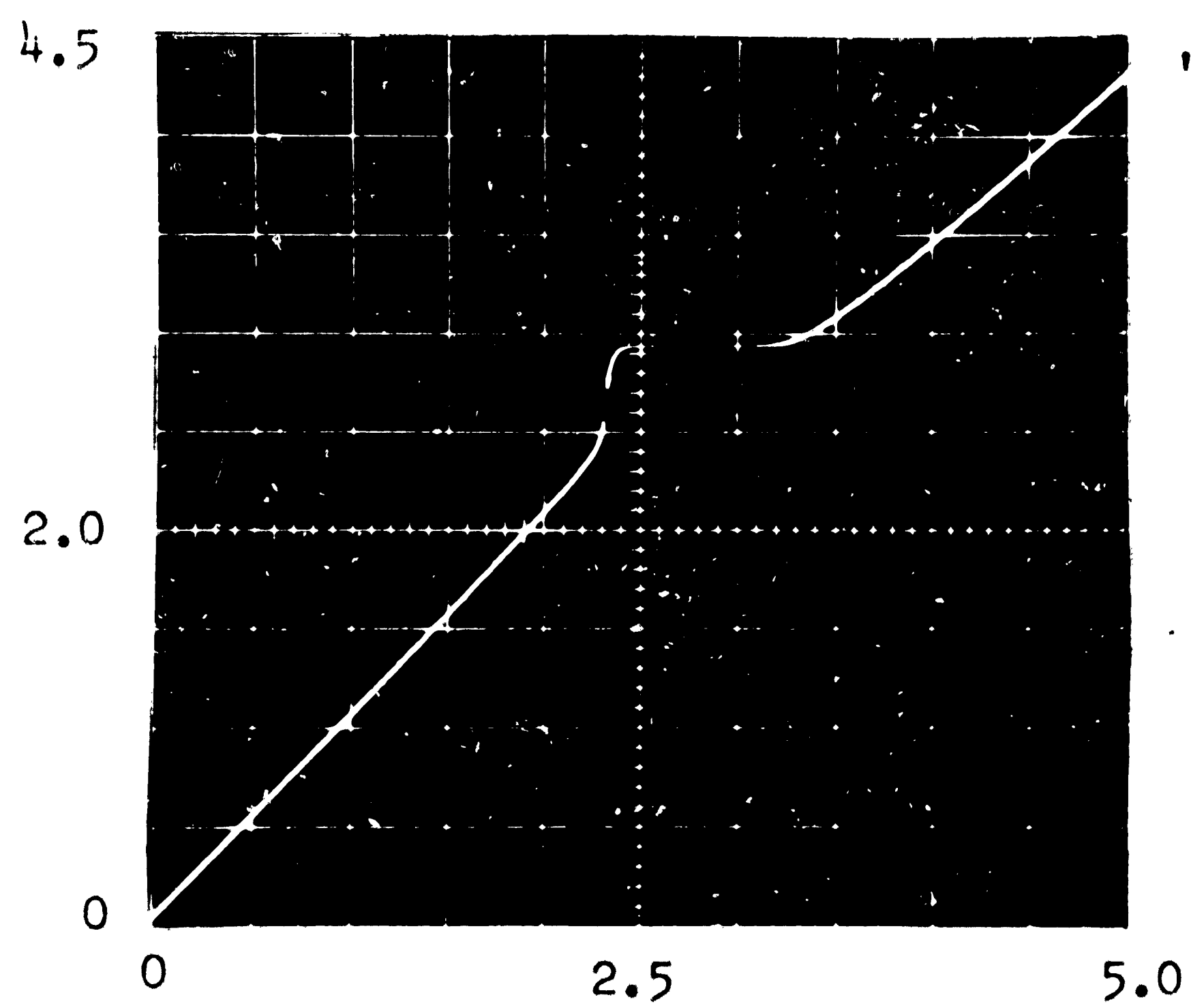
Output voltage on Pin 7
0.2 V/div.



0.5 V/div.
Supply Voltage on Pin 8

OUTPUT VOLTAGE versus SUPPLY VOLTAGES
DCTL H ELEMENT

Output voltage on Pin 7
0.5 V/div.



"0" on Pins 1 and 3

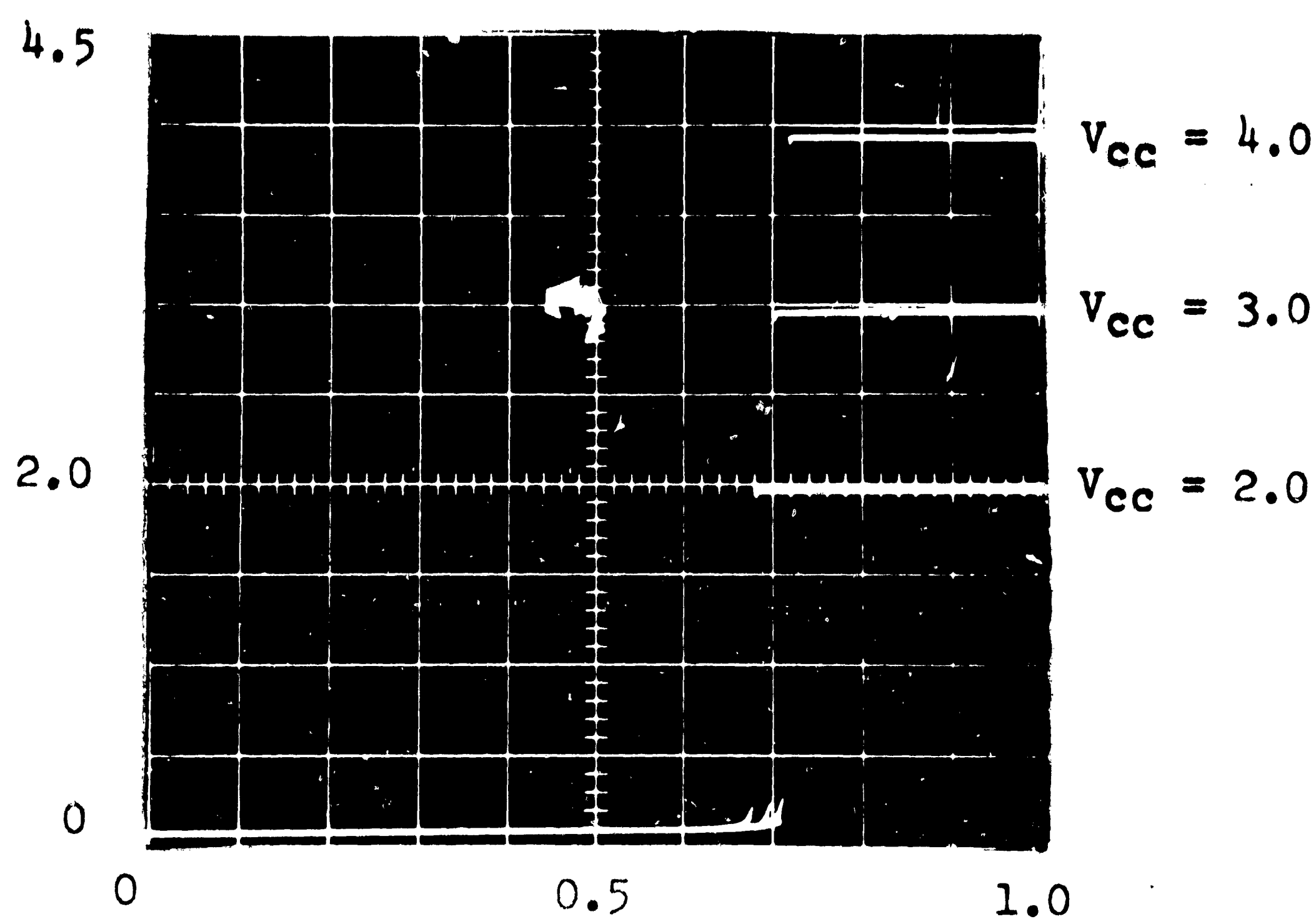
0.5 V/div.
Noise Voltage on Pin 4

OUTPUT VOLTAGE versus GROUND NOISE VOLTAGE
DCTL H ELEMENT



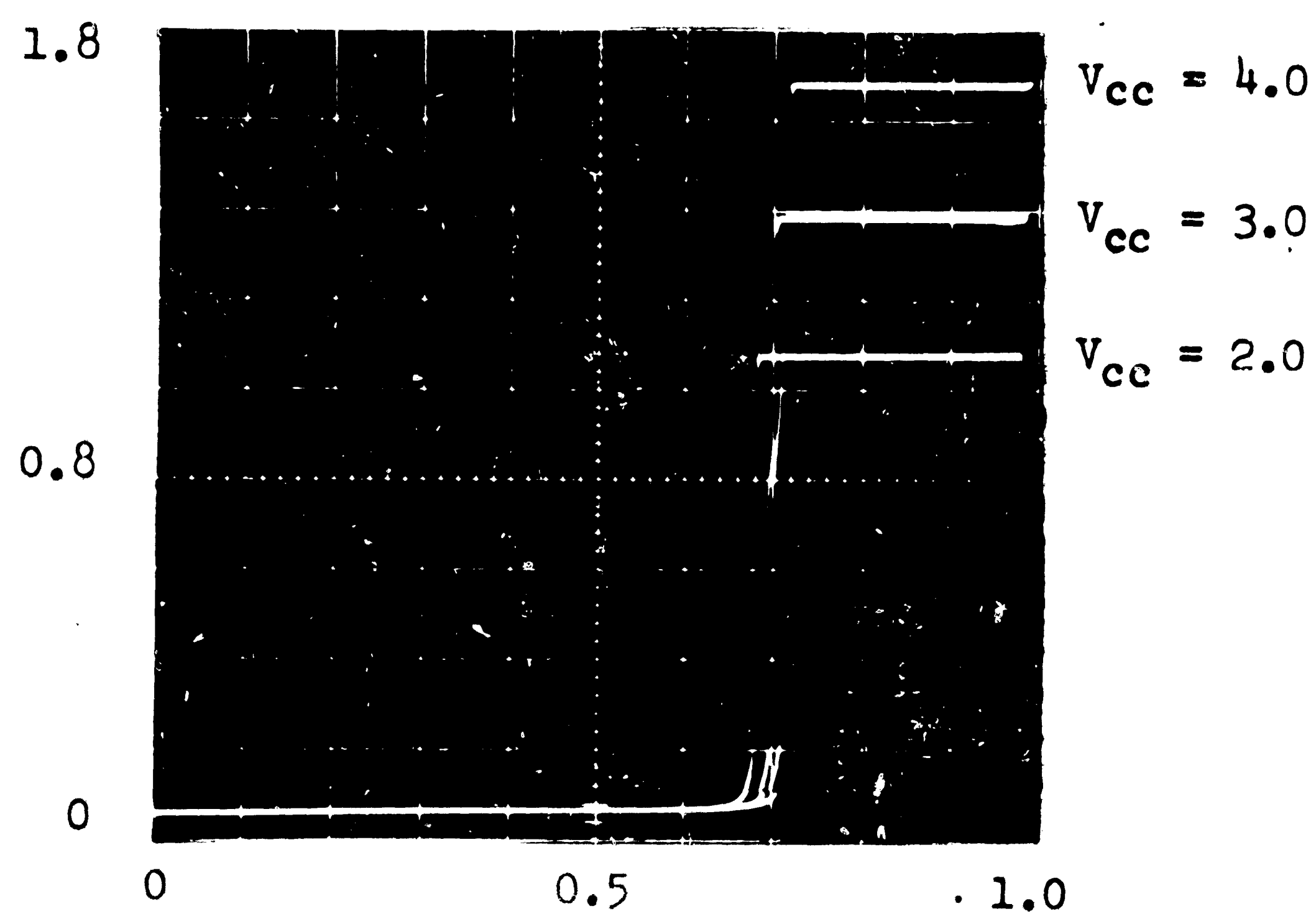
3.2.66

Output voltage on Pin 7
0.5 V/div.



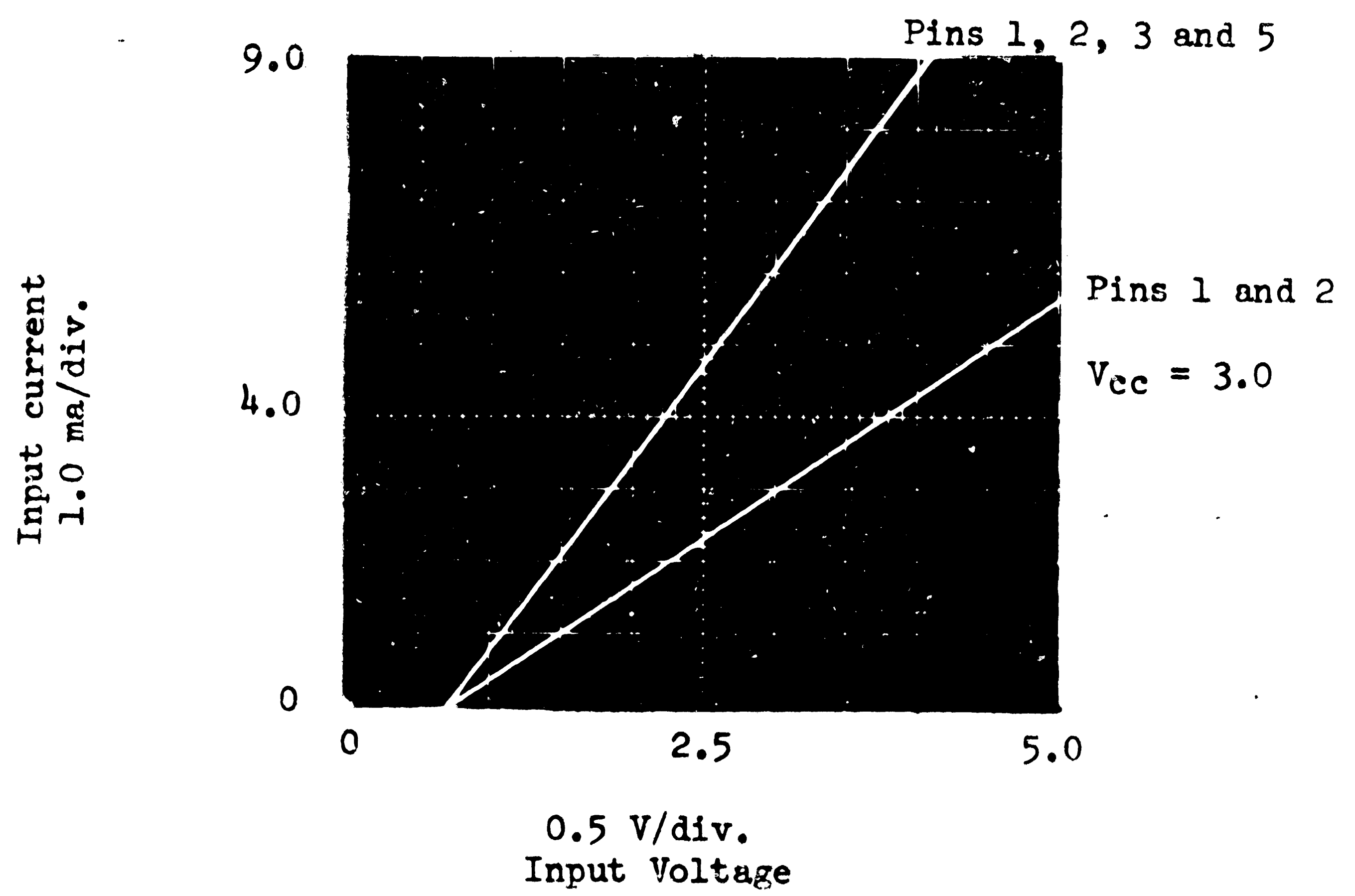
0.1 V/div.
Input Voltage on Pins 1 and 3

Output voltage on Pin 6
0.2 V/div.



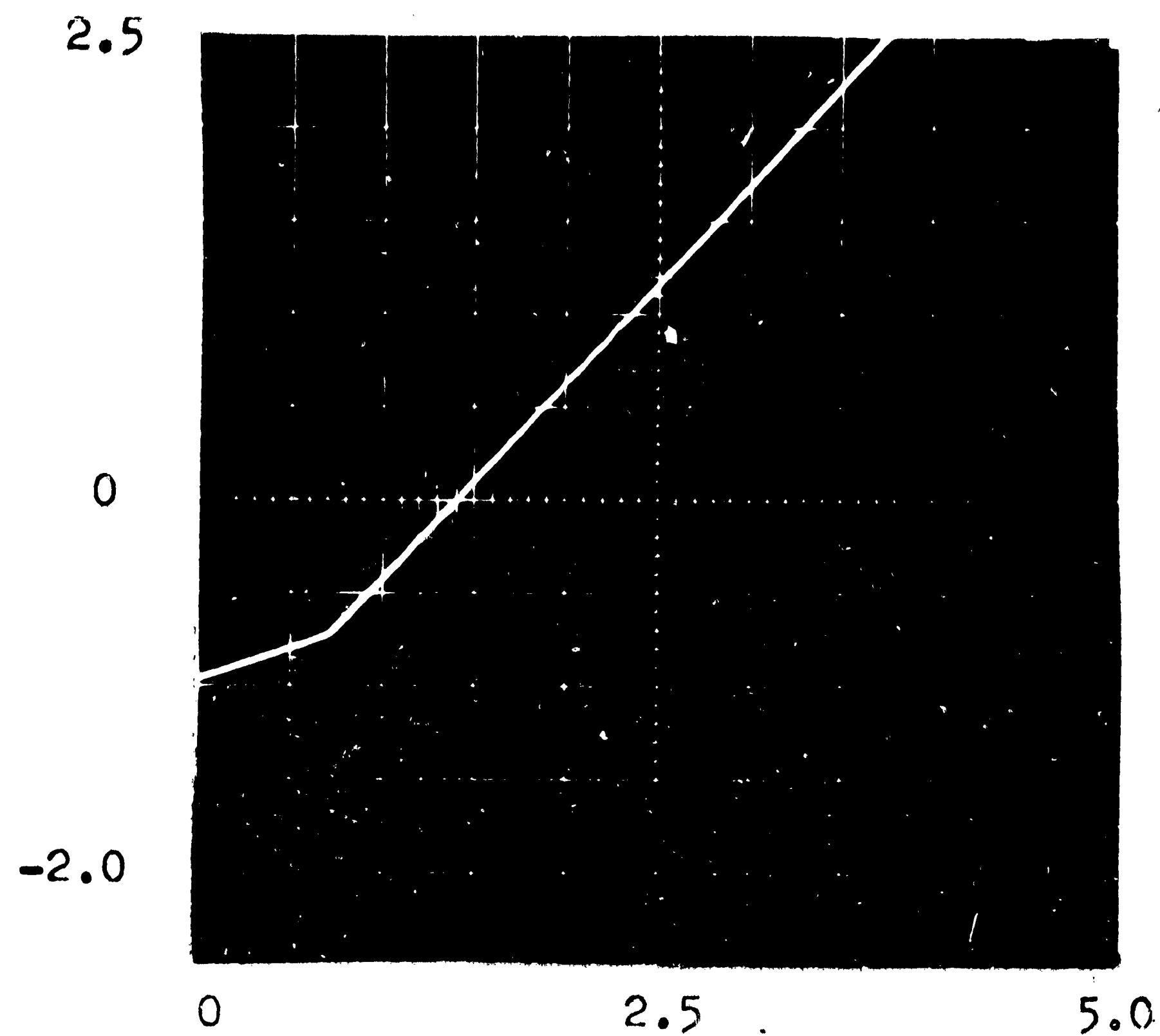
0.1 V/div.
Input Voltage on Pins 1, 2, 3 and 5

INPUT - OUTPUT CHARACTERISTICS
DCTL A ELEMENT



INPUT CHARACTERISTICS
DCTL A ELEMENT

Output current into Pin 6
0.5 ma/div.

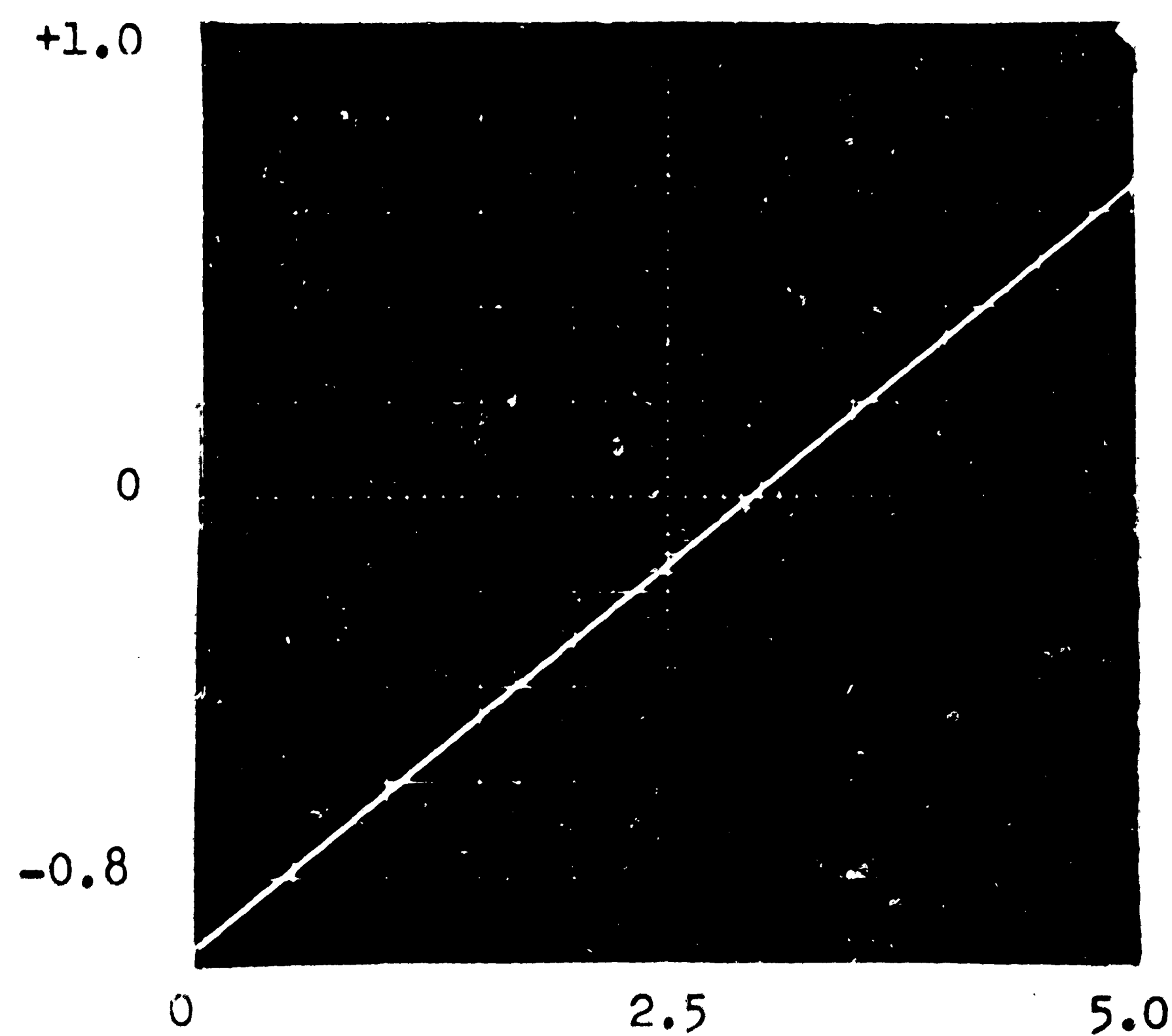


$V_{cc} = 3.0$

"1" on Pins 1,
2, 3 and 5

0.5 V/div.
Output Voltage on Pin 6

Output current into Pin 7
0.2 ma/div.



$V_{cc} = 3.0$

"1" on Pins 1 and 2

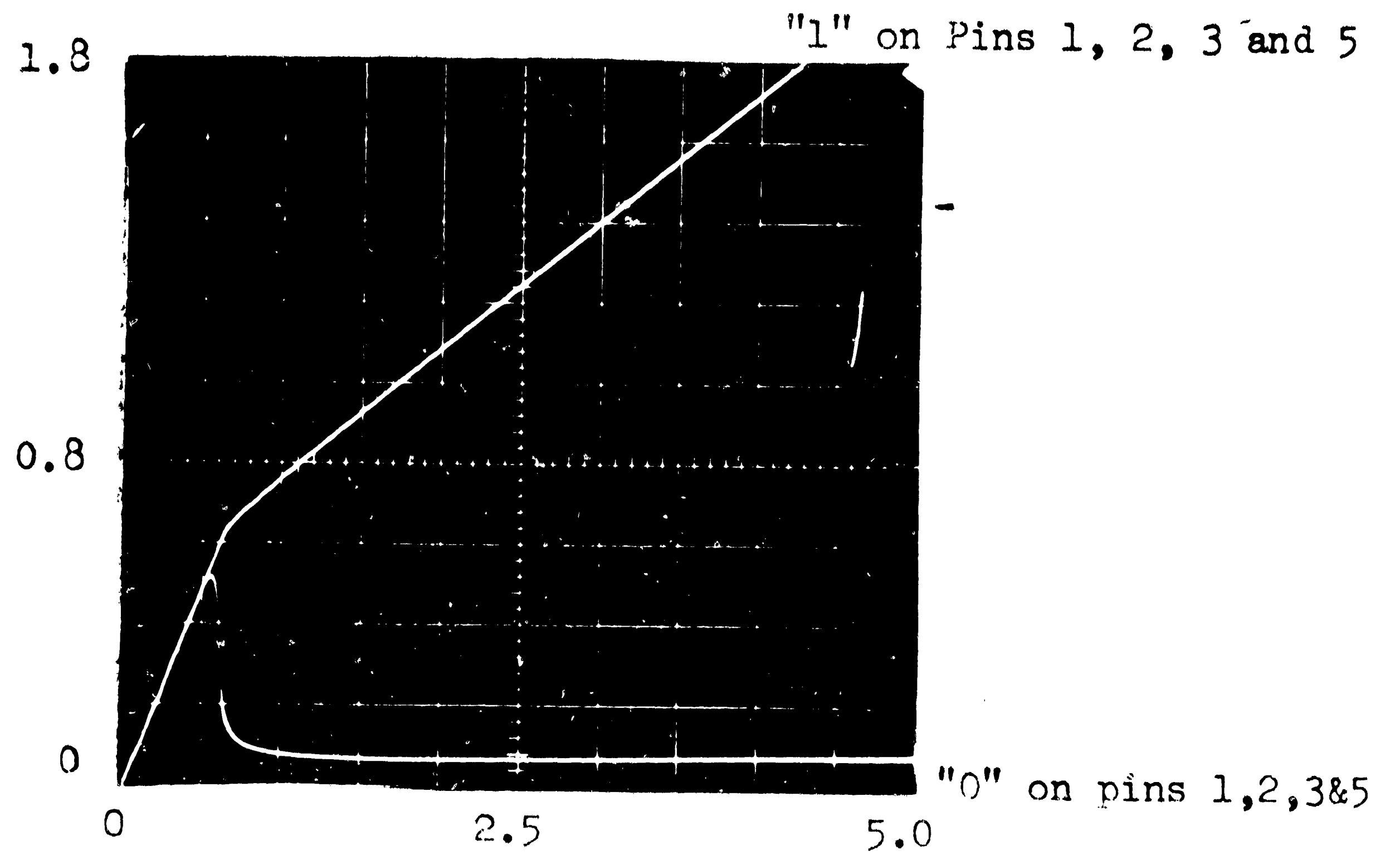
0.5 V/div.

Output Voltage on Pin 7

OUTPUT CHARACTERISTICS
DCTL A ELEMENT

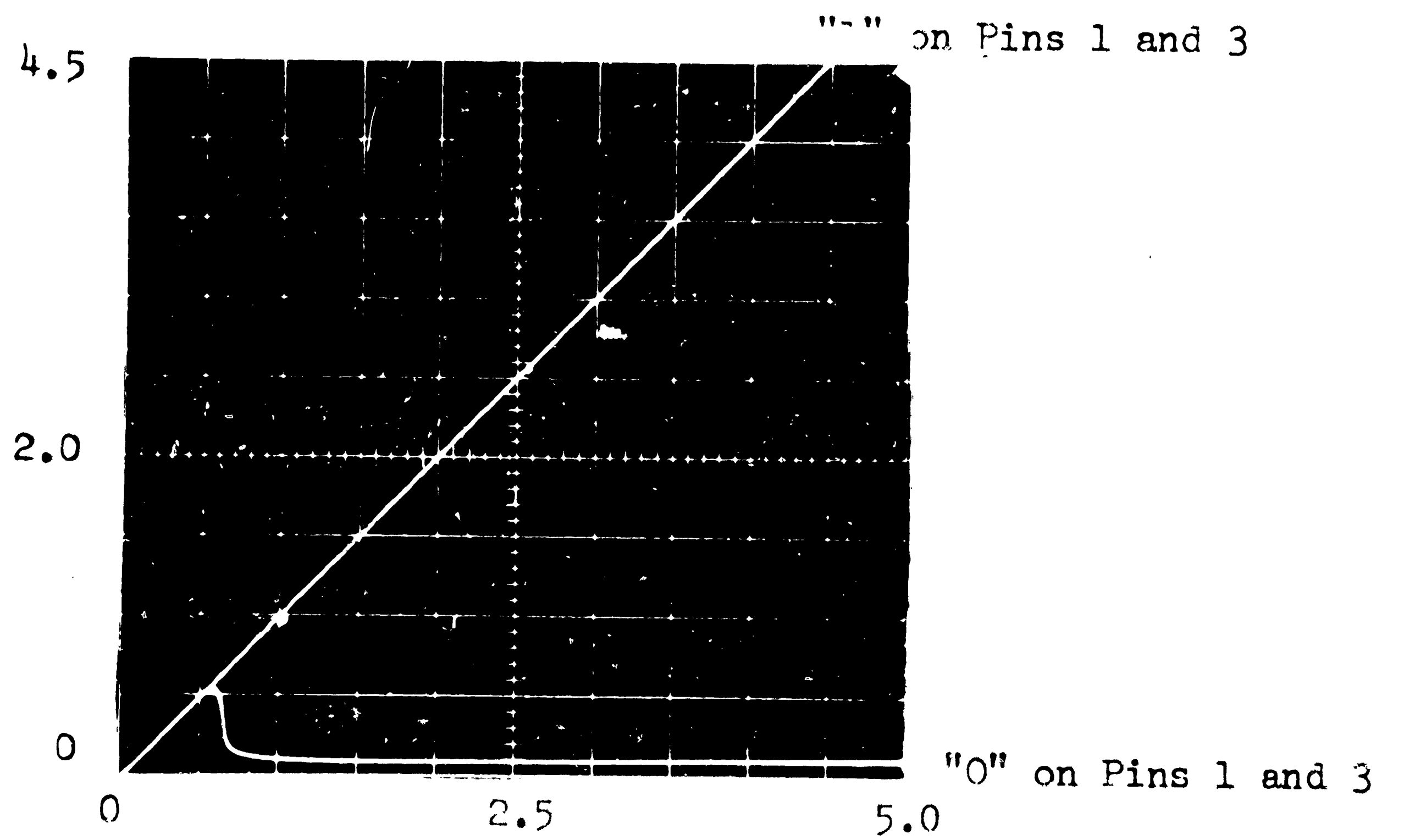
3.2.69

Output voltage on Pin 6
0.2 V/div.



0.5 V/div.
Supply Voltage on Pin 8

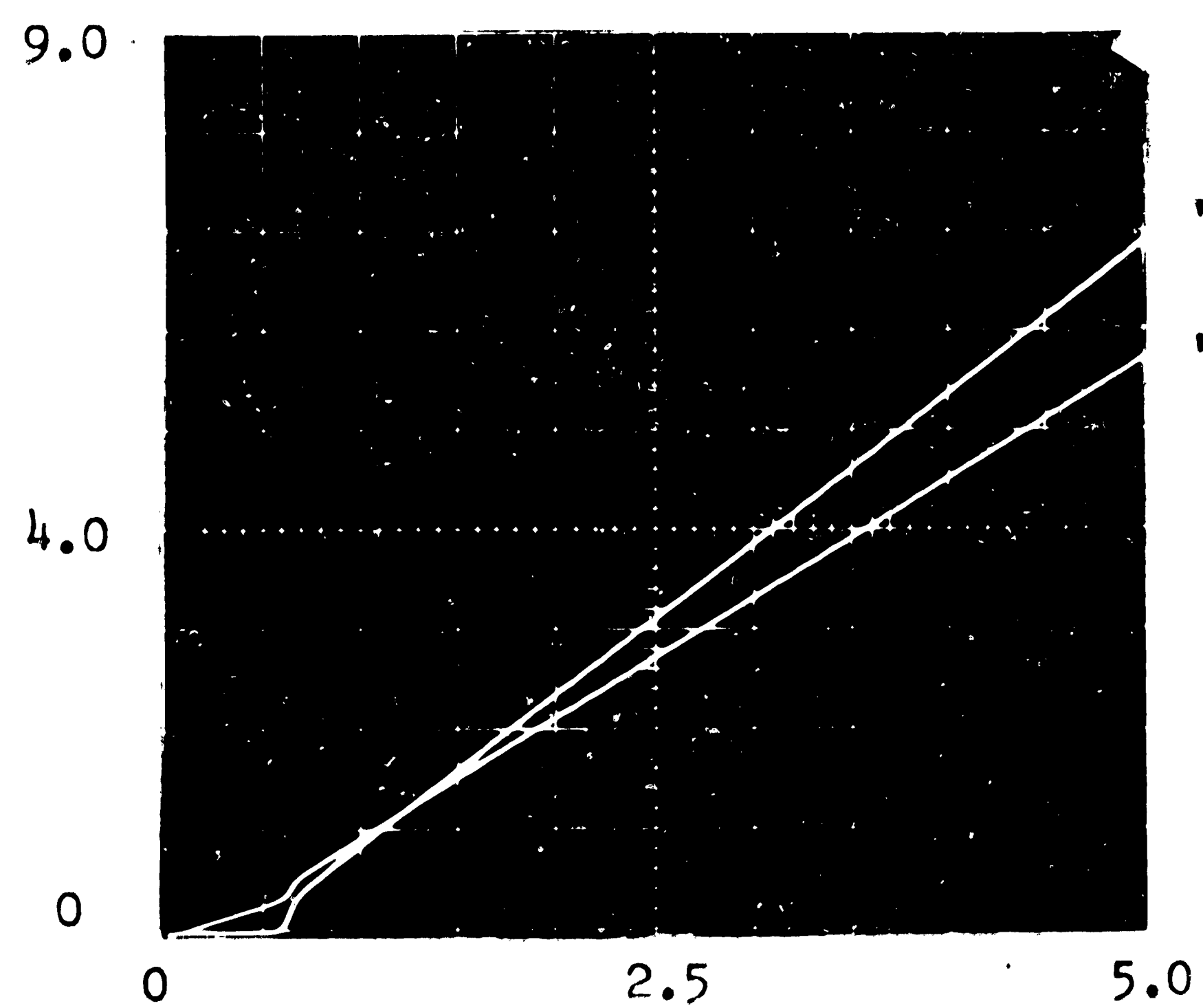
Output voltage on Pin 7
0.5 V/div.



0.5 V/div.
Supply Voltage on Pin 8

OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DCTL A ELEMENT

Supply current into Pin 8
1.0 ma/div.



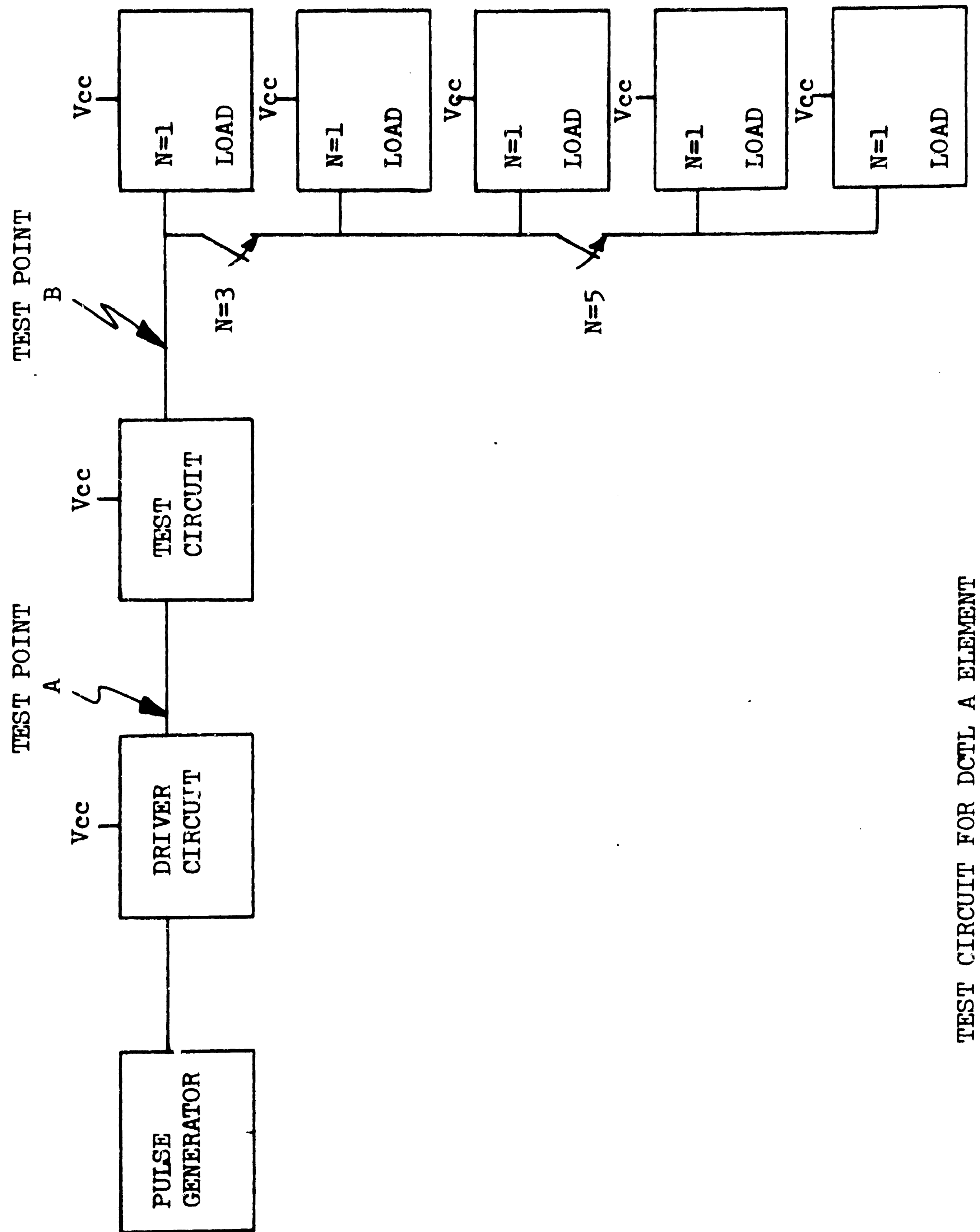
"0" on Pins 1 and 2

"1" on Pins 1 and 2

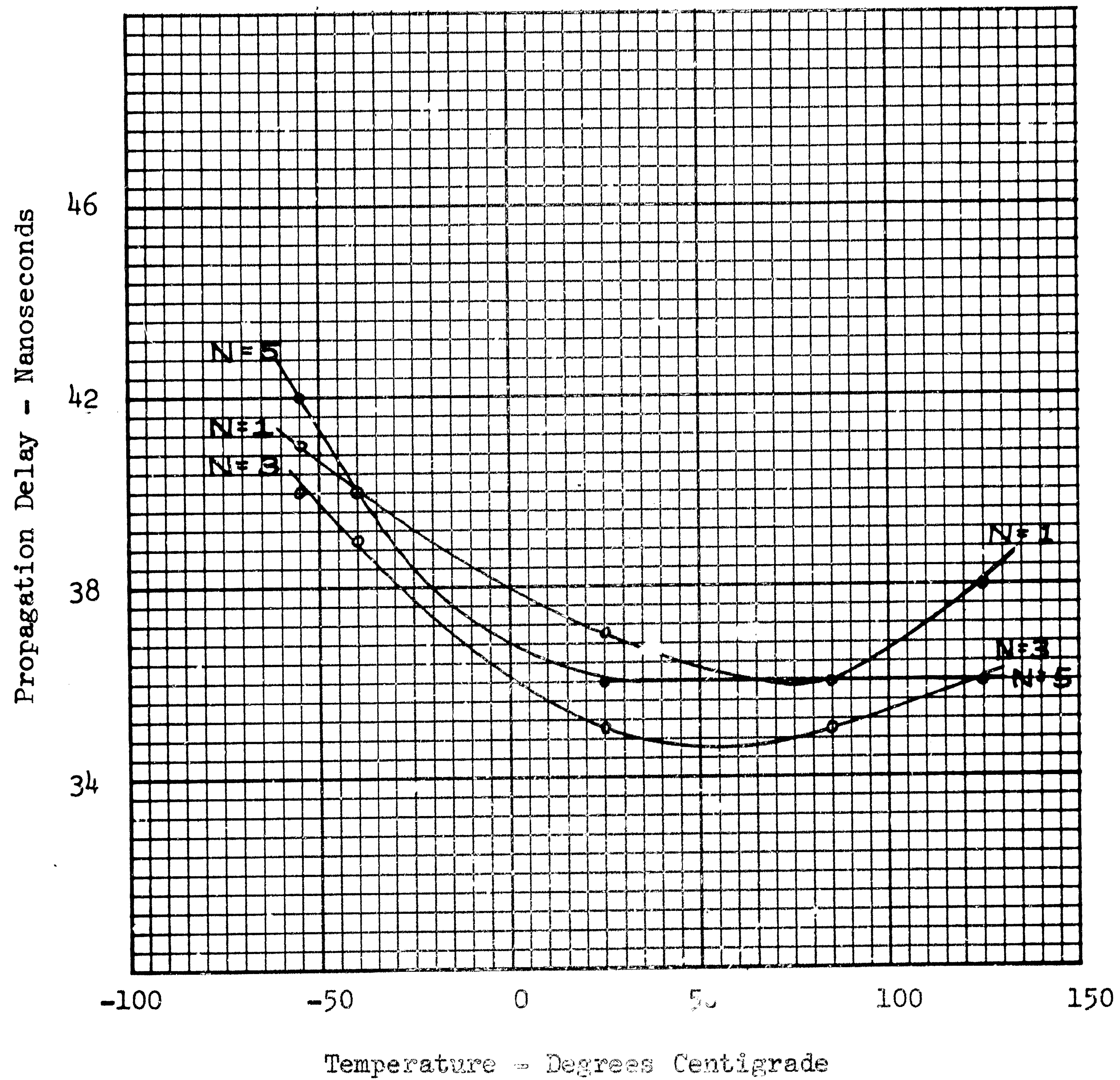
0.5 V/div.
Supply Voltage on Pin 8

POWER DISSIPATION
DCTL A ELEMENT

3.2.71



TEST CIRCUIT FOR DCTL A ELEMENT



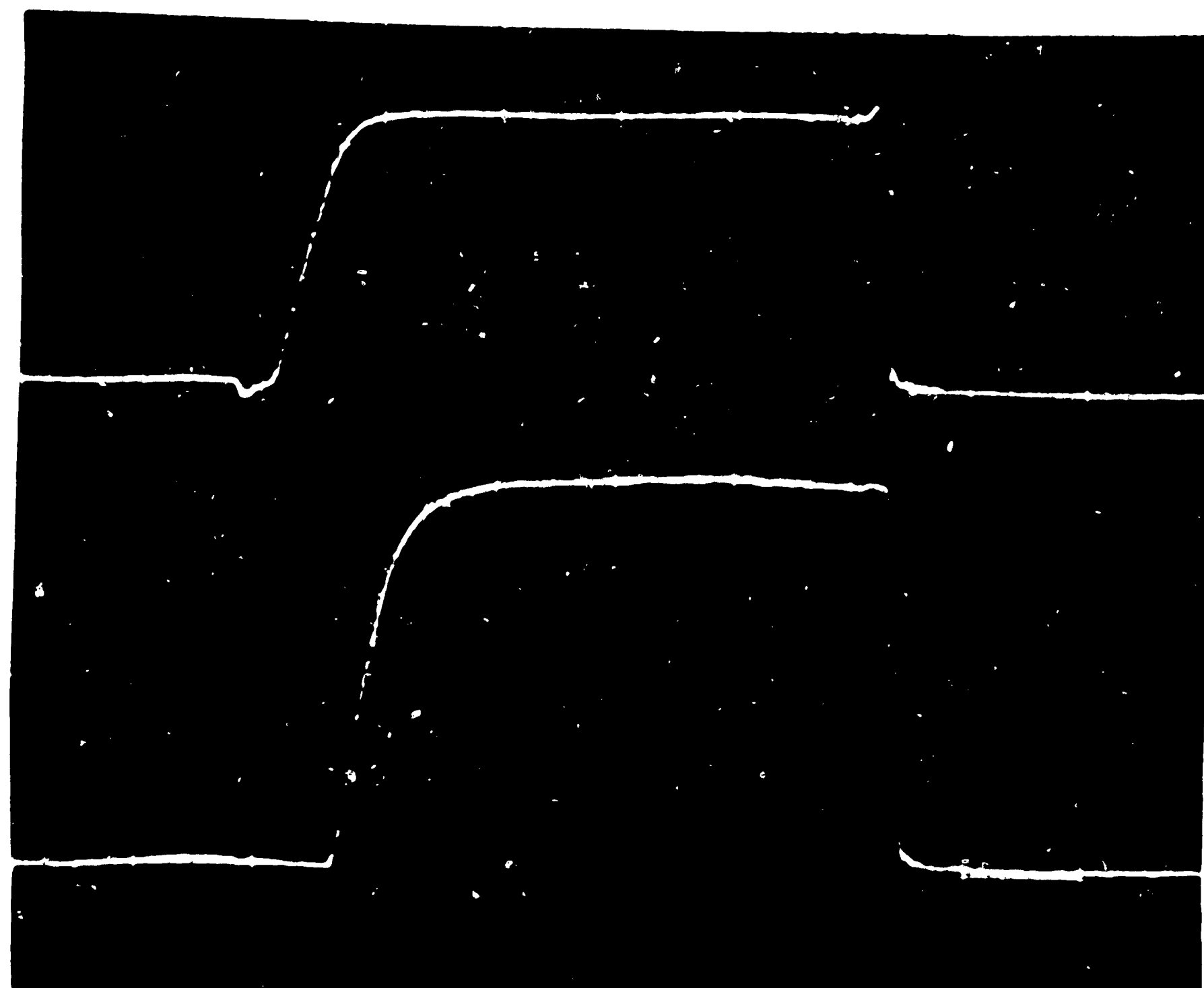
DATA FOR GRAPH TAKEN WITH TEST CIRCUIT AND LOAD SUPPLY AT 3.0 V

DCTL A ELEMENT

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +25°C Vcc 3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>463.</u>	<u>450.</u>	<u>448.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.94</u>	<u>1.02</u>	<u>1.38</u>	<u>1.72</u>
T_r	<u>51.</u>	<u>80.</u>	<u>73.</u>	<u>66.</u>
T_f	<u>11.</u>	<u>16.</u>	<u>13.</u>	<u>12.</u>
T_d		<u>59.</u>	<u>60.</u>	<u>62.</u>
T_s		<u>20.</u>	<u>15.</u>	<u>12.</u>
T_{pd}		<u>42.</u>	<u>37.</u>	<u>35.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. -40°C Vcc 3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>460.</u>	<u>455.</u>	<u>452.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.04</u>	<u>1.10</u>	<u>1.40</u>	<u>1.72</u>
T _r	<u>53.</u>	<u>75.</u>	<u>65.</u>	<u>61.</u>
T _f	<u>11.</u>	<u>12.</u>	<u>9.</u>	<u>8.</u>
T _d		<u>61.</u>	<u>63.</u>	<u>65.</u>
T _s		<u>21.</u>	<u>15.</u>	<u>12.</u>
T _{pd}		<u>45.</u>	<u>40.</u>	<u>38.</u>

Type RTL No. A Temp. -55°C Vcc 3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>459.</u>	<u>454.</u>	<u>451.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.06</u>	<u>1.12</u>	<u>1.42</u>	<u>1.72</u>
T _r	<u>54.</u>	<u>76.</u>	<u>65.</u>	<u>61.</u>
T _f	<u>12.</u>	<u>13.</u>	<u>9.</u>	<u>9.</u>
T _c		<u>64.</u>	<u>65.</u>	<u>67.</u>
T _s		<u>22.</u>	<u>16.</u>	<u>12.</u>
T _{pd}		<u>42.</u>	<u>41.</u>	<u>40.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +85°C Vcc 3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>465.</u>	<u>460.</u>	<u>457.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.35</u>	<u>0.97</u>	<u>1.28</u>	<u>1.60</u>
T _r	<u>53.</u>	<u>76.</u>	<u>70.</u>	<u>67.</u>
T _f	<u>11.</u>	<u>13.</u>	<u>12.</u>	<u>12.</u>
T _d		<u>54.</u>	<u>56.</u>	<u>58.</u>
T _s		<u>20.</u>	<u>15.</u>	<u>13.</u>
T _{pd}		<u>40.</u>	<u>36.</u>	<u>35.</u>

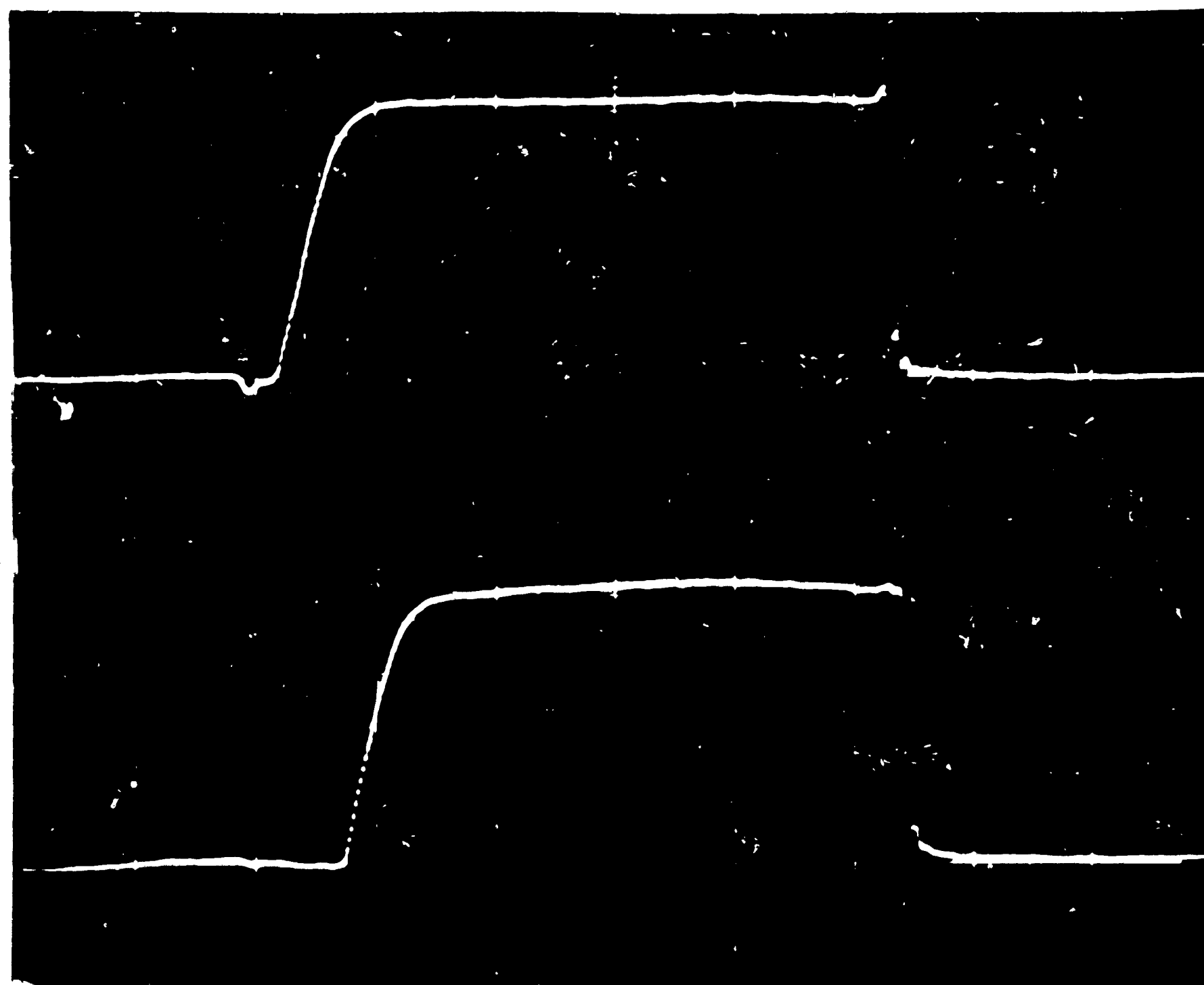
Type RTL No. A Temp. +125°C Vcc 3.0 = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>467.</u>	<u>462.</u>	<u>459.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.77</u>	<u>0.90</u>	<u>1.22</u>	<u>1.56</u>
T _r	<u>57.</u>	<u>81.</u>	<u>75.</u>	<u>72.</u>
T _f	<u>14.</u>	<u>14.</u>	<u>12.</u>	<u>12.</u>
T _d		<u>54.</u>	<u>57.</u>	<u>60.</u>
T _s		<u>21.</u>	<u>17.</u>	<u>15.</u>
T _{pd}		<u>40.</u>	<u>38.</u>	<u>37.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +25°C Vcc 3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>464.</u>	<u>463.</u>	<u>461.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.96</u>	<u>0.80</u>	<u>0.95</u>	<u>1.09</u>
T_r	<u>51.</u>	<u>71.</u>	<u>53.</u>	<u>46.</u>
T_f	<u>11.</u>	<u>15.</u>	<u>12.</u>	<u>12.</u>
T_d		<u>54.</u>	<u>56.</u>	<u>57.</u>
T_s		<u>20.</u>	<u>15.</u>	<u>12.</u>
T_{pd}		<u>41.</u>	<u>35.</u>	<u>32.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. -40°C Vcc 3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>458.</u>	<u>458.</u>	<u>456.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.06</u>	<u>0.92</u>	<u>1.06</u>	<u>1.20</u>
T _r	<u>52.</u>	<u>76.</u>	<u>56.</u>	<u>48.</u>
T _f	<u>11.</u>	<u>15.</u>	<u>14.</u>	<u>12.</u>
T _d		<u>59.</u>	<u>60.</u>	<u>62.</u>
T _s		<u>22.</u>	<u>15.</u>	<u>13.</u>
T _{pd}		<u>46.</u>	<u>39.</u>	<u>35.</u>

Type RTL No. A Temp. -55°C Vcc 3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>458.</u>	<u>456.</u>	<u>454.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.09</u>	<u>0.94</u>	<u>1.08</u>	<u>1.22</u>
T _r	<u>55.</u>	<u>79.</u>	<u>58.</u>	<u>49.</u>
T _f	<u>12.</u>	<u>14.</u>	<u>13.</u>	<u>13.</u>
T _d		<u>61.</u>	<u>63.</u>	<u>65.</u>
T _s		<u>23.</u>	<u>16.</u>	<u>13.</u>
T _{pd}		<u>49.</u>	<u>40.</u>	<u>37.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +85°C Vcc 3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>466.</u>	<u>464.</u>	<u>463.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.87</u>	<u>0.71</u>	<u>0.86</u>	<u>1.0</u>
T _r	<u>54.</u>	<u>69.</u>	<u>53.</u>	<u>48.</u>
T _f	<u>11.</u>	<u>15.</u>	<u>13.</u>	<u>12</u>
T _d		<u>53.</u>	<u>55.</u>	<u>57.</u>
T _s		<u>20.</u>	<u>15.</u>	<u>13.</u>
T _{pd}		<u>40.</u>	<u>35.</u>	<u>33.</u>

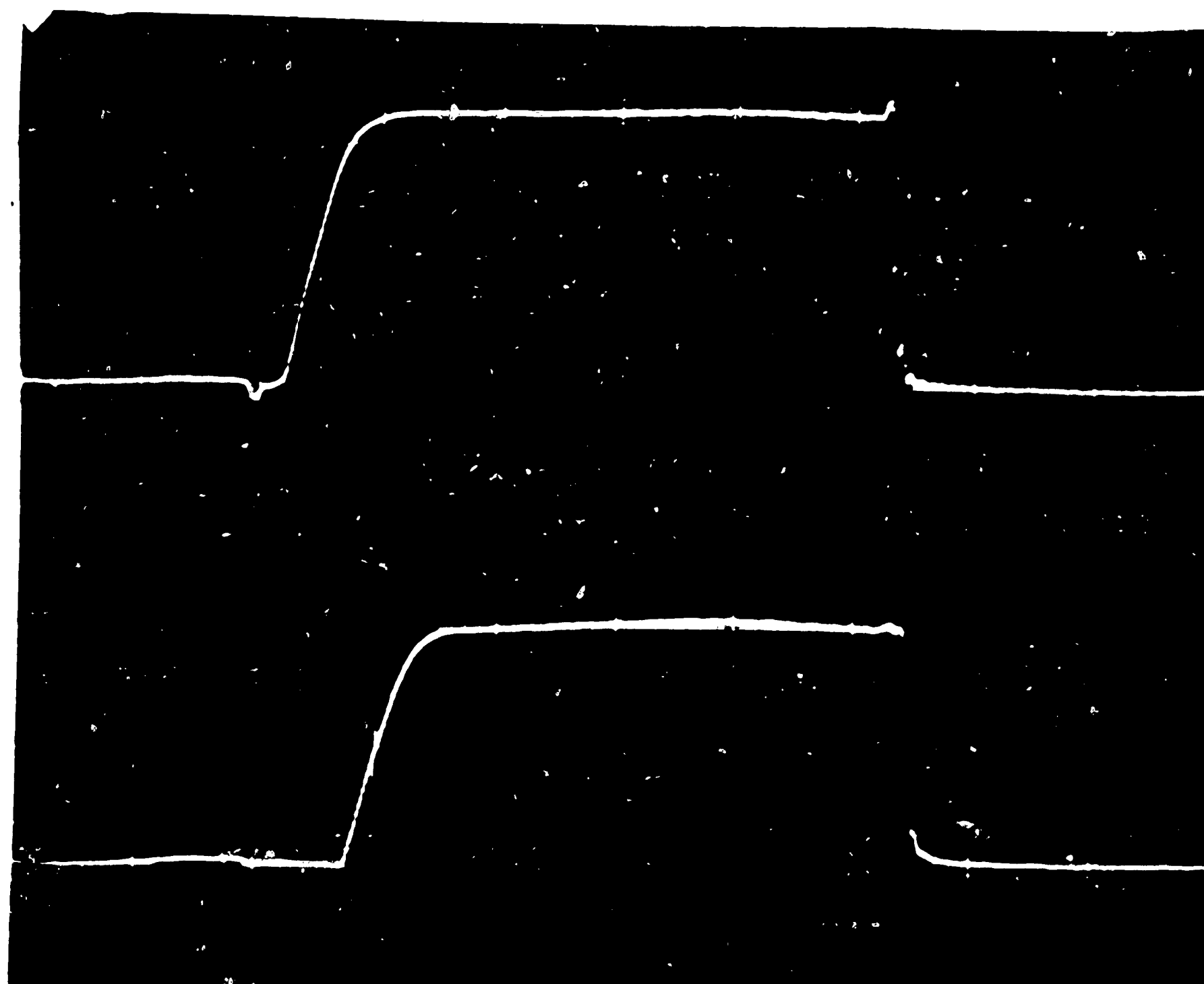
Type RTL No. A Temp. +125°C Vcc 3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>467.</u>	<u>465.</u>	<u>463.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.79</u>	<u>0.63</u>	<u>0.78</u>	<u>0.92</u>
T _r	<u>58.</u>	<u>68.</u>	<u>54.</u>	<u>50.</u>
T _f	<u>14.</u>	<u>15.</u>	<u>13.</u>	<u>12.</u>
T _d		<u>54.</u>	<u>56.</u>	<u>58.</u>
T _s		<u>21.</u>	<u>17.</u>	<u>15.</u>
T _{pd}		<u>40.</u>	<u>36.</u>	<u>34.</u>

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +25°C Vcc 3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>458.</u>	<u>459.</u>	<u>458.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.95</u>	<u>0.74</u>	<u>0.83</u>	<u>0.92</u>
T_r	<u>52.</u>	<u>80.</u>	<u>55.</u>	<u>45.</u>
T_f	<u>10.</u>	<u>15.</u>	<u>13.</u>	<u>12</u>
T_d		<u>55.</u>	<u>56.</u>	<u>57.</u>
T_s		<u>19.</u>	<u>13.</u>	<u>11.</u>
T_{pd}		<u>44.</u>	<u>36.</u>	<u>33.</u>



TEST CIRCUIT OUTPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. -40°C Vcc 3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>453.</u>	<u>454.</u>	<u>455.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.06</u>	<u>0.84</u>	<u>0.95</u>	<u>1.04</u>
T _r	<u>54.</u>	<u>89.</u>	<u>61.</u>	<u>49.</u>
T _f	<u>11.</u>	<u>15.</u>	<u>14.</u>	<u>12.</u>
T _d		<u>61.</u>	<u>61.</u>	<u>63.</u>
T _s		<u>22.</u>	<u>15.</u>	<u>13.</u>
T _{pd}		<u>50.</u>	<u>40.</u>	<u>37.</u>

Type RTL No. A Temp. -55°C Vcc 3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>451.</u>	<u>453.</u>	<u>452.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>1.08</u>	<u>0.88</u>	<u>0.97</u>	<u>1.06</u>
T _r	<u>55.</u>	<u>92.</u>	<u>63.</u>	<u>50.</u>
T _f	<u>11.</u>	<u>16.</u>	<u>14.</u>	<u>13.</u>
T _d		<u>63.</u>	<u>64.</u>	<u>66.</u>
T _s		<u>22.</u>	<u>16.</u>	<u>13.</u>
T _{pd}		<u>53.</u>	<u>42.</u>	<u>39.</u>

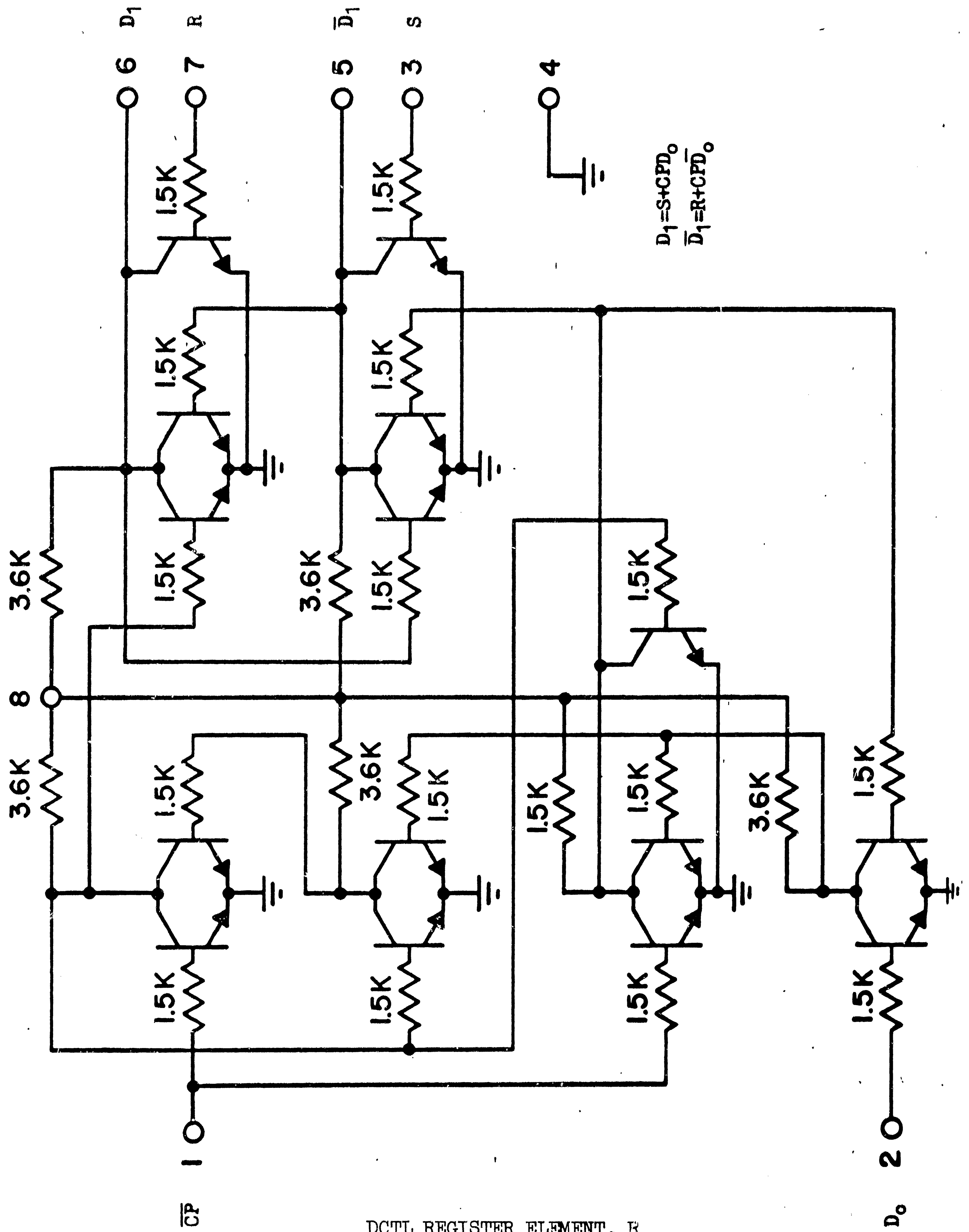
GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +85°C Vcc 3.0 N = 5

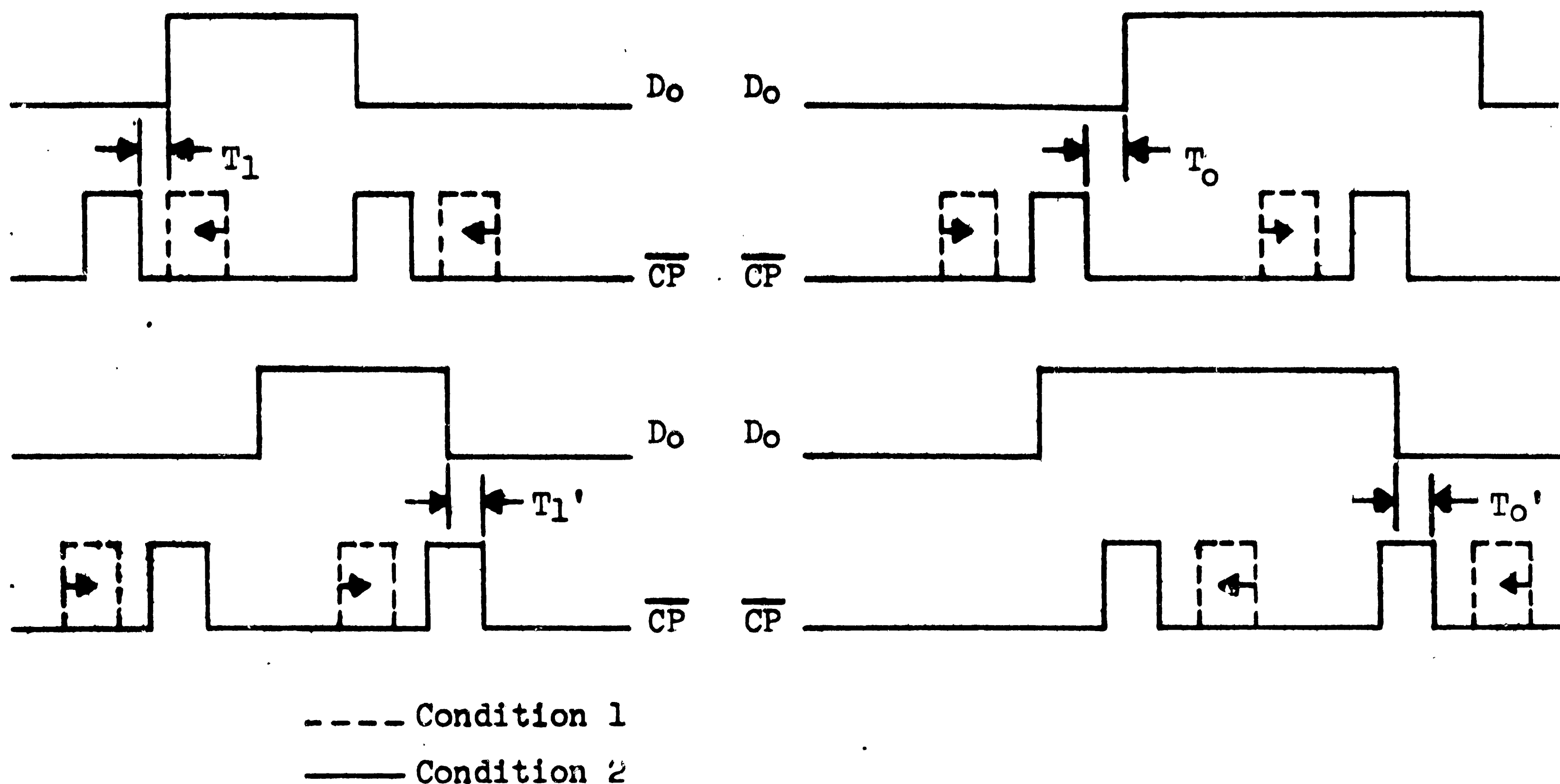
	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>461.</u>	<u>462.</u>	<u>462</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.85</u>	<u>0.64</u>	<u>0.73</u>	<u>0.82</u>
T _r	<u>53.</u>	<u>77.</u>	<u>55.</u>	<u>46.</u>
T _f	<u>10.</u>	<u>17.</u>	<u>13.</u>	<u>13.</u>
T _d		<u>54.</u>	<u>55.</u>	<u>57.</u>
T _s		<u>19.</u>	<u>15.</u>	<u>12.</u>
T _{pd}		<u>42.</u>	<u>36.</u>	<u>34.</u>

Type RTL No. A Temp. +125°C Vcc 3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>2.0</u>	Vcc <u>3.0</u>	Vcc <u>4.0</u>
Pulse Width	<u>500.</u>	<u>462.</u>	<u>464.</u>	<u>461.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>0.78</u>	<u>0.57</u>	<u>0.66</u>	<u>0.75</u>
T _r	<u>57.</u>	<u>77.</u>	<u>56.</u>	<u>47.</u>
T _f	<u>12.</u>	<u>19.</u>	<u>16.</u>	<u>14.</u>
T _d		<u>54.</u>	<u>56.</u>	<u>58.</u>
T _s		<u>20.</u>	<u>16.</u>	<u>14.</u>
T _{pd}		<u>42.</u>	<u>36.</u>	<u>35.</u>



DCTL REGISTER ELEMENT, R

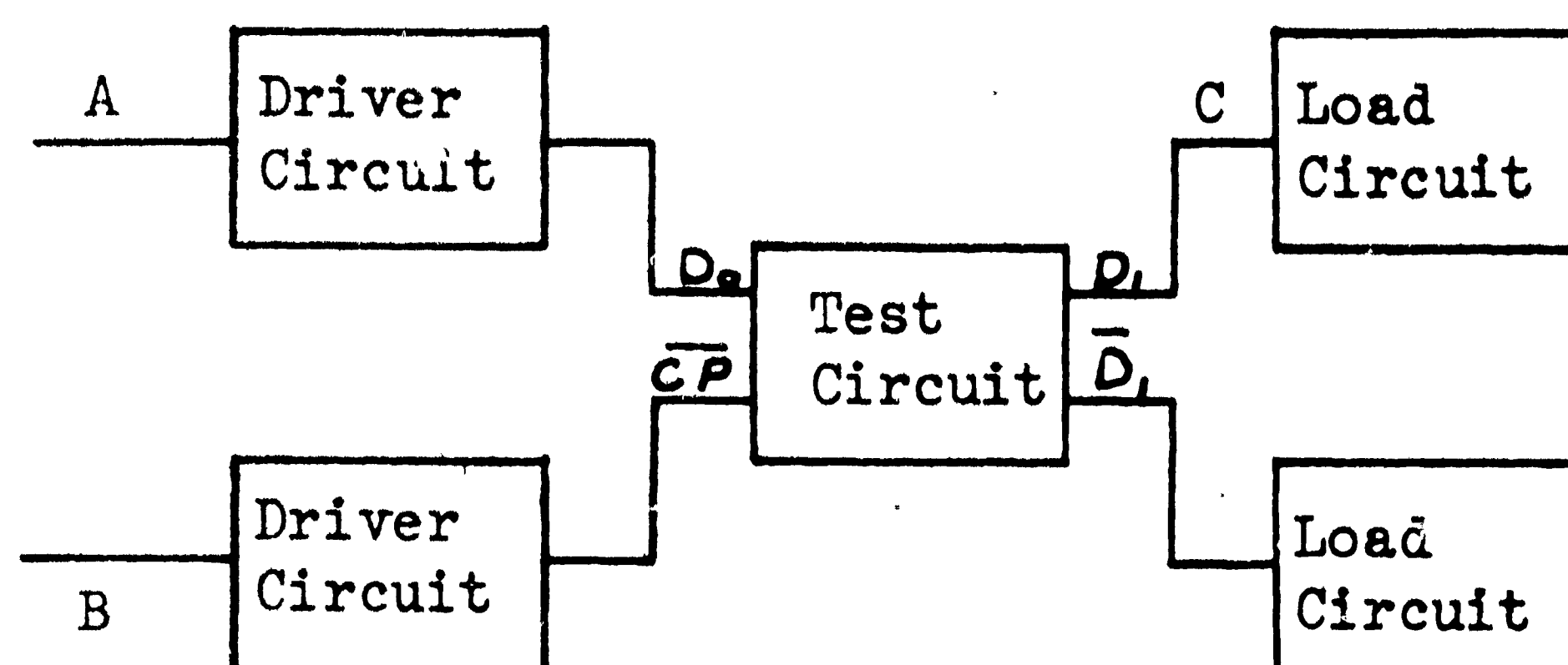


PROCEDURE FOR DETERMINING MINIMUM TIME RELATIONSHIPS
 BETWEEN \overline{CP} INPUT AND D_0 INPUT

PROCEDURE:

1. The inputs were time orientated as shown in the above diagrams as condition 1.
2. The input clock pulse \overline{CP} was delayed in the direction of the arrows until the circuit ceased to operate as viewed at D_1 .
3. The pulse train \overline{CP} was then reversed until the circuit began to toggle and the time indicated for each case was recorded between the 50% points.

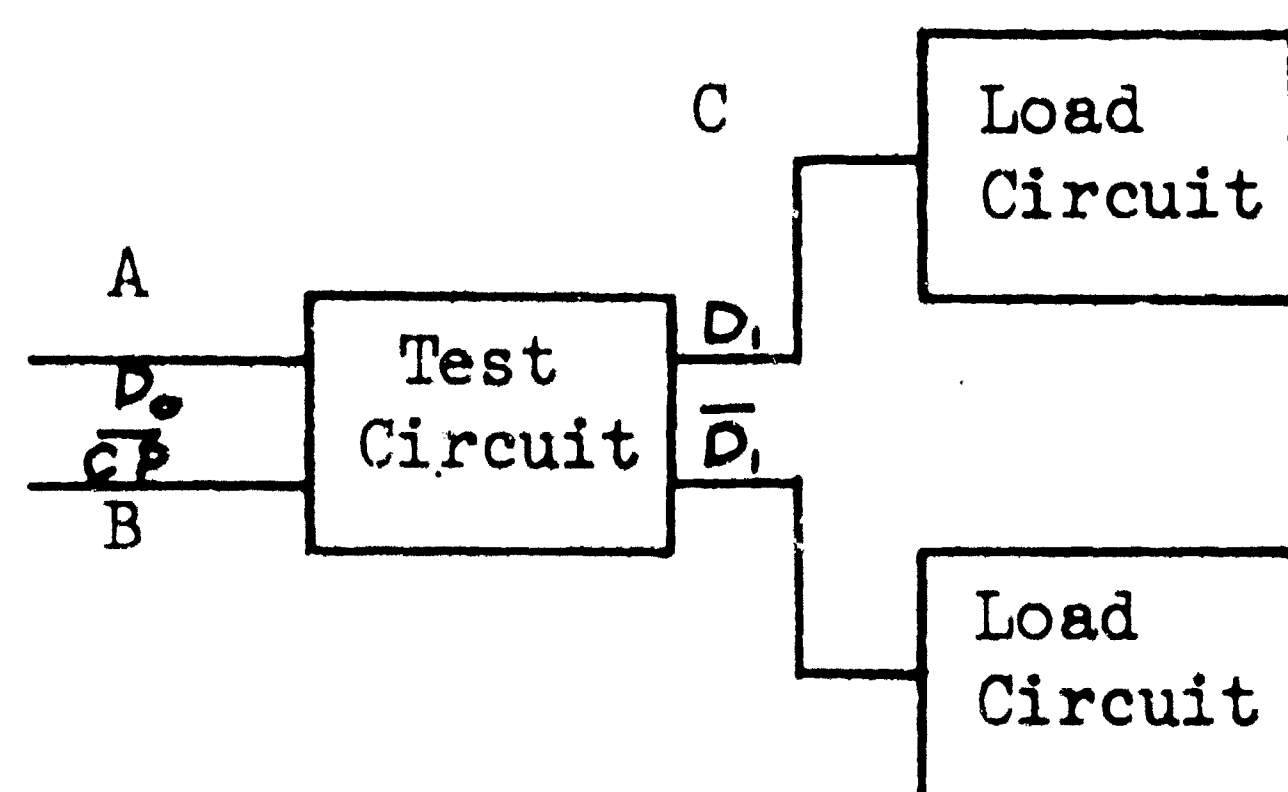
NOTE: The threshold voltage of the clock pulse is approximately 0.6 volts. That is, the trigger point is at .6 volts on the negative slope of the clock pulse. The measuring point is at 50% or 1.5 V on the 1.5 V and 0.6 V on a 20 ns fall time pulse should account for the apparent pre-trigger when setting the output high.



CONDITION 1

	25°C	-55°C	+125°C
T_1	6.57	6.3	10.4
T_1'	2.97	1.5	15.3
T_o	6.85	6.7	12.9
T_o'	7.17	1.5	18.

The table of data is an average of 4 readings for each temperature and read at the driver inputs.



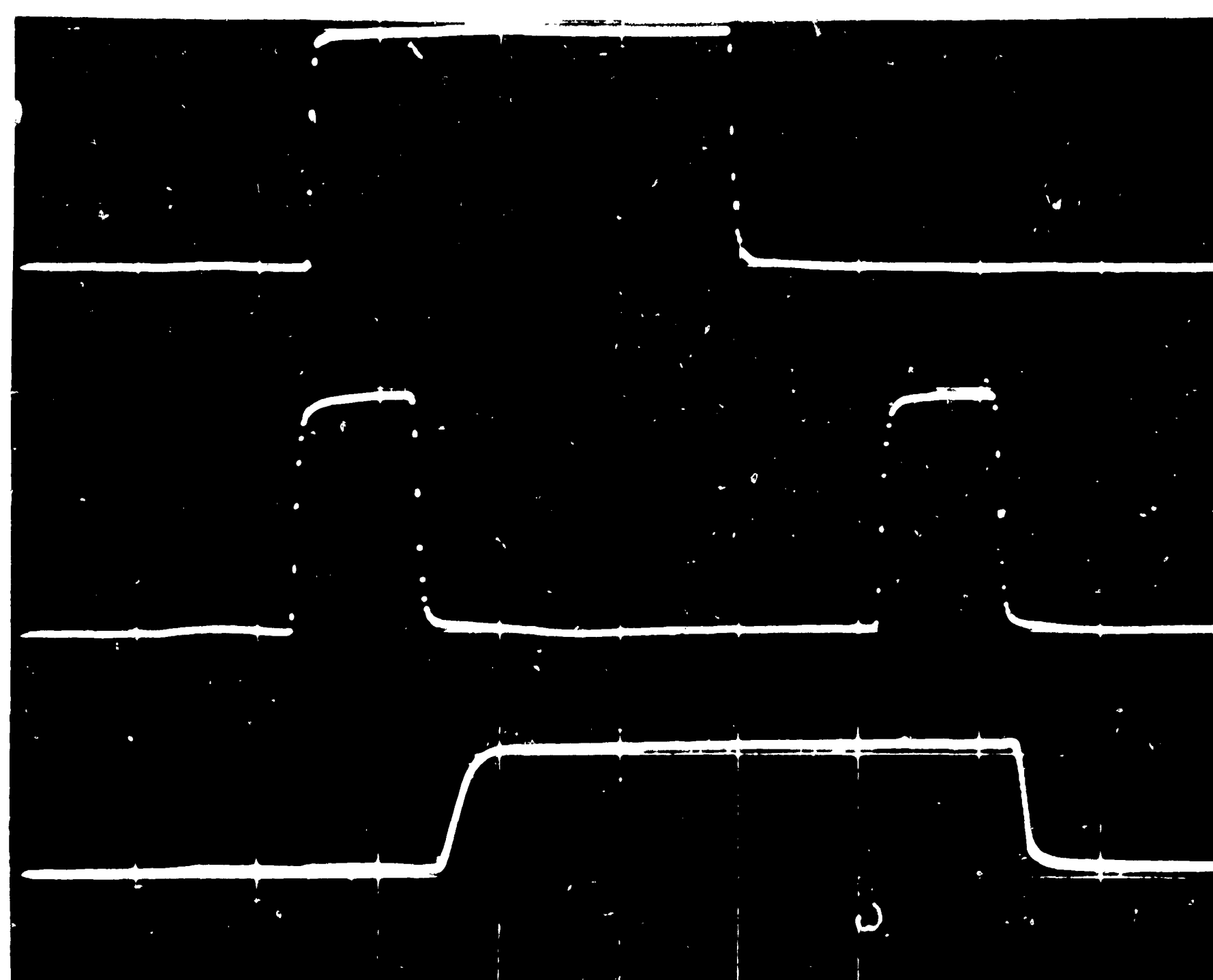
CONDITION 2

	25°C	-55°C	+125°C
T_1	5.45	5.0	7.73
T_1'	2.1	4.4	1.0
T_o	5.9	4.9	8.1
T_o'	0	2.4	1.0

The table of data is an average of 2 readings for each temperature and read at test circuit input.

NOTE: All readings in nanoseconds

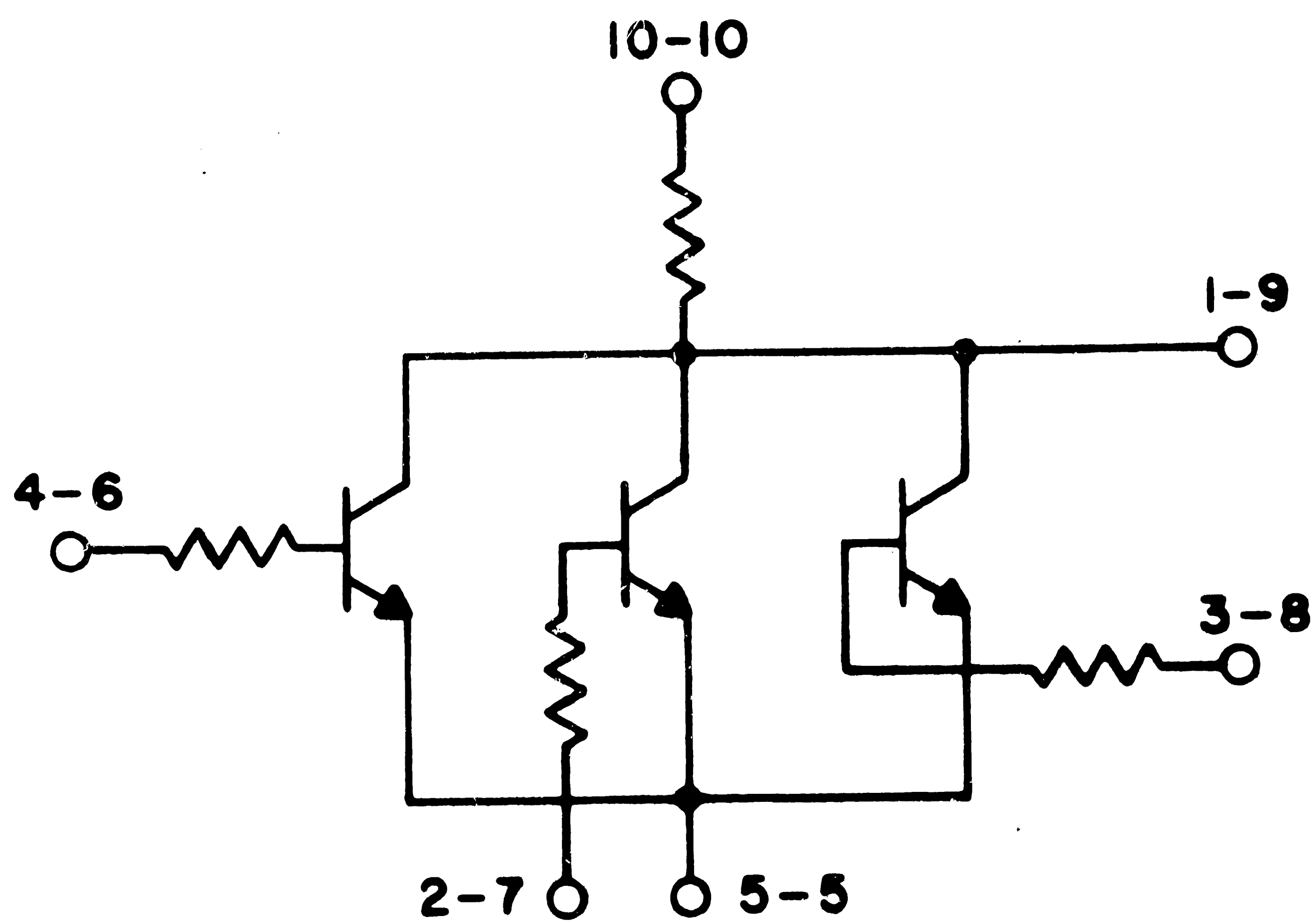
	TEST CKT INPUT CLOCK	TEST CIRCUIT OUTPUTS FOR TEMPERATURES OF				
		25°C	-40°C	-55°C	+85°C	+125°C
Amplitude	3.0	1.03	1.14	1.16	0.94	0.85
Pulse Width	200.	992.	994.	995.	983.	984.
T _r	18.	56.	58.	58.	56.	57.
T _f	19.	37.	45.	48.	42.	48.
T _d		48.	50.	52.	50.	50.
T _s		42.	46.	49.	42.	45.
T _{pd}		56.	64.	68.	56.	59.



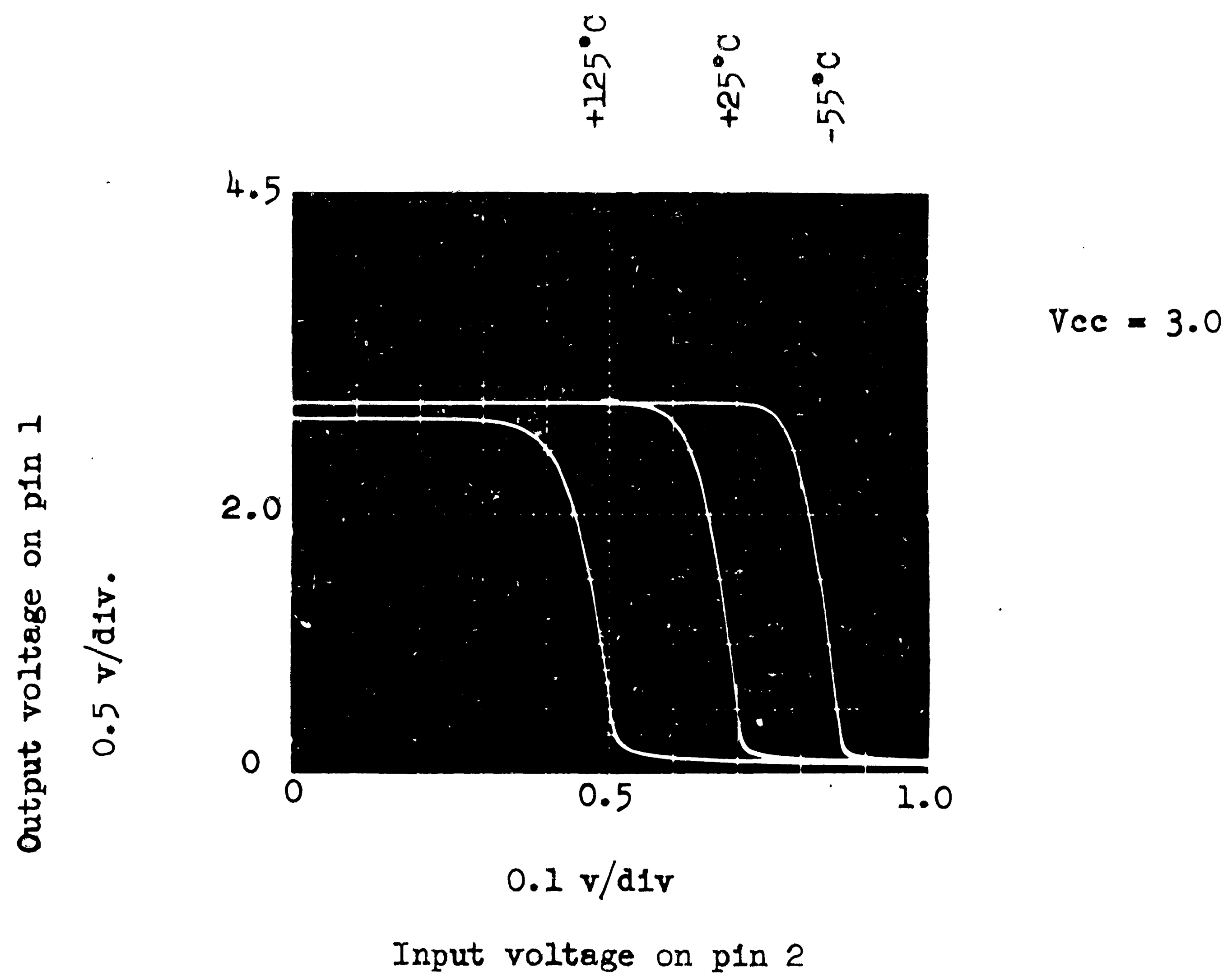
INPUT D₀

INPUT CLOCK \overline{CP}

OUTPUT D₁

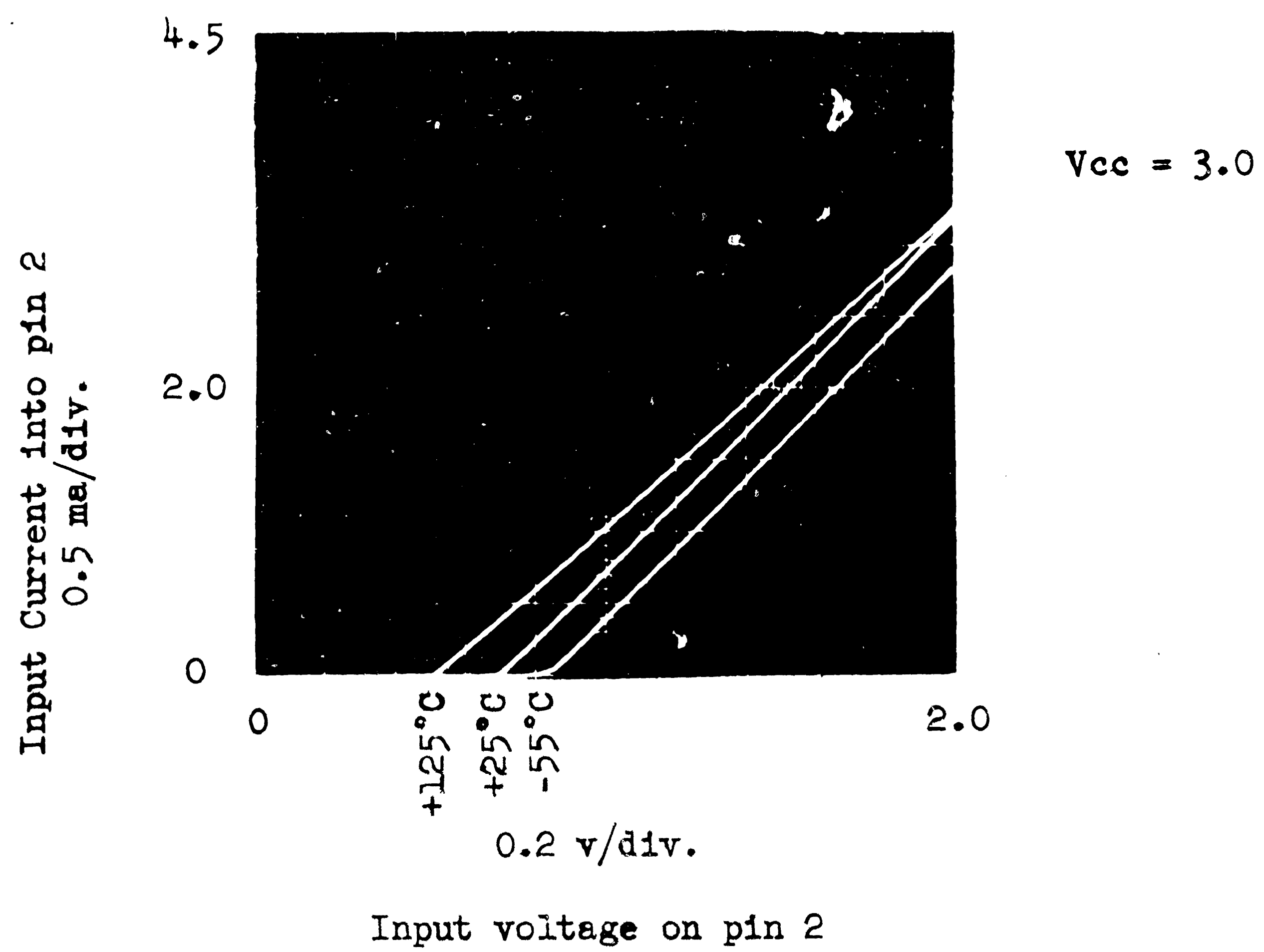


DUAL 3 - INPUT DCTL HIGH POWER GATE ELEMENT



INPUT OUTPUT CHARACTERISTICS

RTL 153D₃

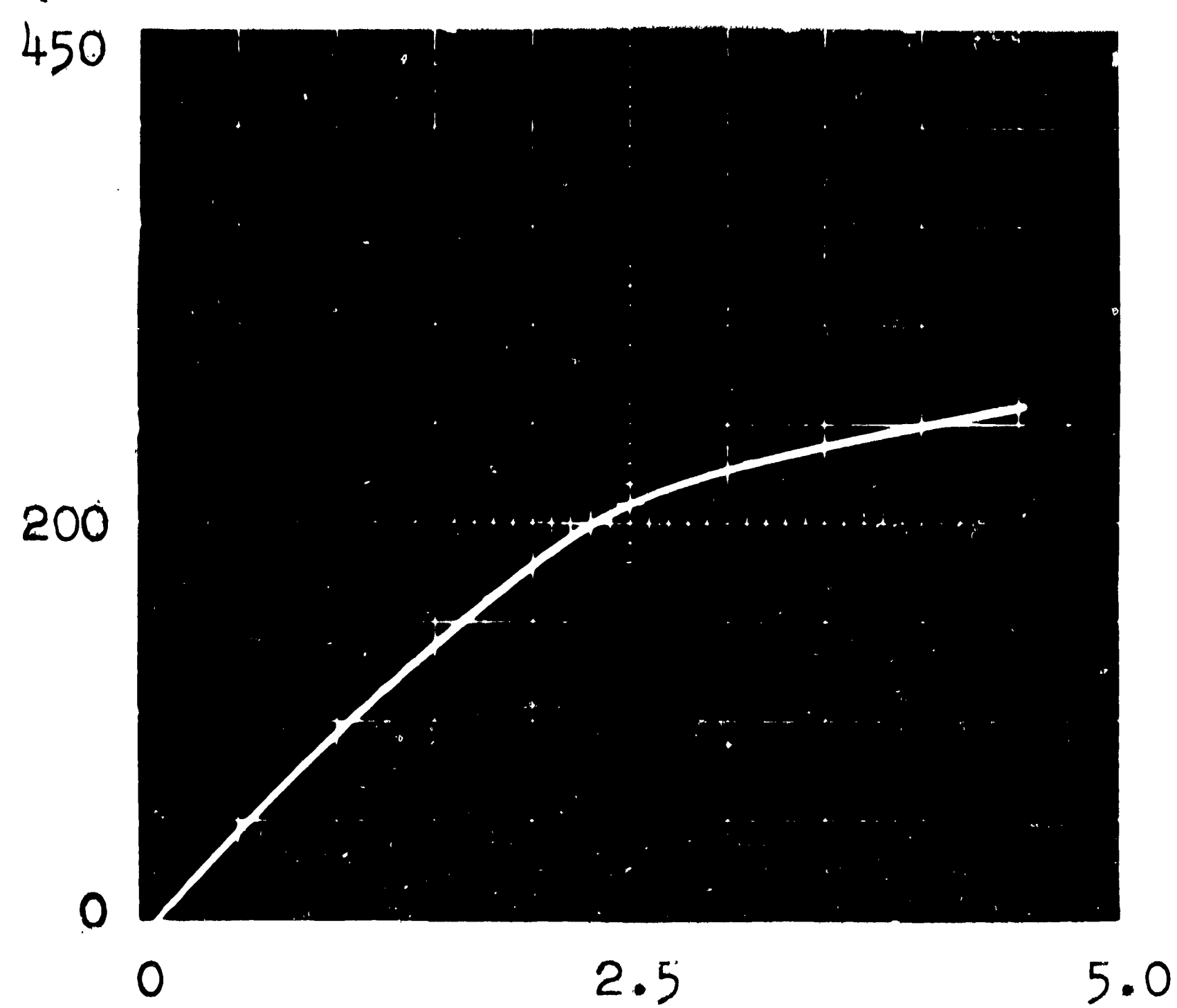


INPUT CHARACTERISTICS

RTL 153D₃

Output current into pin 1

50 ma/div.



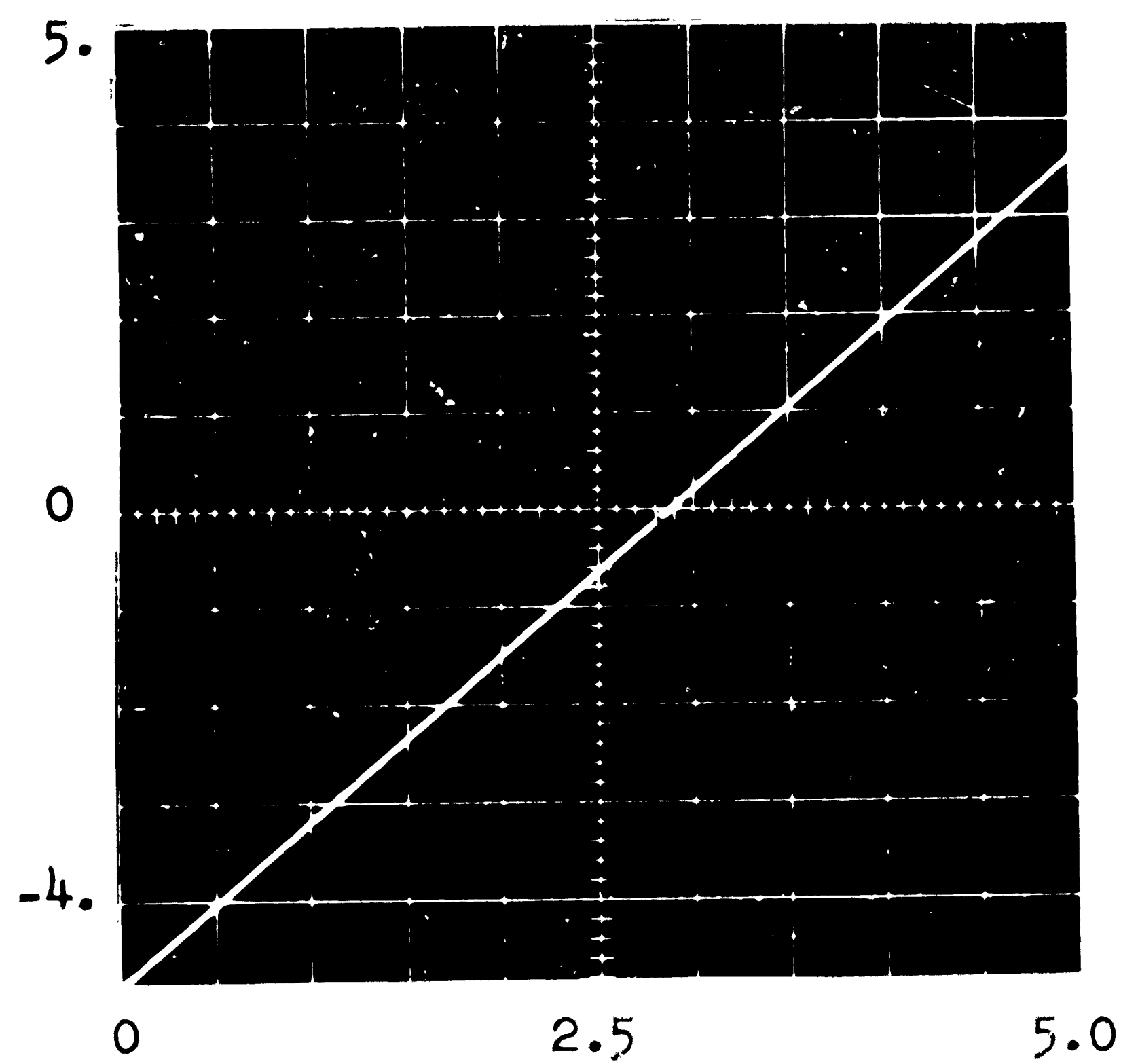
Vcc = 3.0
"1" on pin 2

0.5 v/div.

Output voltage on pin 1

Output current into pin 1

1 ma/div.



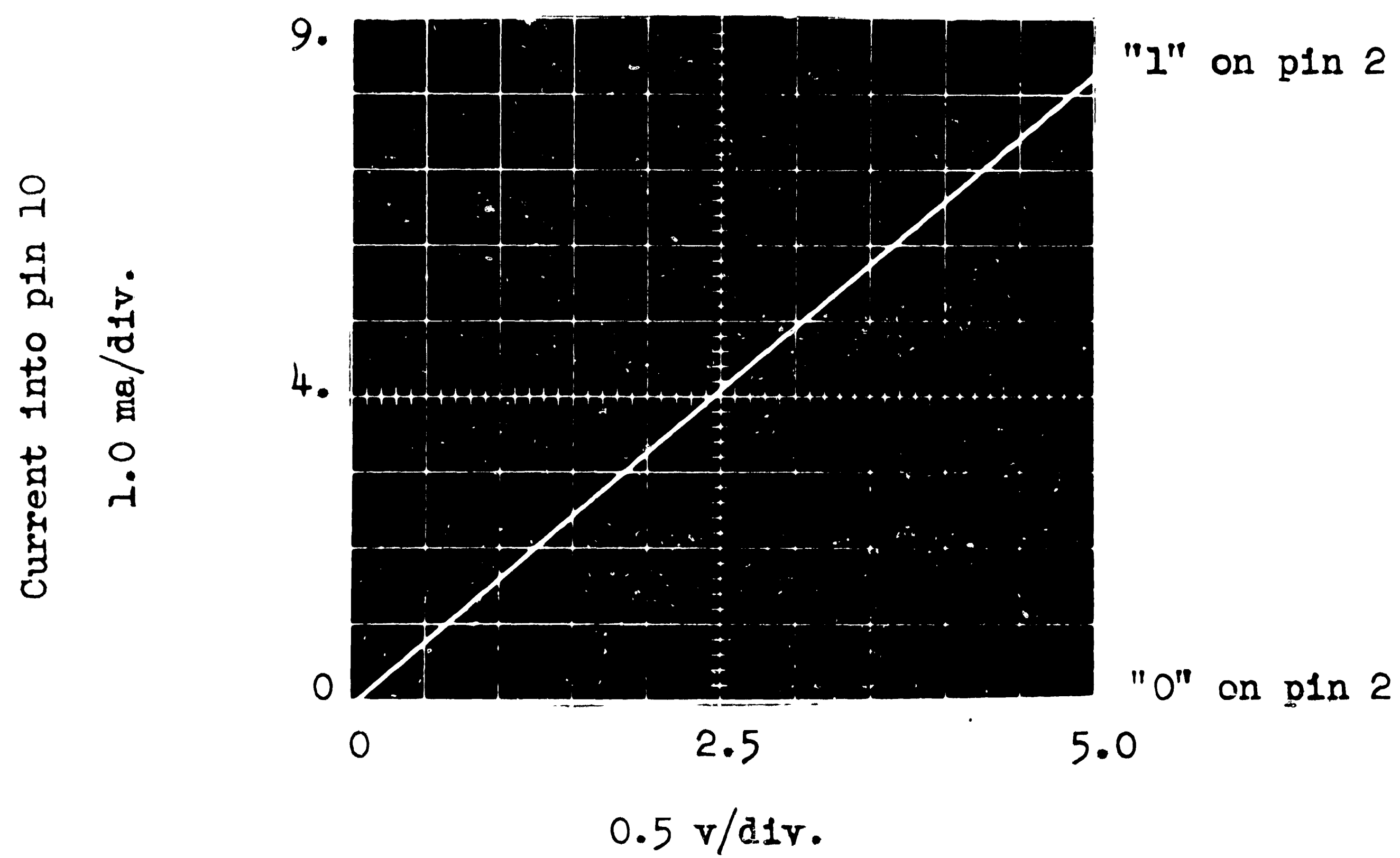
Vcc = 3.0
"0" on pin 2

0.5 v/div.

Output voltage on pin 1

OUTPUT CHARACTERISTICS
RTL 153D₃

3.2.90



Supply voltage on pin 10

POWER DISSIPATION CURVES

RTL 153D₃

EVALUATION

The General Microelectronic DTL line is a family of monolithic, planar, epitaxial devices consisting of five DTL circuits and two diode AND Gates.

DTL 254G4 and 254G3 are identical DTL NAND/NOR Gates with the exception that 254G4 has an additional input diode. Both are provided with an optional internal pull-up resistor which may or may not be used according to the application. They also have an extra input terminal (without the input diode) to allow additional AND Gating or to permit OR-diode gating.

DTL 264P is a NAND/NOR Gate similar to the 254G3 except no pull-up resistor is provided and this circuit has higher dc fan-out capabilities.

DTL 264D2 is a Dual 2 input DTL NAND/NOR gate with a pull-up resistor provided. There are no spare inputs provided on this circuit. The circuit will generate the exclusive OR function when pins 2 and 10 are tied together.

DTL 264B is a DTL set reset flip-flop with provisions for clock operation. The circuit was designed for ripple counting and shifting. The clock pulse, when operating in the clock mode, must have a fall time described by:

$$\frac{T_F}{V_{CP}} = < 50 \frac{\text{nSec}}{\text{volt}}$$

where T_F is fall time
and V_{CP} is the clock pulse amplitude

Also, the minimum clock pulse width is determined by the time constant of the charging circuit which is influenced by the fan-out of the gate driving the clocked set (or reset) inputs and the output impedance of the clock driver.

The output are buffered for high d-c fan out and driving of capacitive loads. This element can be used in either double or single power supply systems.

The truth table for the 264B for positive logic is:

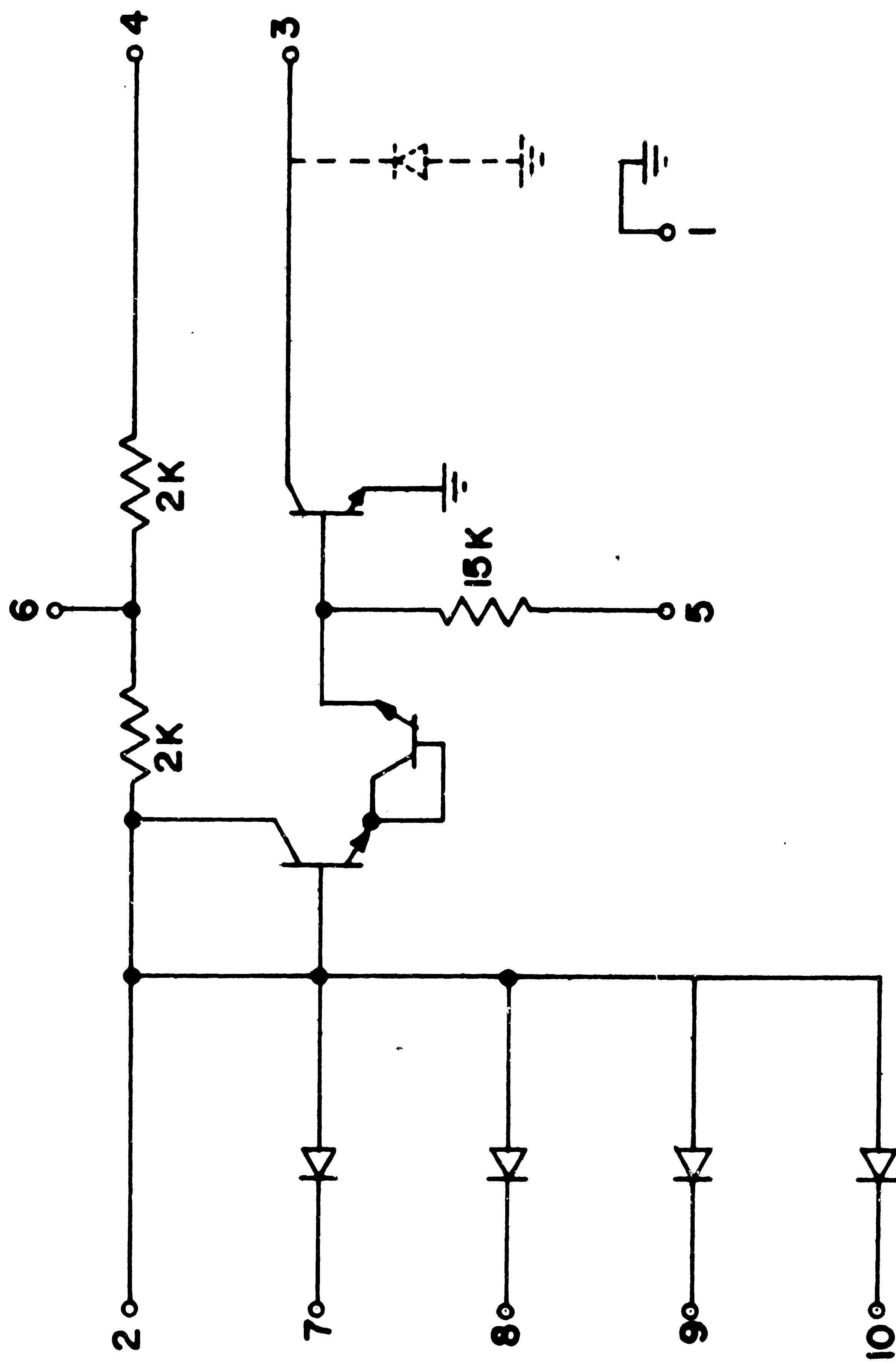
CLOCKED		SET-RESET	DIRECT SET		RESET	
S_c	R_c	Q	S_d	R_d	Q	\overline{Q}
0	0	?	0	0	*	1
0	1	1	0	1	1	0
1	0	0	1	0	0	1
1	1	No Change	1	1	No Change	

DTL 254G6 and DTL 254D3 are Diode AND Gates; the 254G6 is designed to be used as a 6 input AND Gate but the supply resistor is not connected internally to the output terminal. The 254D3 is a Dual 3-input Diode AND Gate with the supply connected internally to the output pin.

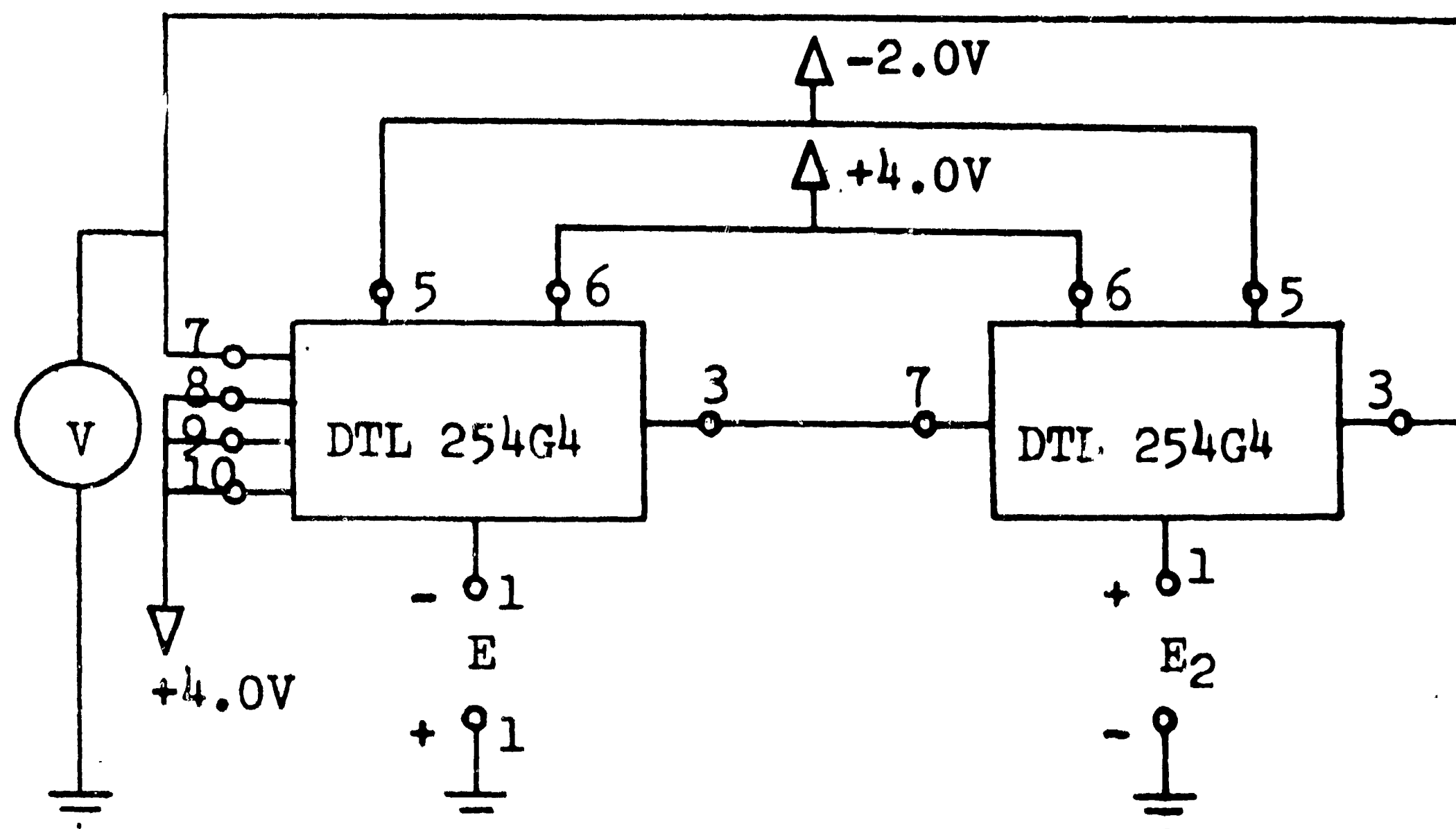
All circuits with the exception of the 254G3 were tested statically on a transistor curve tracer.

DYNAMIC TEST PROCEDURE

1. The block diagram for each test precedes the data for that circuit.
2. The temperature was regulated at 25°C the pulse repetition rate was set at 1 MC with a pulse width of 500 ns. The supply voltages for the 254G4 and 264B were set at: $V_6 = +4.0$, $V_5 = -2.0$. The load for the 254G4 and 264B was 1.
3. Data was taken for the 254D3 at supply voltages of 3.0V, 4.0V and 5.0V with a load of 1.
4. The above was repeated for temperatures of -40°C, -55°C, +85°C and +125°C.
5. The above was repeated for varying loads of 3 and 5 for the 254G4 and the 254D3.



254G4 4-INPUT DTL NOR GATE



NOISE TEST

PROCEDURE:

1. The circuits were connected as in the above block diagram.
2. E_2 was replaced by a short.
3. E_1 was increased until V indicated a change of state.
4. The system was reset by opening the negative terminal of E_1 which set V to zero.
5. E_1 was replaced by a short.
6. E_2 was increased until V indicated a change of state.
7. The system was reset by disconnecting E_1 's short which set V to zero.

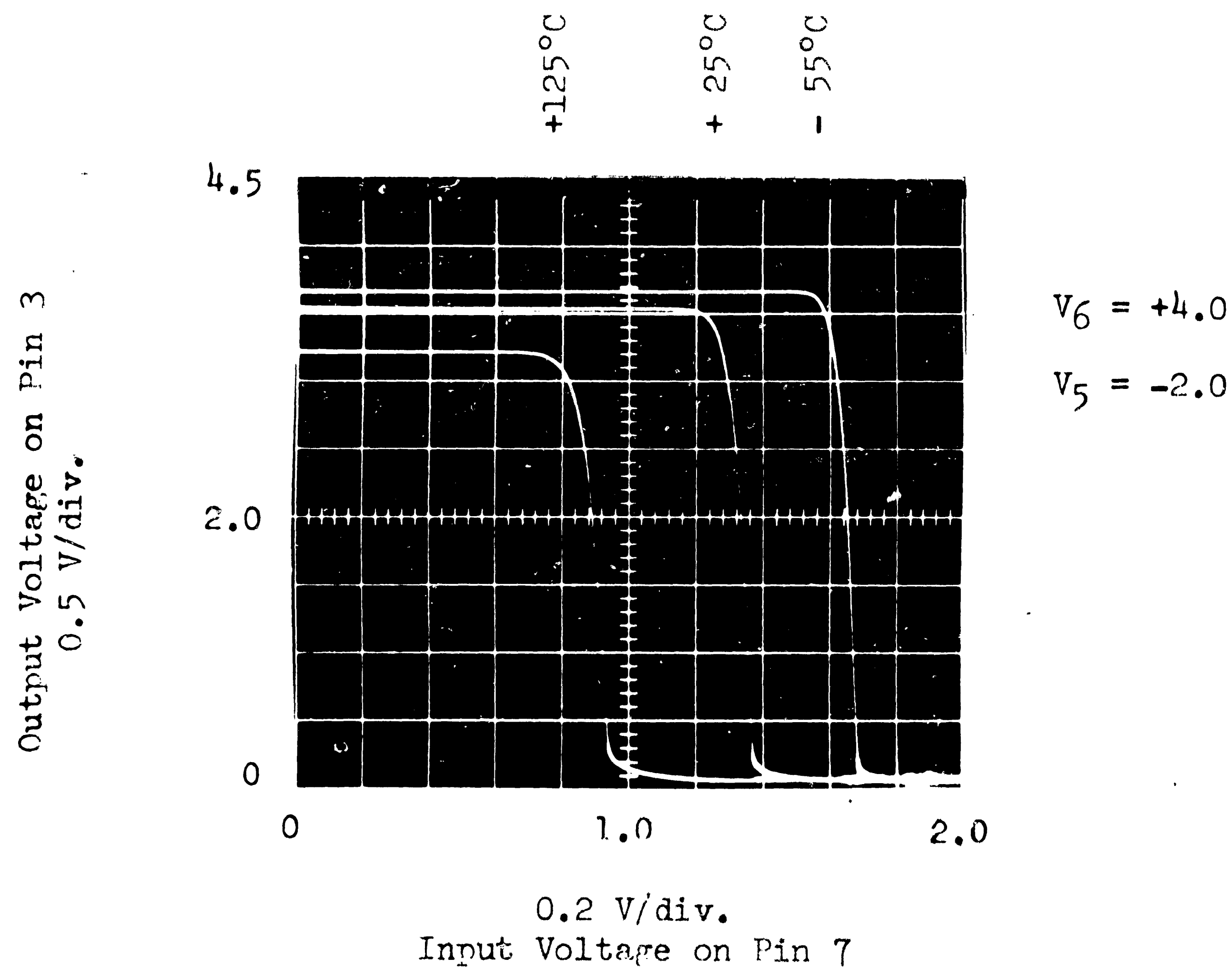
DATA:

The average of five test runs was:
 E_1 at system change of state -1.208
 E_2 at system change of state +1.18

The noise margin of the DTL elements used was 1.18 V.

EQUIPMENT:

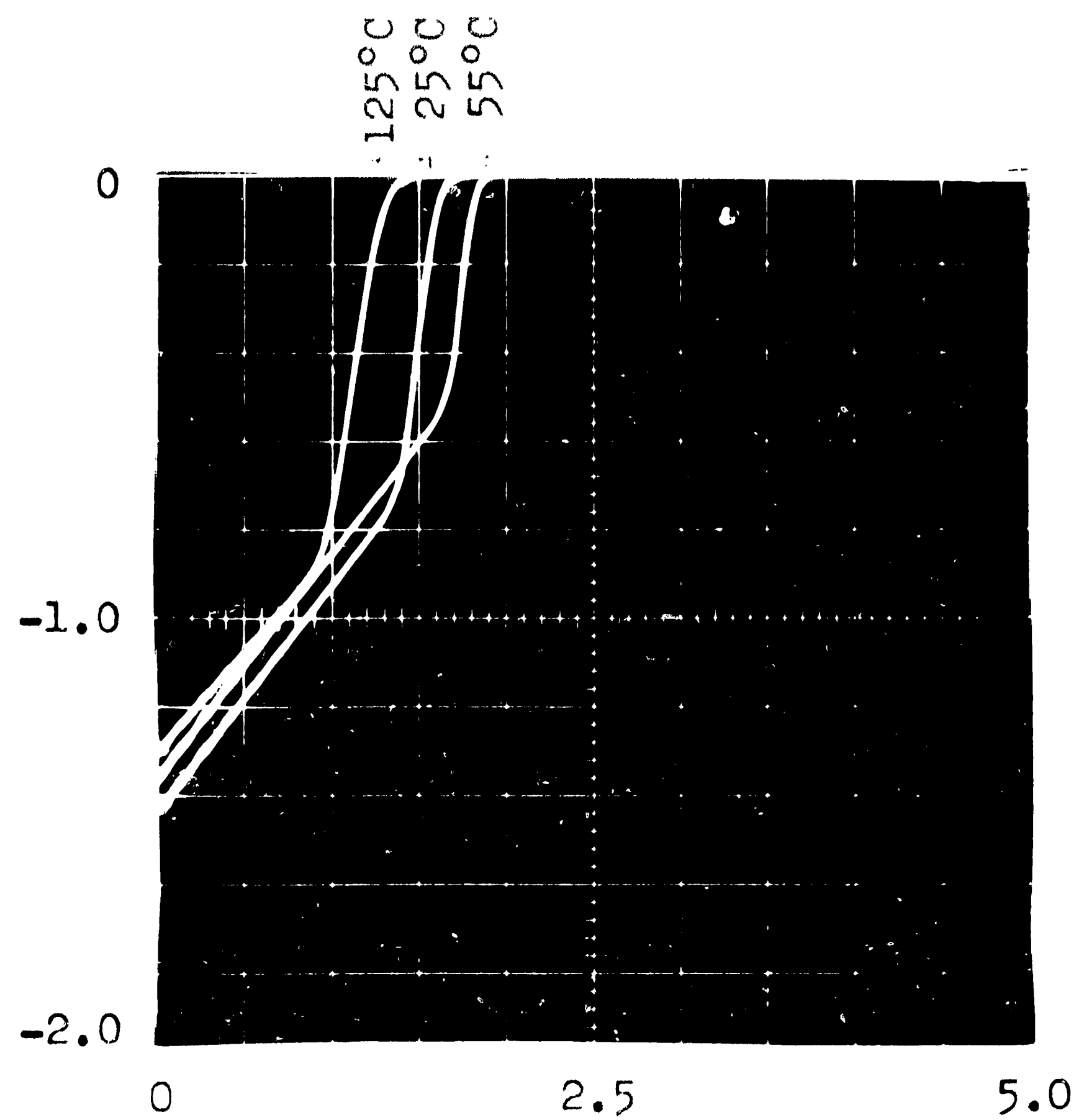
Voltmeter; Hewlett Packard, Model 412A
 Power Supplies; Harrison Laboratories, Model 6204A
 E_1 and E_2 ; Harrison Laboratories, Model 865B



NOTE: All curve tracer tests for this circuit were performed with the pull-up resistor provided internally.

INPUT - OUTPUT CHARACTERISTICS
DTL 254C4

Current into Pin 7
0.2 ma/div.

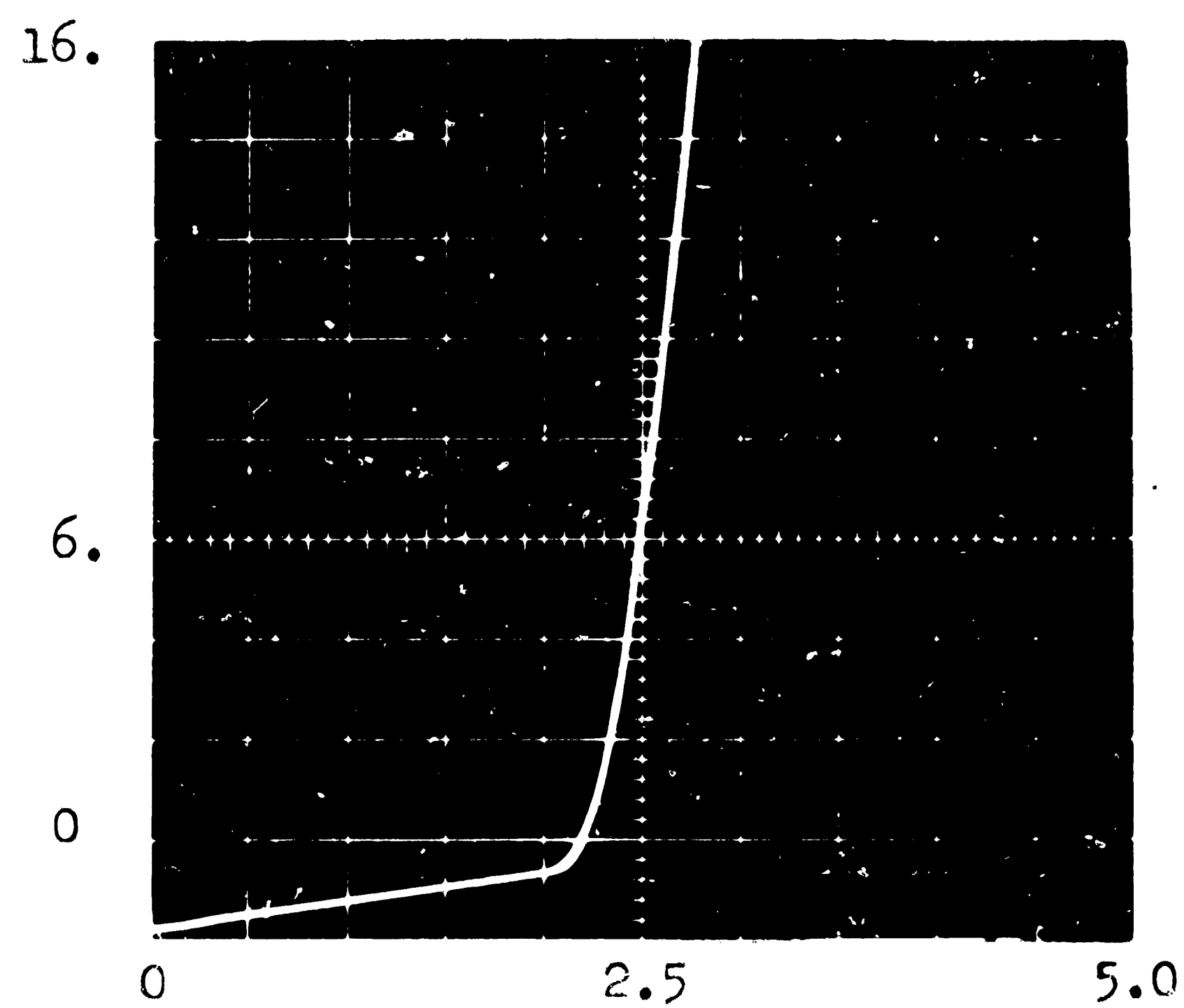


$V_6 = +4.0$

$V_5 = -2.0$

0.5 V/div.
Input Voltage on Pin 7

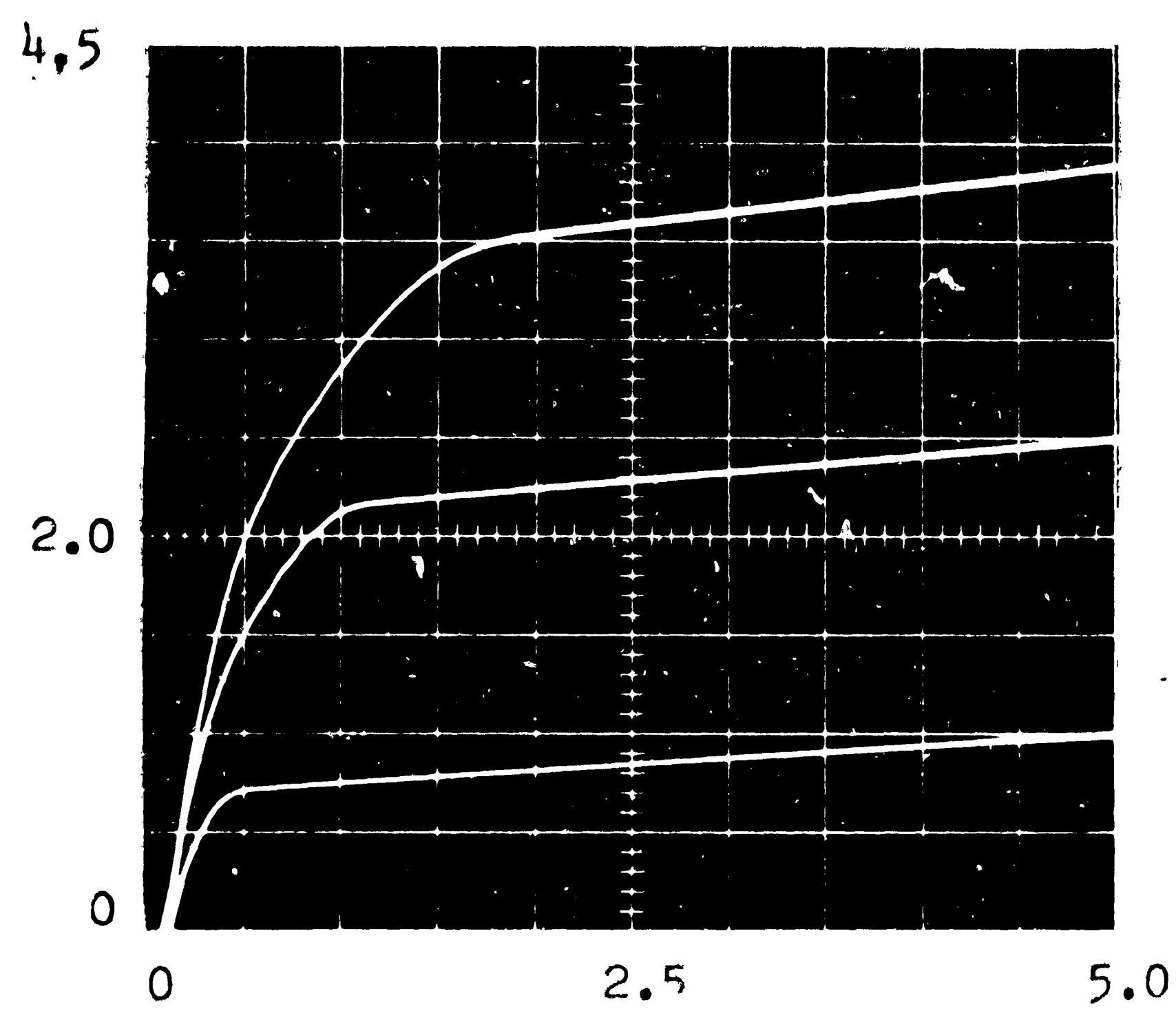
Current into Pin 2
2.0 ma/div.



0.5 V/div.
"Direct" Input Voltage on Pin 2
(No input diode)

INPUT CHARACTERISTICS
DTL 254G4

Output Current into Pin 3
5.0 ma/div.



$V_5 = -2.0$

$V_6 = +5.0$

$V_6 = +4.0$

$V_6 = +3.0$

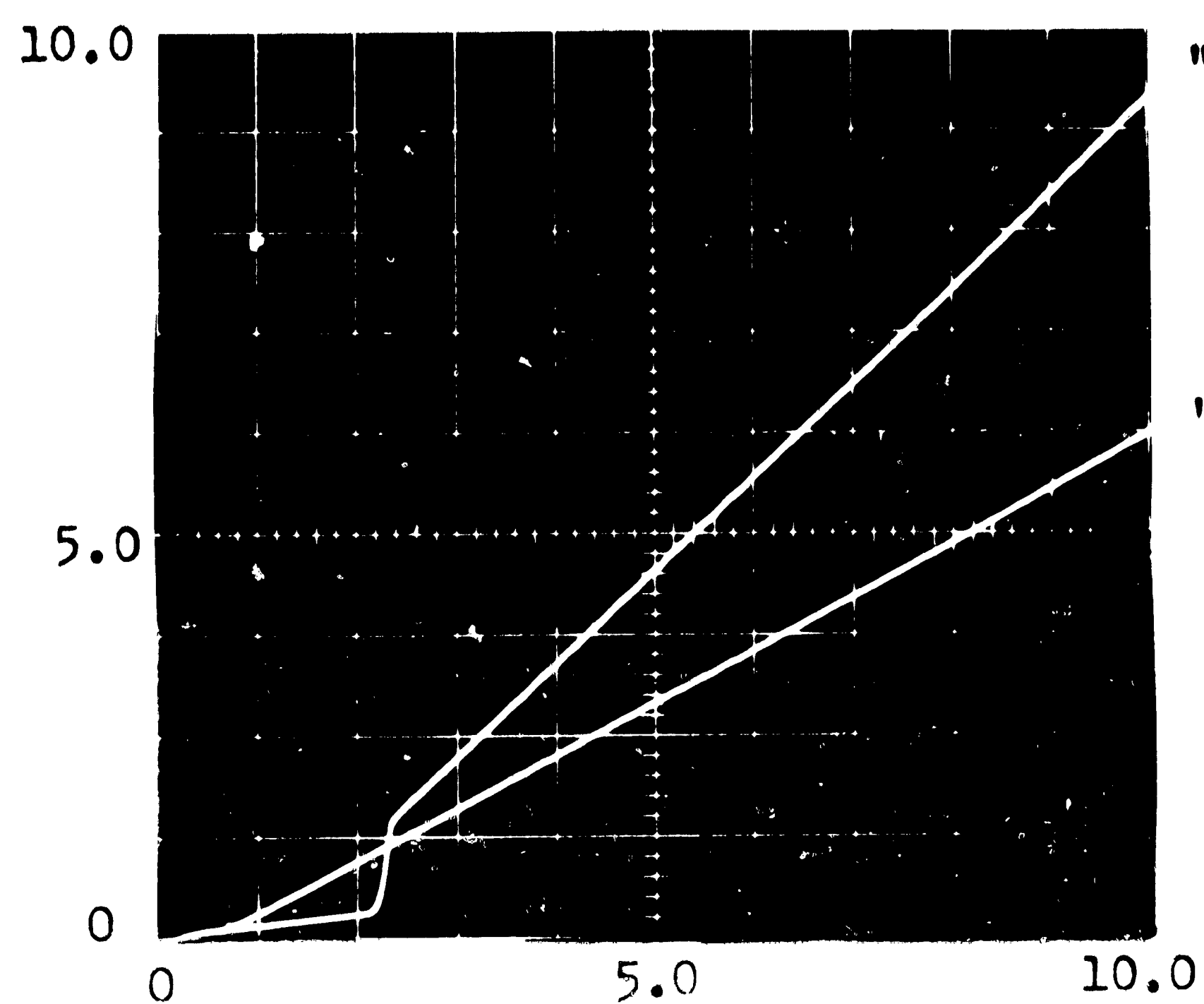
0.5 V/div.

Output Voltage on Pin 3

OUTPUT CHARACTERISTICS
DTL 254G4

3.2.98

Current into Pin 6
1.0 ma/div.

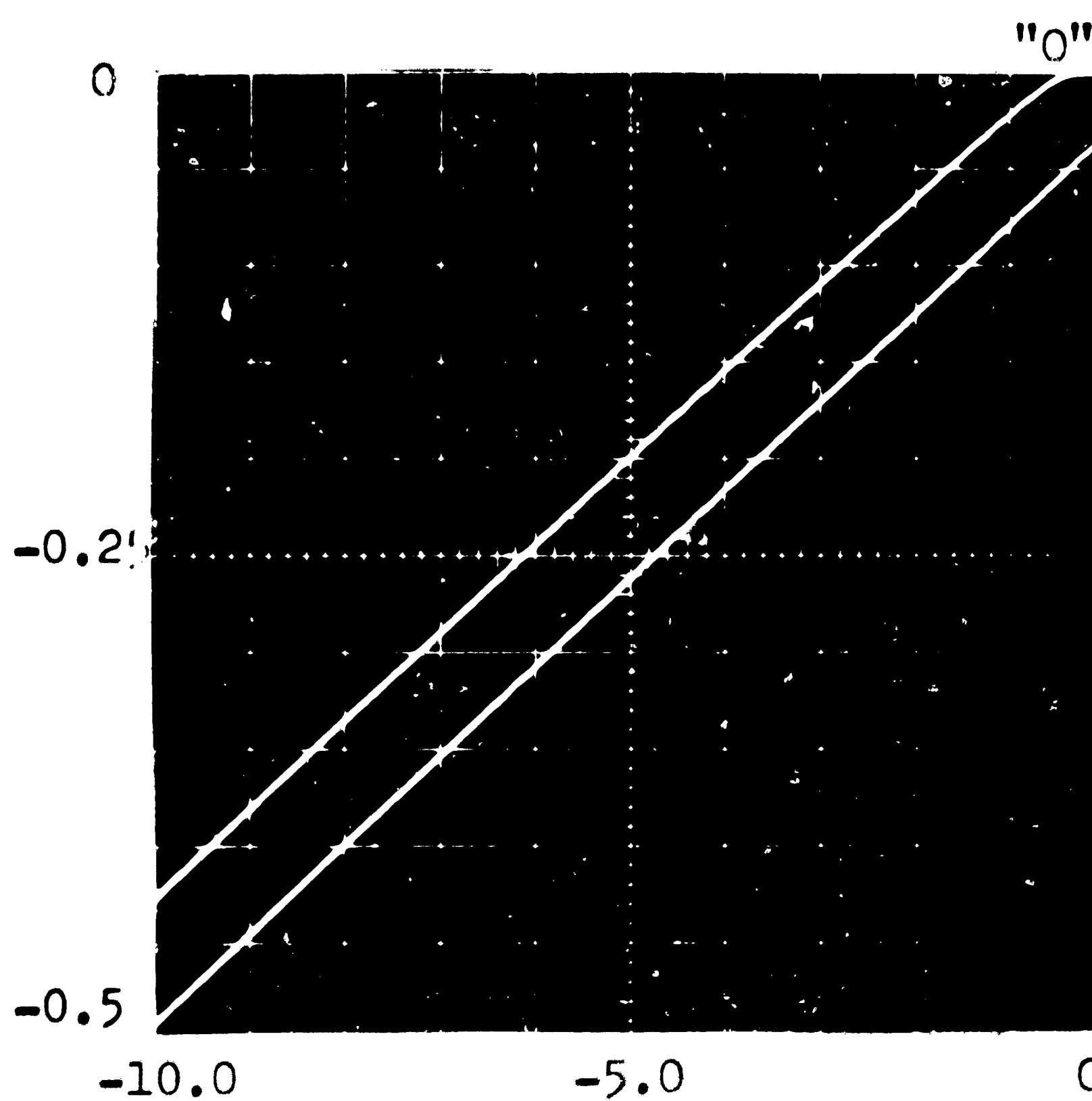


"1" on Pin 7
 $V_5 = -2.0$

"0" on Pin 7

1.0 V/div.
Supply Voltage on Pin 6

Current into Pin 5
0.05 V/div.



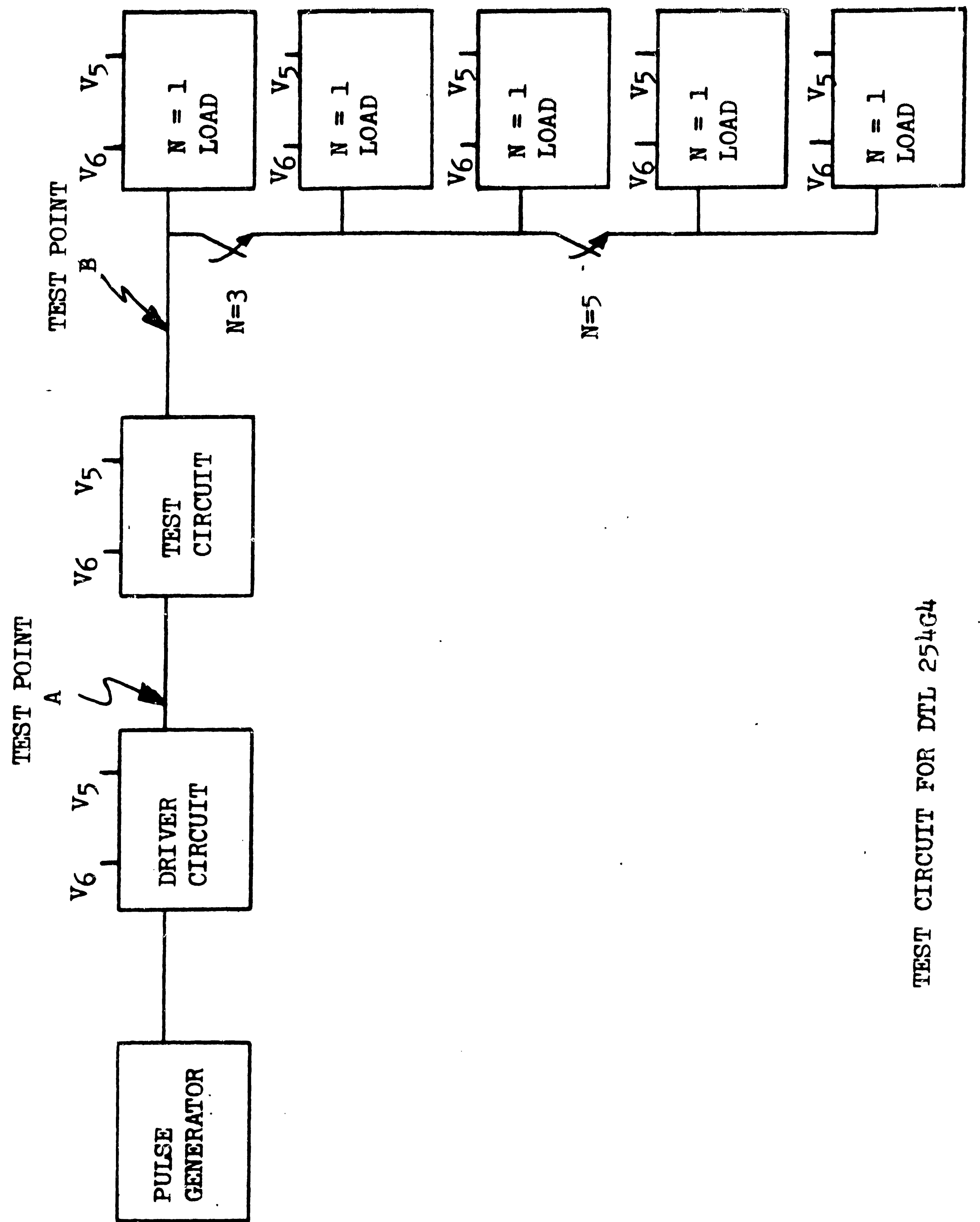
"0" on Pin 7

"1" on Pin 7

$V_6 = +4.0$

1.0 V/div.
Supply Voltage on Pin 5

POWER DISSIPATION CURVES
DTL 254G4

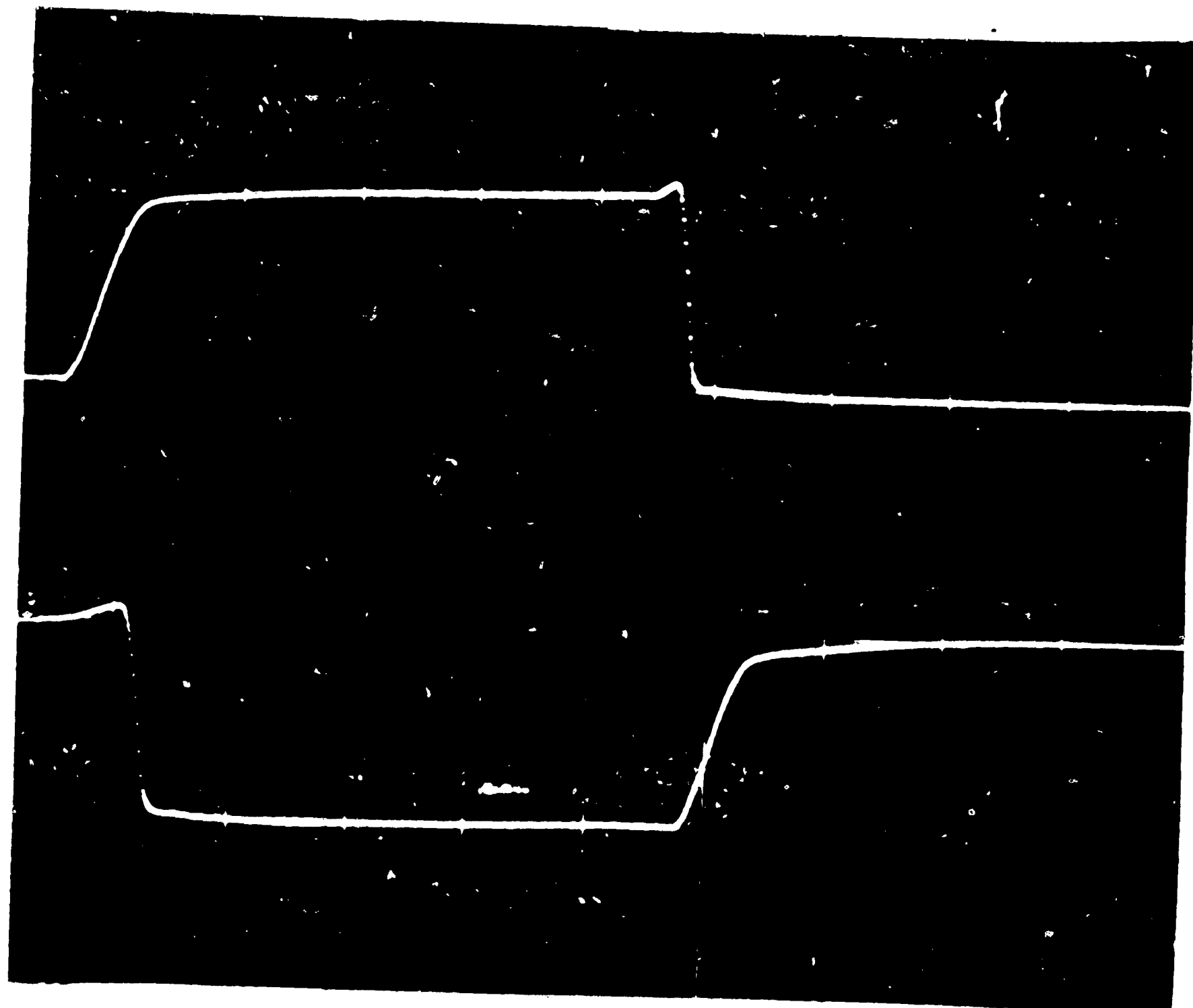


TEST CIRCUIT FOR DTL 254G4

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. +25°C V6 +4.0 V5 -2.0 N = 1

	TEST CKT. INPUT	TEST CKT. OUTPUT
		V6 <u>+4.0</u>
		V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>500.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.70</u>	<u>1.68</u>
T _r	<u>56.</u>	<u>60.</u>
T _f	<u>13.</u>	<u>16.</u>
T _d		<u>50.</u>
T _s		<u>17.</u>
T _{pd}		<u>34.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. -40°C V6 +4.0 V5 -2.0 N = 1

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>+4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>478.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.84</u>	<u>1.86</u>
T _r	<u>58.</u>	<u>55.</u>
T _f	<u>16.</u>	<u>19.</u>
T _d		<u>60.</u>
T _s		<u>12.</u>
T _{pd}		<u>36.</u>

Type DTL No. 254G4 Temp. -55 V6 +4.0 V5 -2.0 N = 1

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>+4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>471.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.89</u>	<u>1.90</u>
T _r	<u>59.</u>	<u>57.</u>
T _f	<u>18.</u>	<u>21.</u>
T _d		<u>64.</u>
T _s		<u>11.</u>
T _{pd}		<u>39.</u>

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. +85°C V6 +4.0 V5 -2.0 N = 1

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500</u>	<u>519</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.52</u>	<u>1.50</u>
T _r	<u>59.</u>	<u>70.</u>
T _f	<u>13.</u>	<u>15.</u>
T _d		<u>44.</u>
T _s		<u>27.</u>
T _{pd}		<u>36.</u>

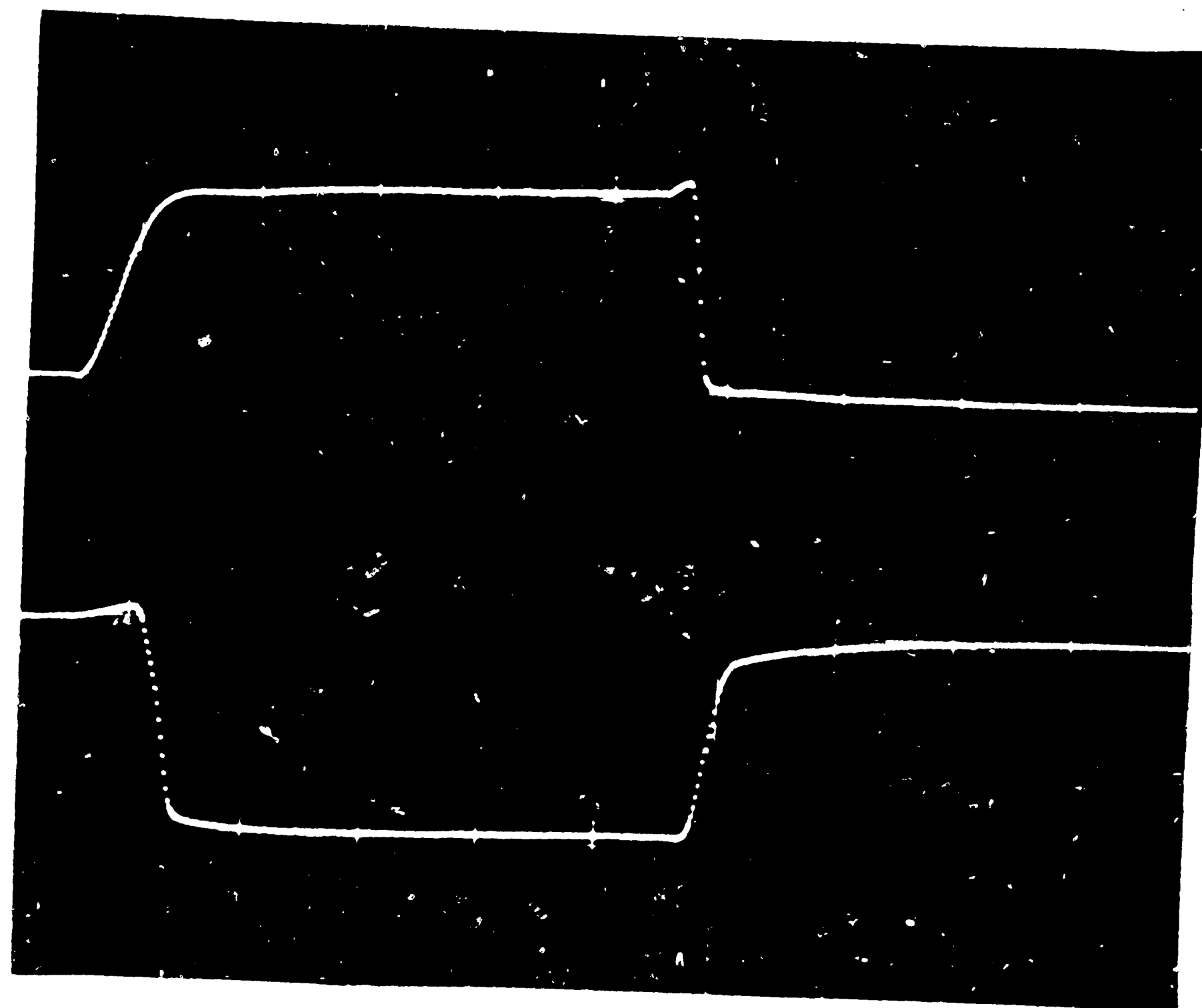
Type DTL No. 254G4 Temp. +125°C V6 4.0 V5 -2.0 N = 1

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>531.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.38</u>	<u>1.36</u>
T _r	<u>66.</u>	<u>76.</u>
T _f	<u>14.</u>	<u>16.</u>
T _d		<u>42.</u>
T _s		<u>35.</u>
T _{pd}		<u>39.</u>

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. +25°C V6 +4.0 V5 -2.0 N = 3

	TEST CKT. INPUT	TEST CKT. OUTPUT
		V6 <u>+4.0</u>
		V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>480.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.72</u>	<u>1.80</u>
T _r	<u>59.</u>	<u>52.</u>
T _f	<u>13.</u>	<u>25.</u>
T _d		<u>51.</u>
T _s		<u>12.</u>
T _{pd}		<u>30.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. -40°C V6 +4.0 V5 -2.0 N = 3

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>+4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>451.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.88</u>	<u>1.94</u>
T _r	<u>61.</u>	<u>36.</u>
T _f	<u>17.</u>	<u>35.</u>
T _d		<u>62.</u>
T _s		<u>8.</u>
T _{pd}		<u>36.</u>

Type DTL No. 254G4 Temp. -55°C V6 +4.0 V5 -2.0 N = 3

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>+4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>442.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.92</u>	<u>1.98</u>
T _r	<u>62.</u>	<u>35.</u>
T _f	<u>18.</u>	<u>39.</u>
T _d		<u>66.</u>
T _s		<u>7.</u>
T _{pd}		<u>40.</u>

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. +85°C V6 +4.0 V5 -2.0 N = 3

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>507.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.56</u>	<u>1.62</u>
T _r	<u>58.</u>	<u>65.</u>
T _f	<u>14.</u>	<u>22.</u>
T _d		<u>45.</u>
T _s		<u>21.</u>
T _{pd}		<u>32.</u>

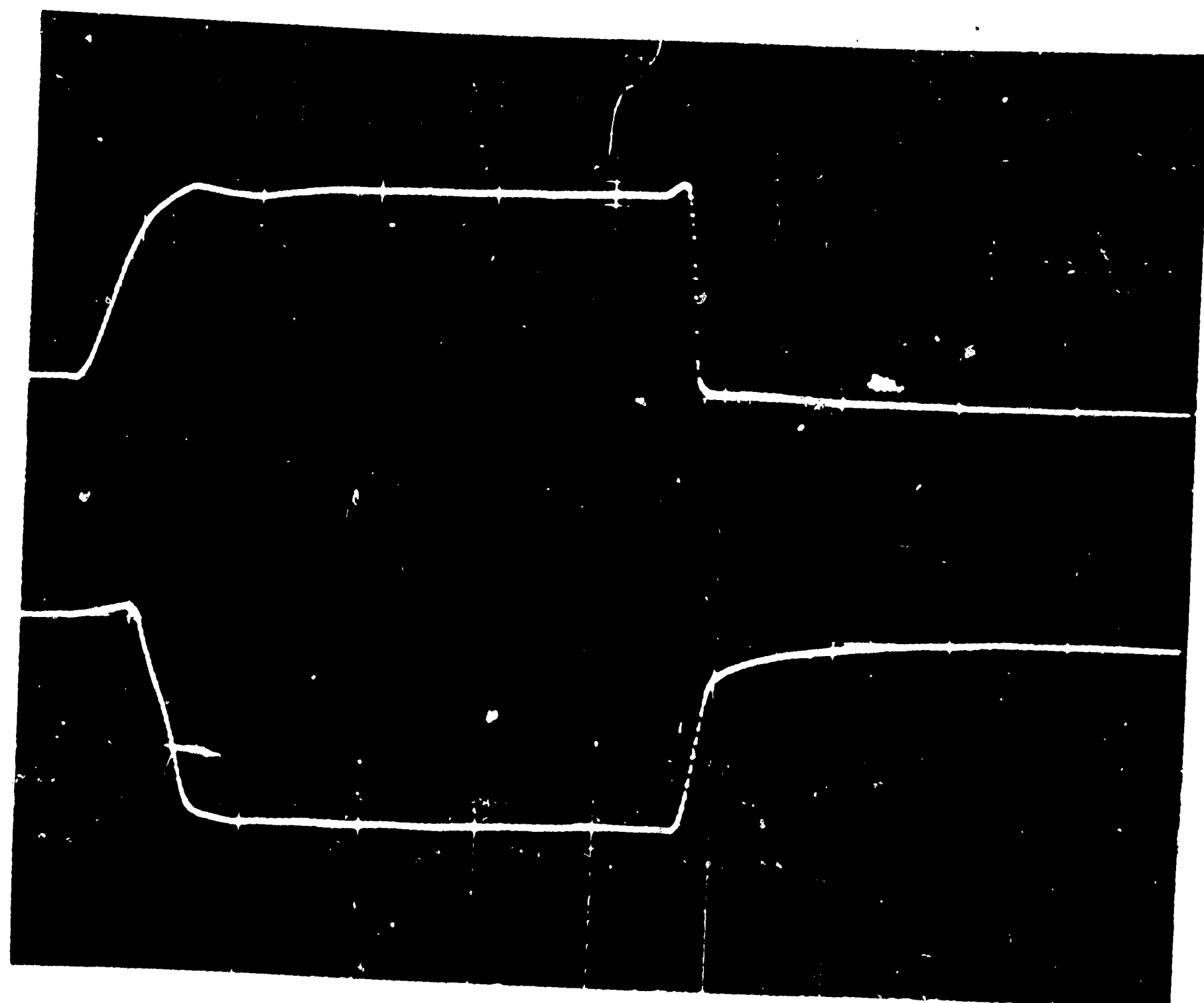
Type DTL No. 254G4 Temp +125°C V6 4.0 V5 -2.0 N = 3

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>515.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.42</u>	<u>1.50</u>
T _r	<u>62.</u>	<u>71.</u>
T _f	<u>14.</u>	<u>24.</u>
T _d		<u>43.</u>
T _s		<u>28.</u>
T _{pd}		<u>35.</u>

GENERAL MICRO-ELECTRONICS

Type DIL No. 254G4 Temp. +25°C V6 +4.0 V5 -2.0 N = 5

	TEST CKT. INPUT	TEST CKT. OUTPUT
		V6 <u>+4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>465.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.76</u>	<u>1.75</u>
T _r	<u>61.</u>	<u>70.</u>
T _f	<u>13.</u>	<u>43.</u>
T _d		<u>52.</u>
T _s		<u>9.</u>
T _{pd}		<u>34.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. -40°C V6 +4.0 V5 -2.0 N = 5

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>+4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>425.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.90</u>	<u>1.86</u>
T _r	<u>63.</u>	<u>56.</u>
T _f	<u>16.</u>	<u>57.</u>
T _d		<u>62.</u>
T _s		<u>5.</u>
T _{pd}		<u>45.</u>

Type DTL No. 254G4 Temp -55°C V6 +4.0 V5 -2.0 N = 5

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>+4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>411.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.94</u>	<u>1.83</u>
T _r	<u>64.</u>	<u>55.</u>
T _f	<u>18.</u>	<u>69.</u>
T _d		<u>67.</u>
T _s		<u>5.</u>
T _{pd}		<u>50.</u>

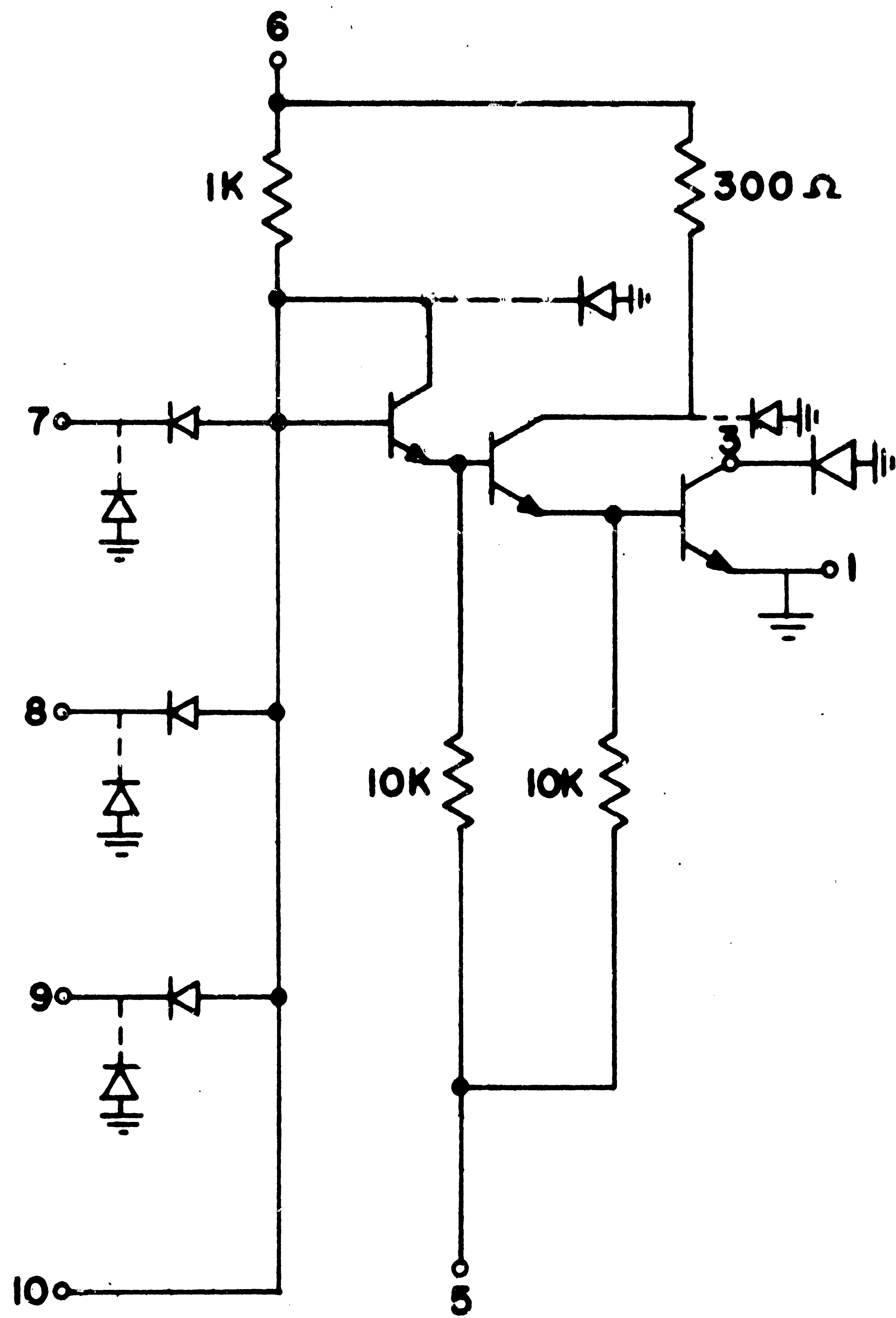
GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. +85°C V6 +4.0 V5 -2.0 N = 5

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>+4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>492.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.58</u>	<u>1.56</u>
T _r	<u>60.</u>	<u>78.</u>
T _f	<u>14.</u>	<u>46.</u>
T _d		<u>45.</u>
T _s		<u>16.</u>
T _{pd}		<u>31.</u>

Type DTL No. 254G4 Temp +125°C V6 +4.0 V5 -2.0 N = 5

	TEST CKT INPUT	TEST CKT OUTPUT V6 <u>+4.0</u> V5 <u>-2.0</u>
Pulse Width	<u>500.</u>	<u>505.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>1.44</u>	<u>1.44</u>
T _r	<u>62.</u>	<u>84.</u>
T _f	<u>14.</u>	<u>54.</u>
T _d		<u>43.</u>
T _s		<u>23.</u>
T _{pd}		<u>33.</u>



264P 3-INPUT DTL POWER NOR GATE

3.2.110

TABLE FOR PROPAGATION DELAY versus TEMPERATURE CURVE

(Temperature -°C)	$T_{pd} \text{ NS}^1$	Period-NS	$T_{pd} - \text{NS}^2$
-55	41	599	42.7
-40	40	614	43.9
+25	47	717	50.5
+85	58	905	64.6
+125	66	1000	71.4

TEST CONDITIONS: Nine DTL Power Gates Connected in a Ring Oscillator
 $V_6 = +4.0$ $V_5 = -2.0$ $V_1 = 0$

NOTES:

1. Measured as defined in data section:

$$T_{pd} = \frac{T_1 + T_2}{2}$$

T_1 = Time between 50% of input leading edge and 50% of output leading edge.

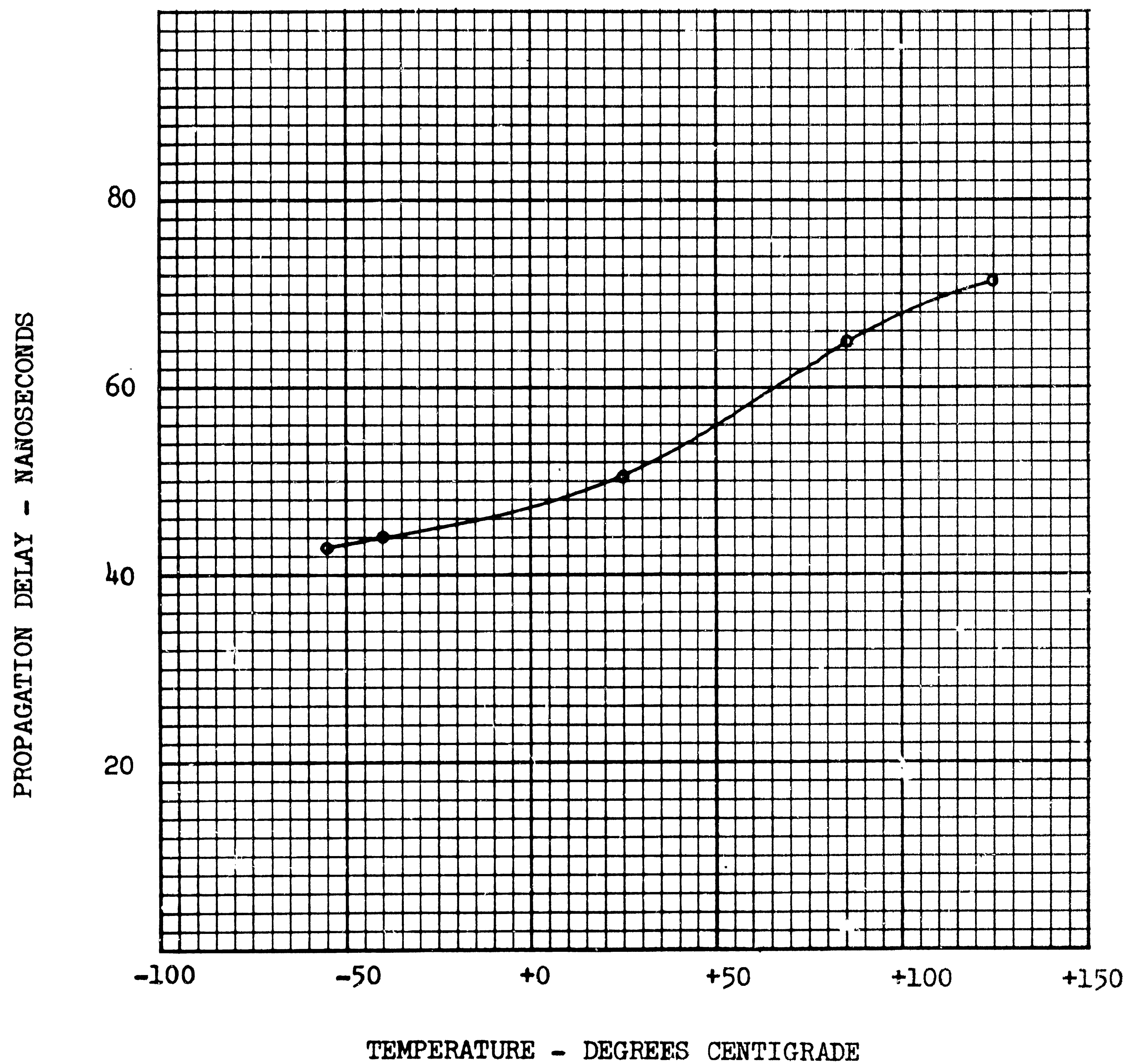
T_2 = Time between 50% of input trailing edge and 50% of output trailing edge.

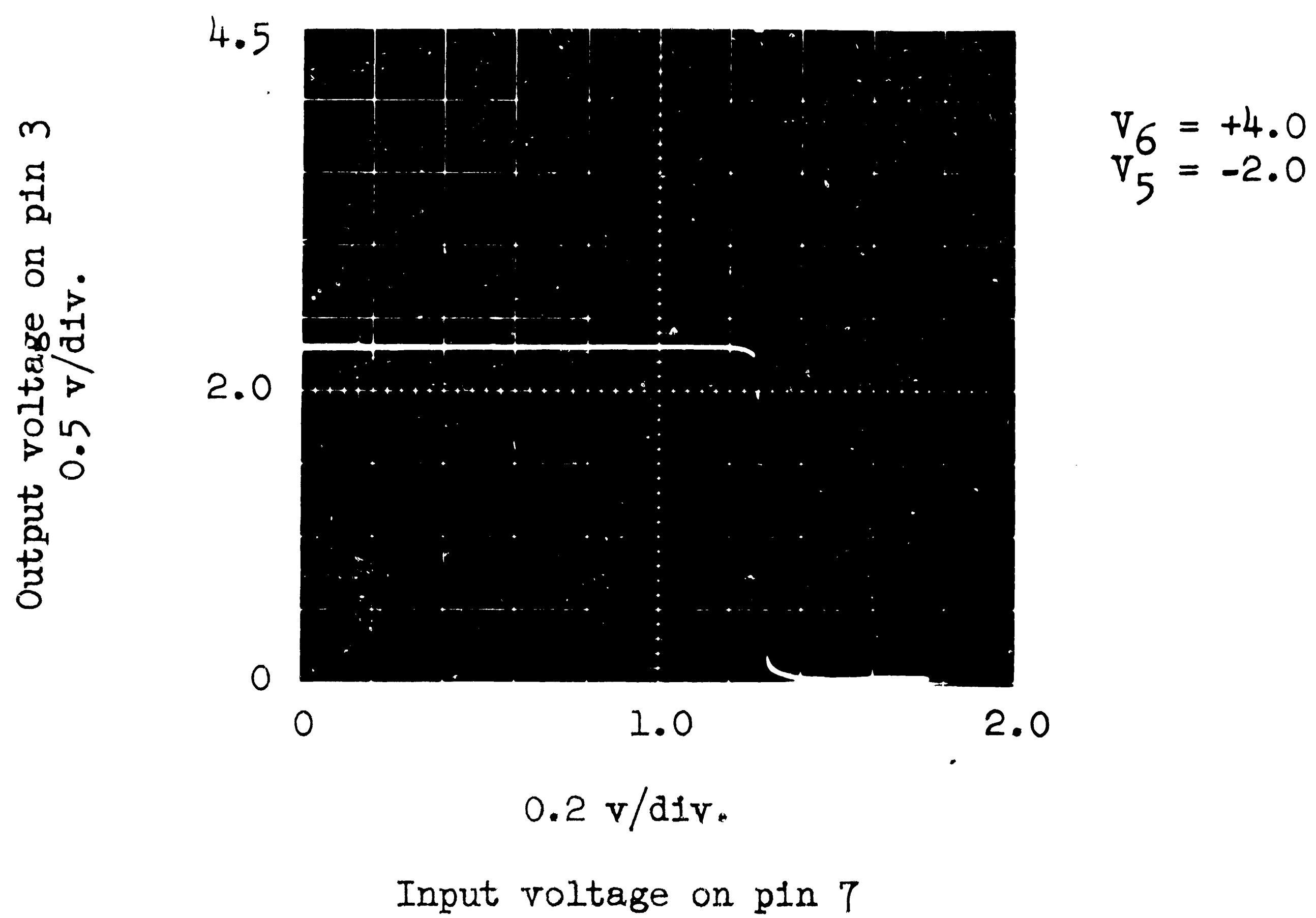
2. Defined as:

$$T_{pd} = \frac{\text{Period}}{2N}$$

N is total number of circuits in the ring oscillator.

PROPAGATION DELAY versus TEMPERATURE





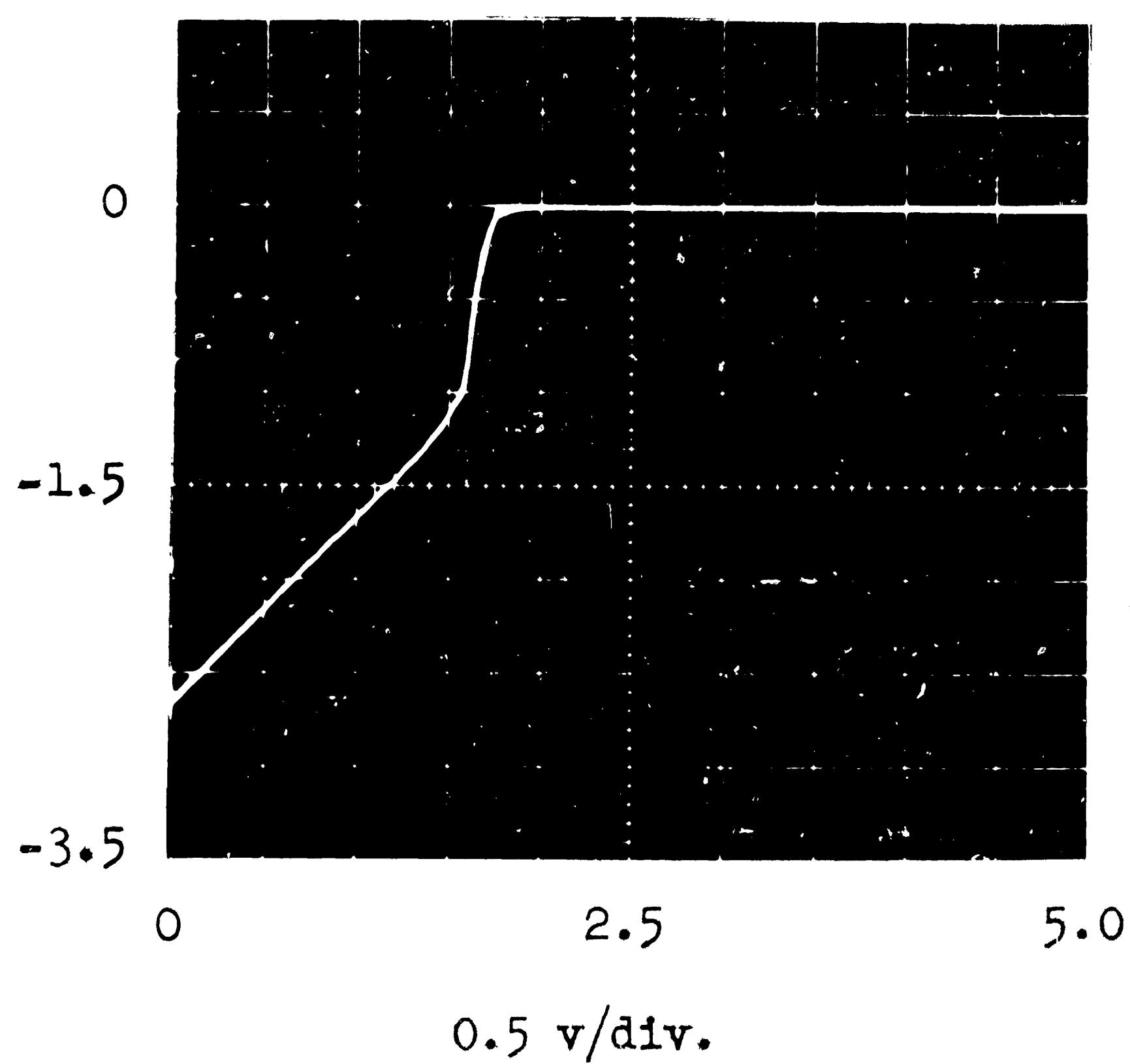
NOTE: The test gate was connected to drive the direct input of a similar gate for proper biasing conditions.

INPUT - OUTPUT CHARACTERISTICS

DTL - 264P

3.2.113

Input Current into pin 7
0.5 ma/div.



$V_6 = +4.0$
 $V_5 = -2.0$

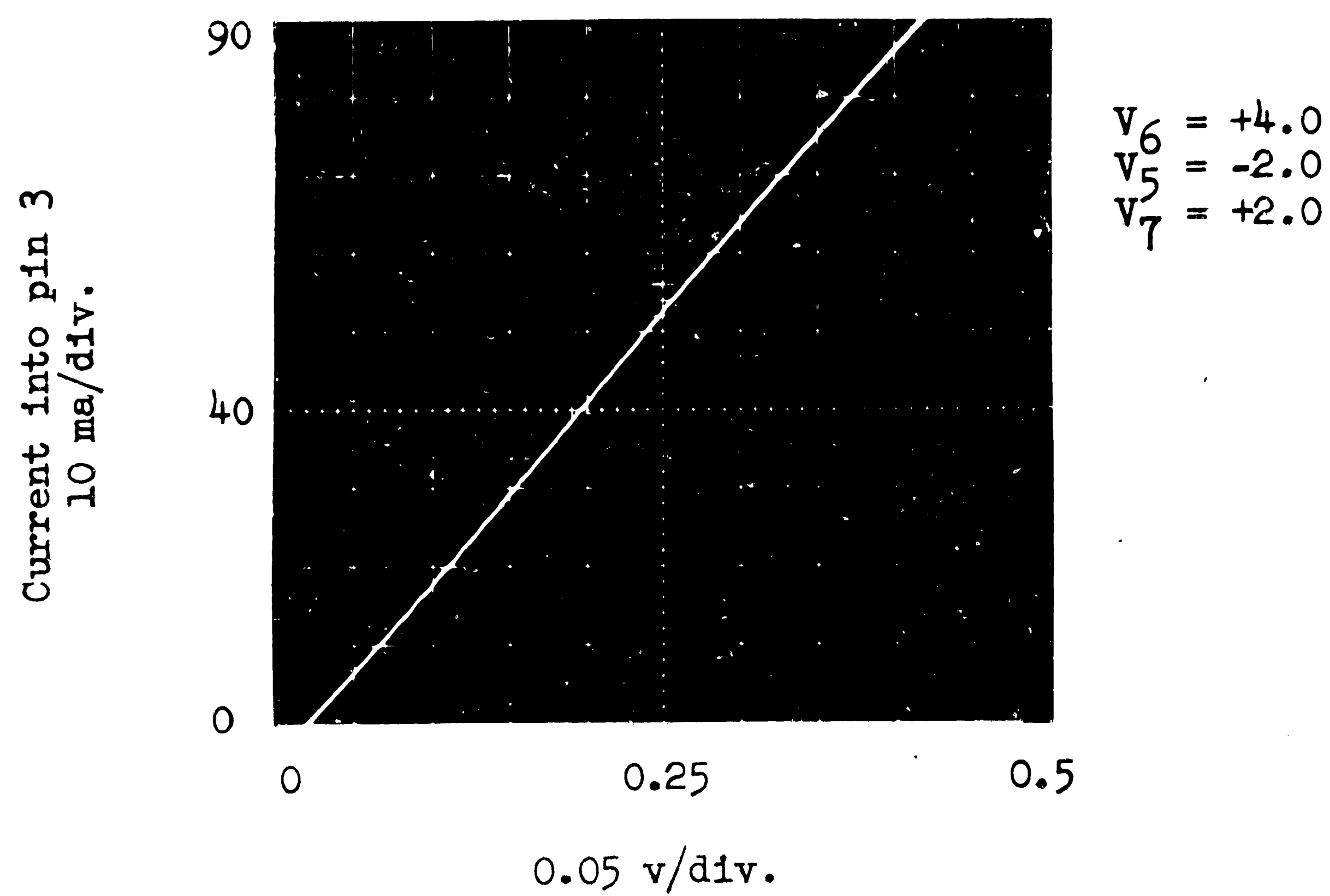
Input voltage on pin 7

NOTE: Refer to note on Input Output Characteristics.

INPUT CHARACTERISTICS

DTL - 264P

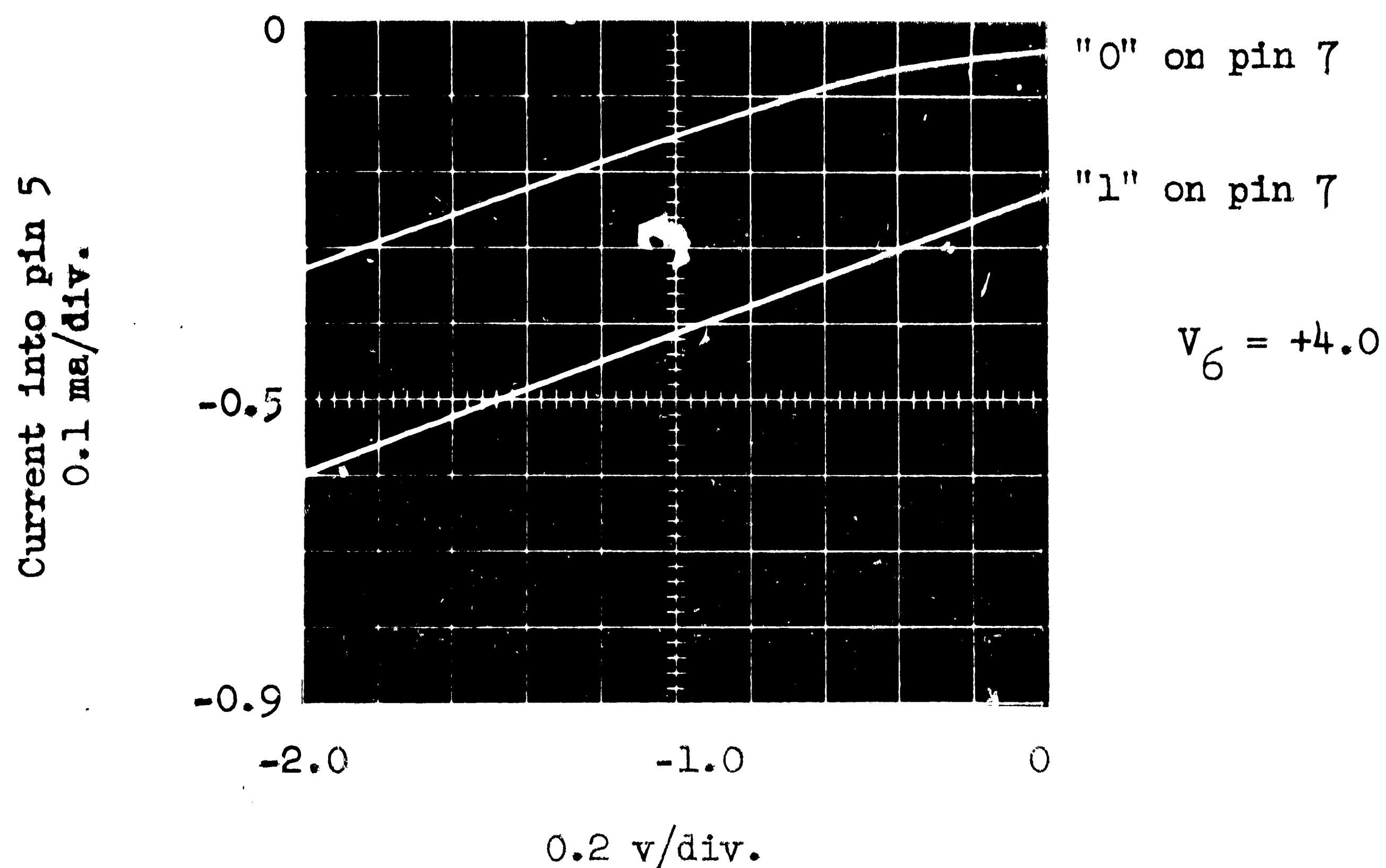
3.2.114



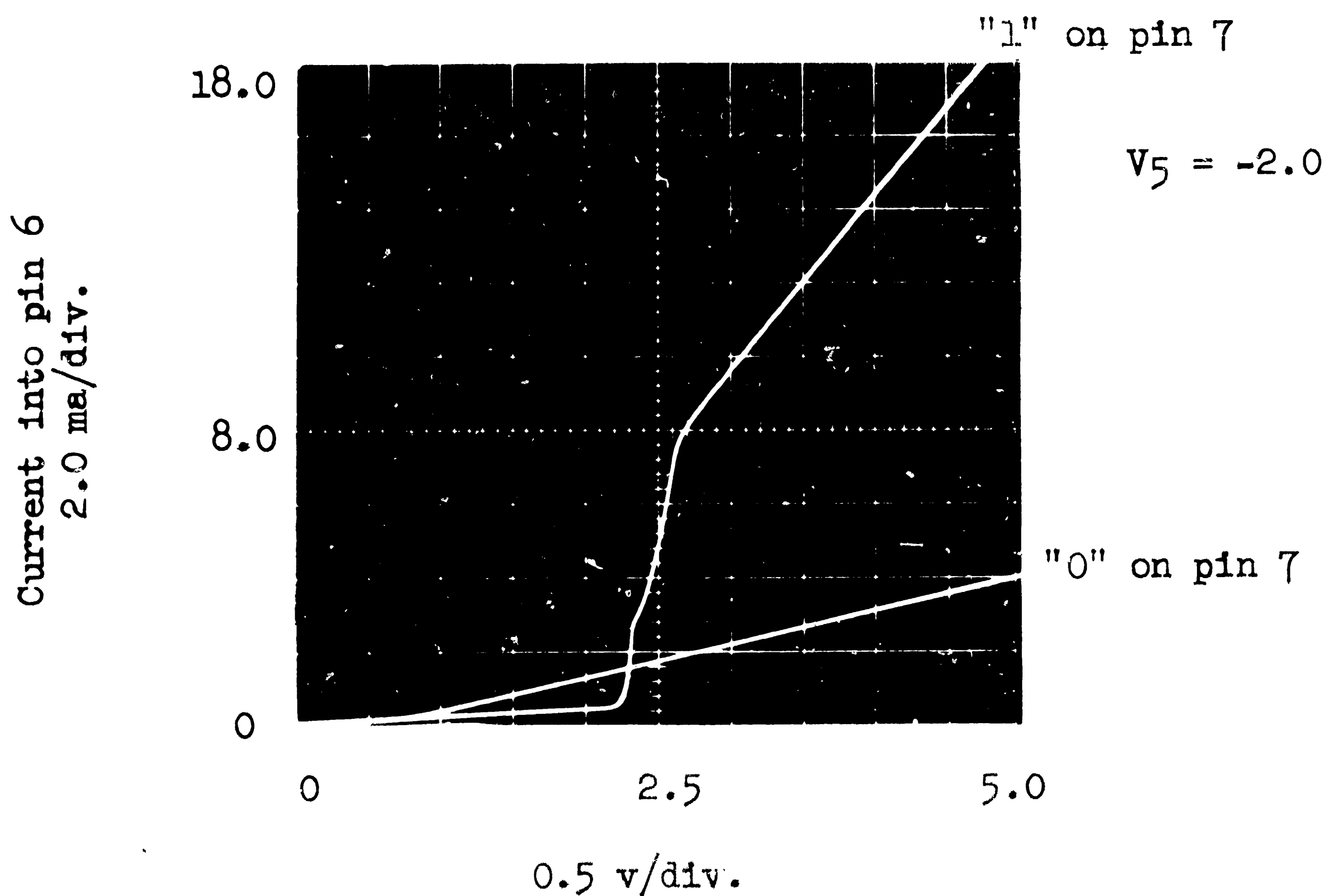
NOTE: Test ran "unloaded".

OUTPUT CHARACTERISTICS

DTL - 264P



Supply voltage on pin 5

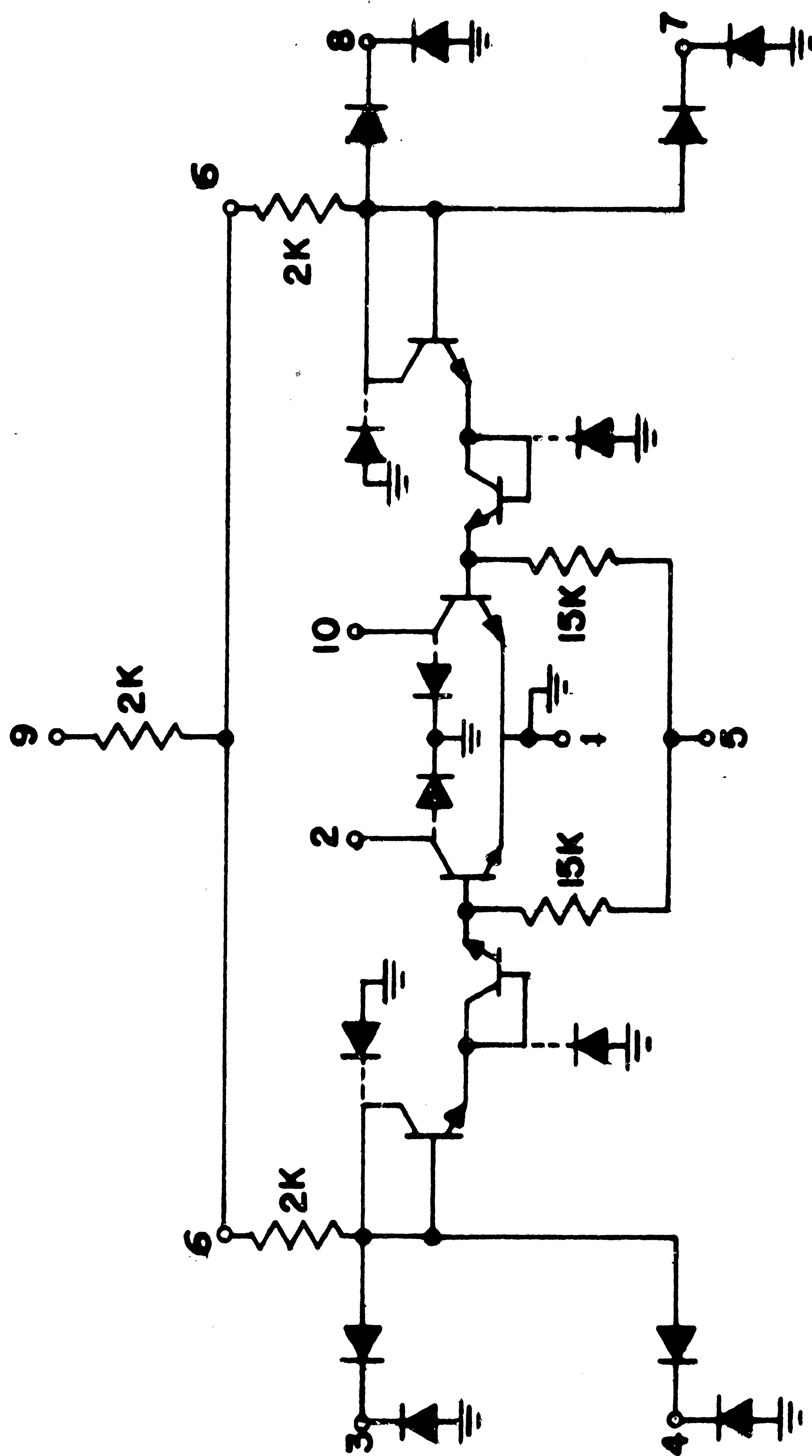


Supply voltage on pin 6

NOTE: Tests performed with 1K ohm pull-up resistor between pin 6 and pin 3.

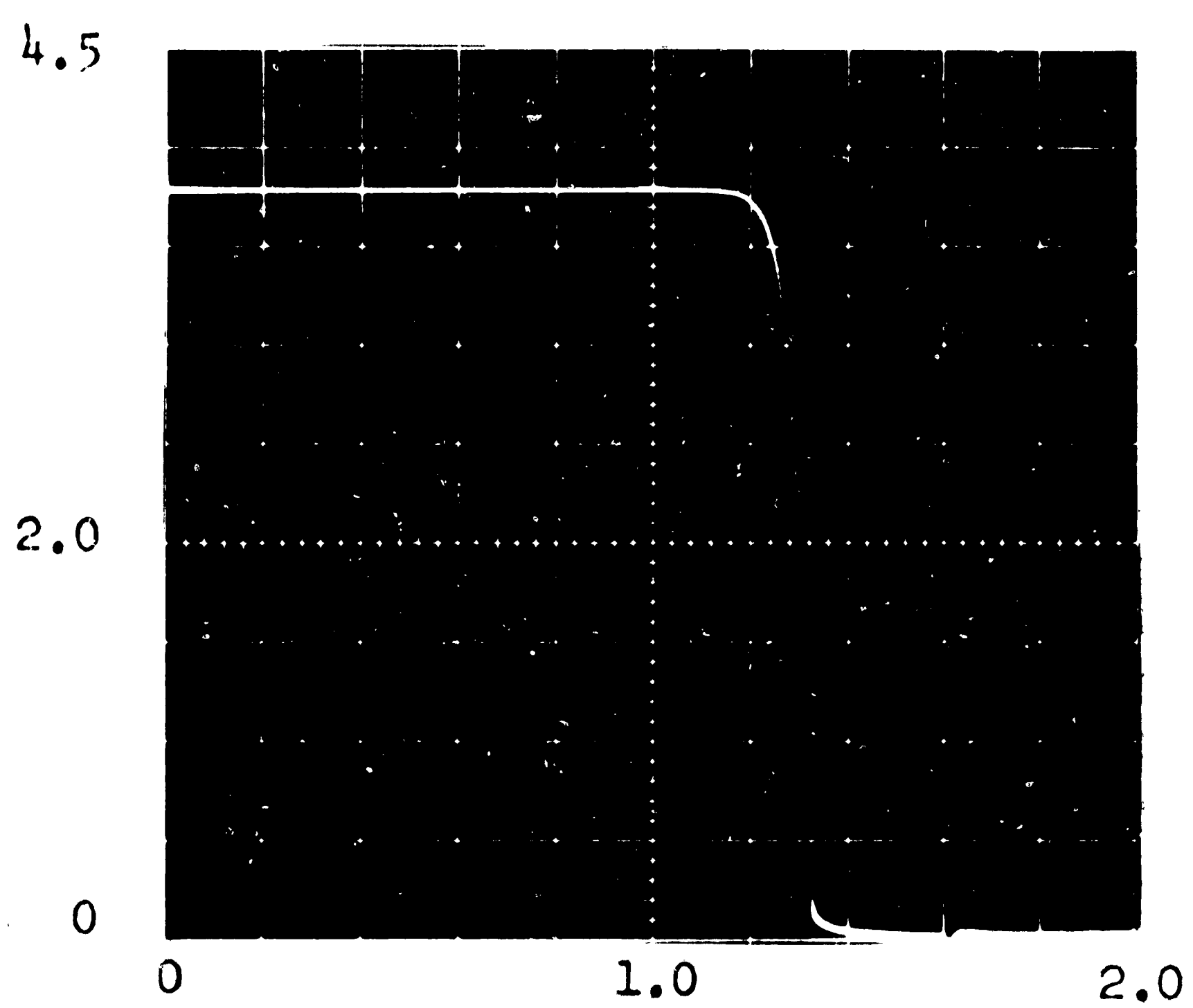
POWER DISSIPATION CURVES
DTL - 264P

3.2.116



264D₂ DUAL 2-INPUT DTL GATE/EXCLUSIVE OR ELEMENT

Output voltage on pins 2, 9 and 10
0.5 V/div.

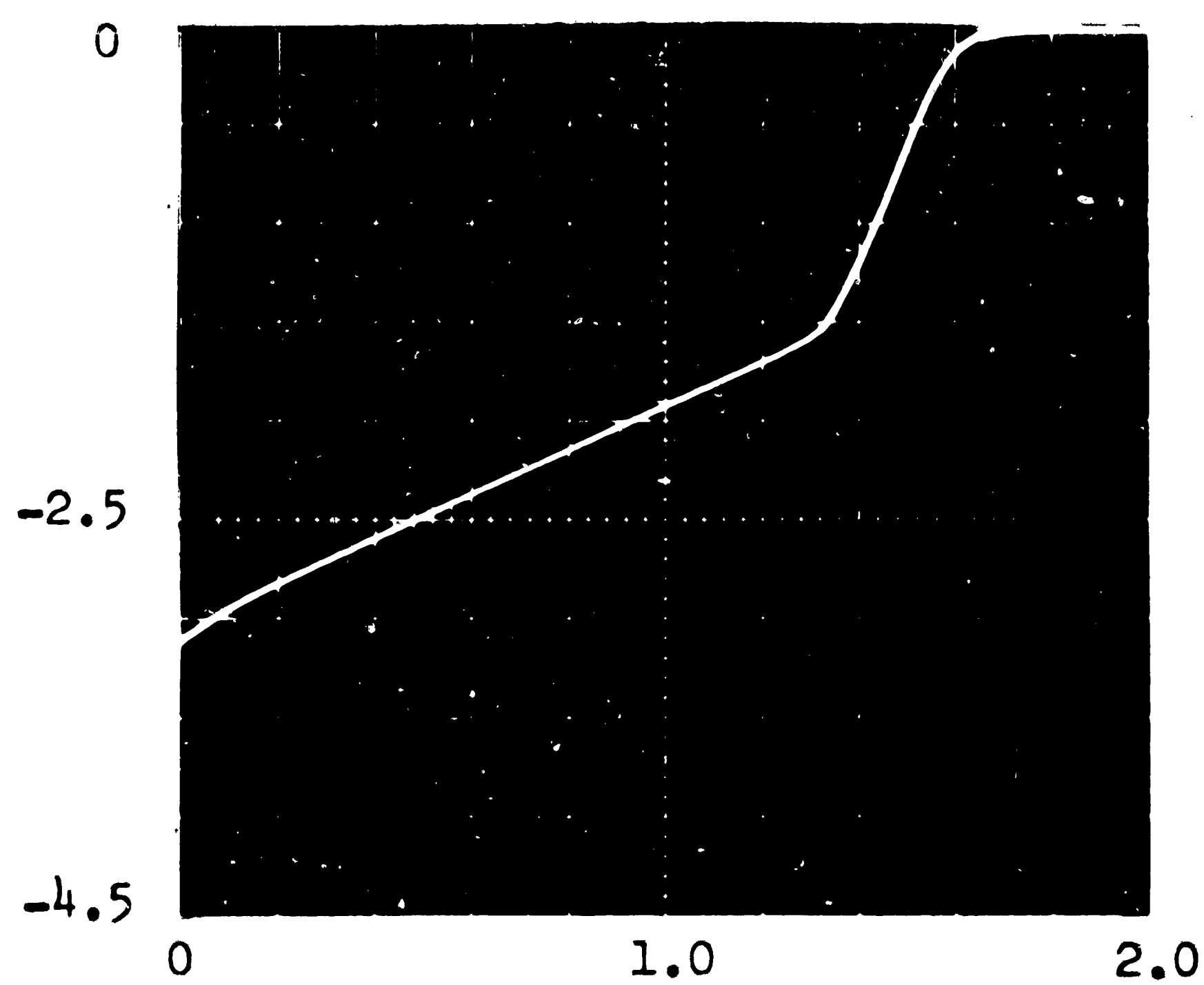


0.2 V/div.
Input Voltage on Pins 3 and 8

NOTE: Input pins 3 and 8 tied common.
Output pins 2 and 10 tied to pin 9
to utilize the pull up resistor

INPUT OUTPUT CHARACTERISTICS
DTL-264D2

Input Current into Pins 3 and 8
0.5 ma/div.



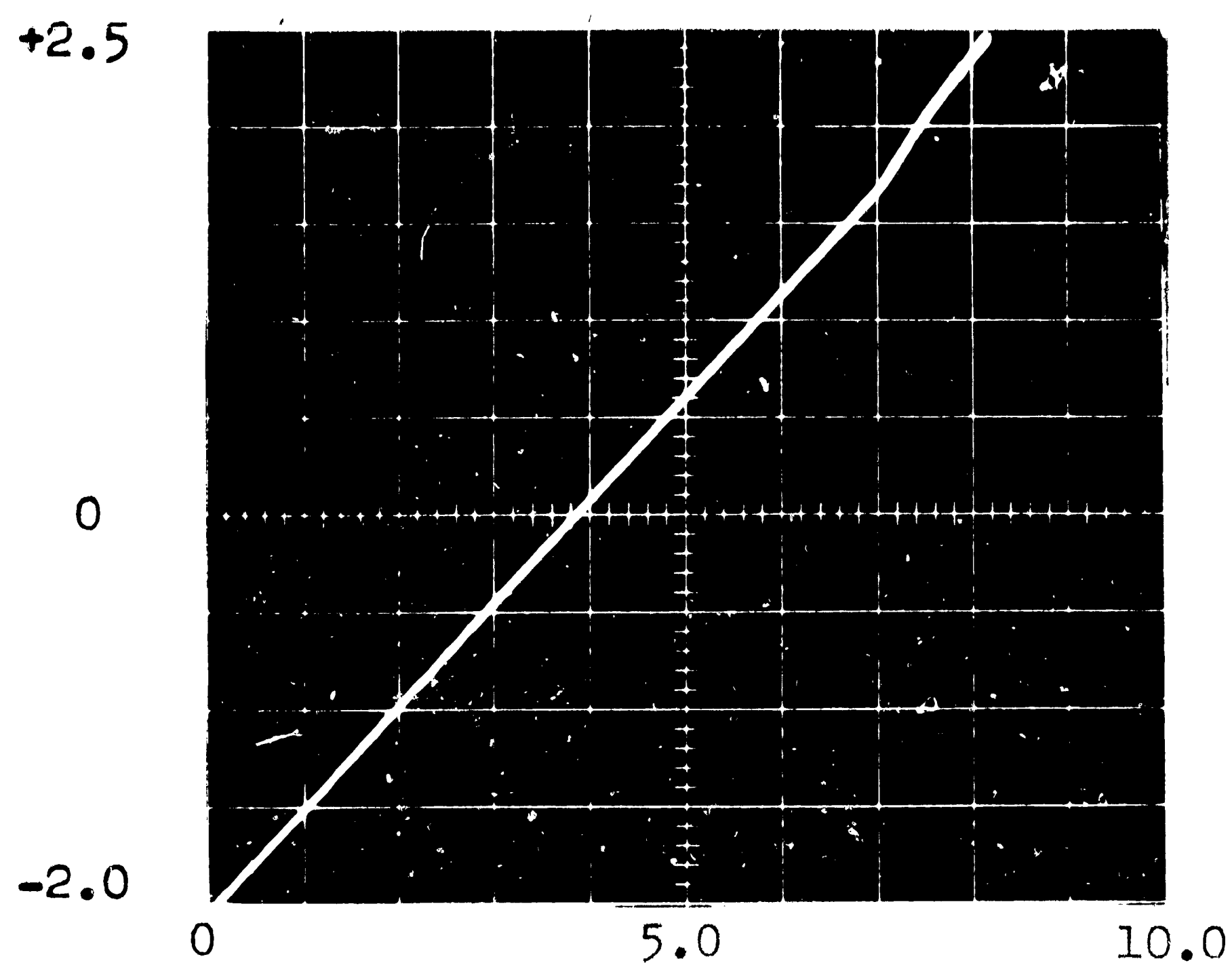
$V_6 = +4.0$

$V_5 = -2.0$

0.2 V/div.
Input Voltage on Pins 3 and 8

INPUT CHARACTERISTICS
DTL 264D2

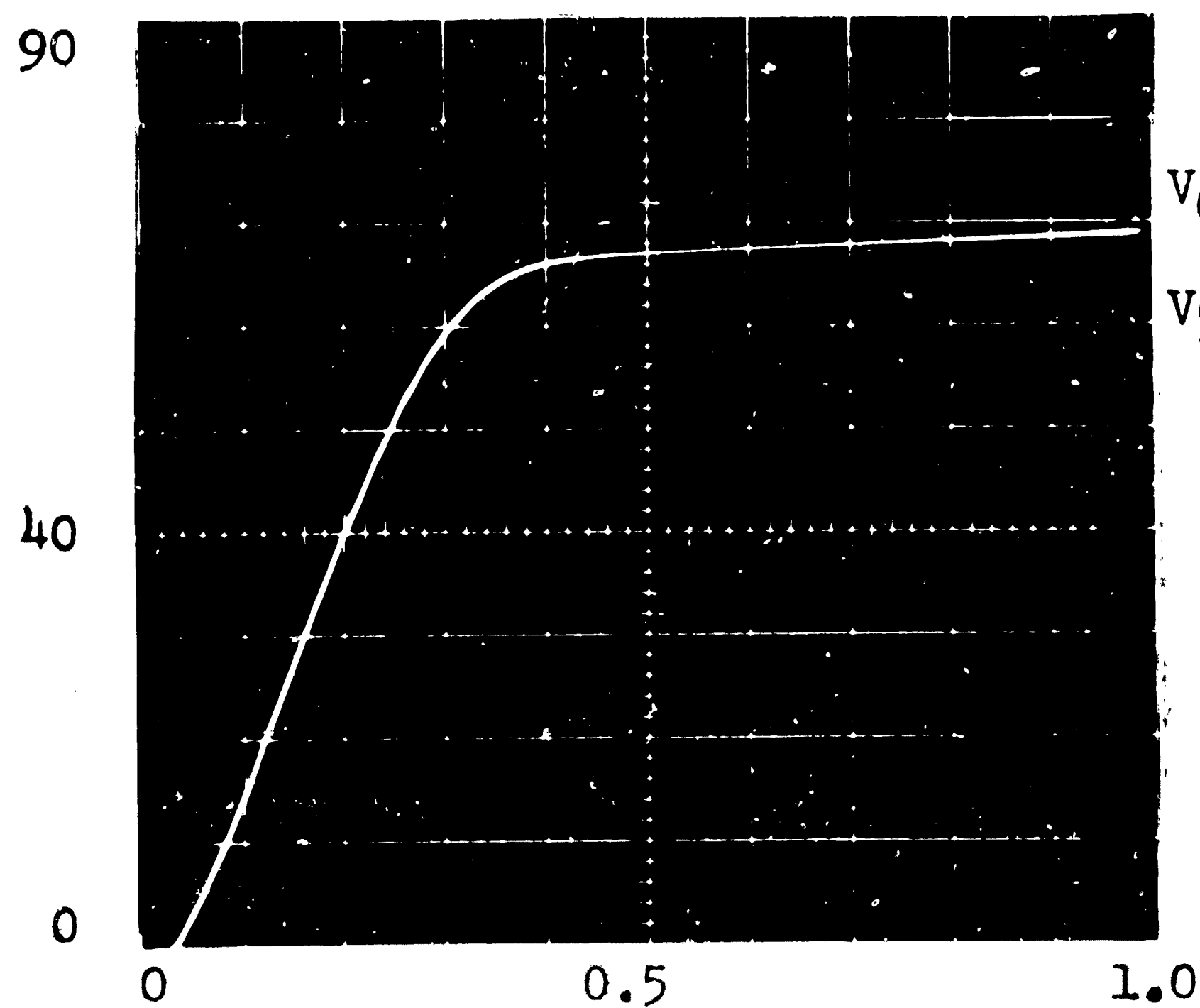
Output current into pins 2, 9 and 10
0.5 ma/div.



$V_6 = +4.0$
 $V_5 = -2.0$
 $V_3 = V_8 = 0.0$

1.0 V/div.
Output Voltage on Pins 2, 9 and 10

Output current into pins 2, 9 and 10
10. ma/div.



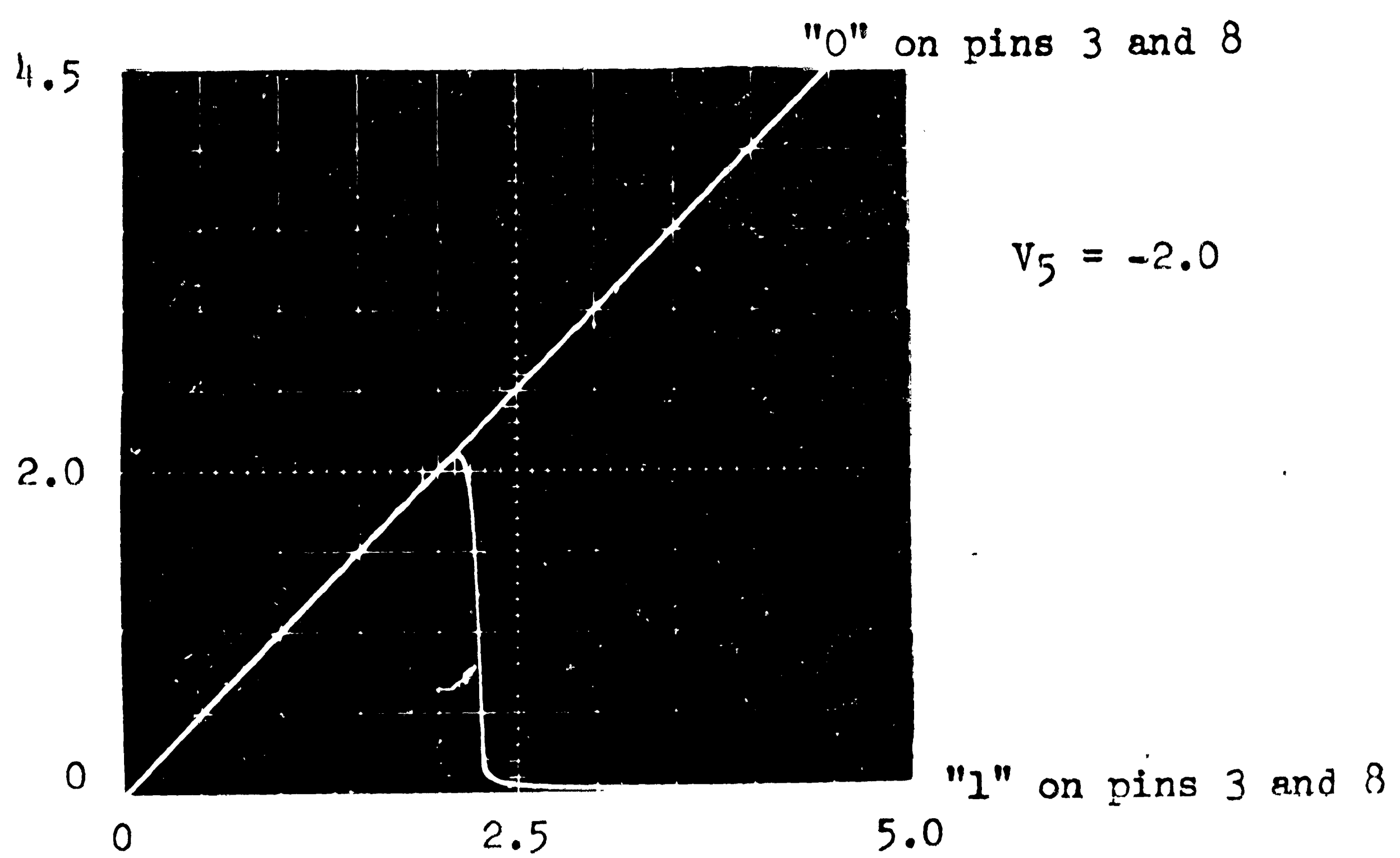
$V_6 = V_3 = V_8 = +4.0$
 $V_5 = -2.0$

0.1 V/div.
Output Voltage on Pins 2, 9 and 10

OUTPUT CHARACTERISTICS
DTL 264D2

3.2.120

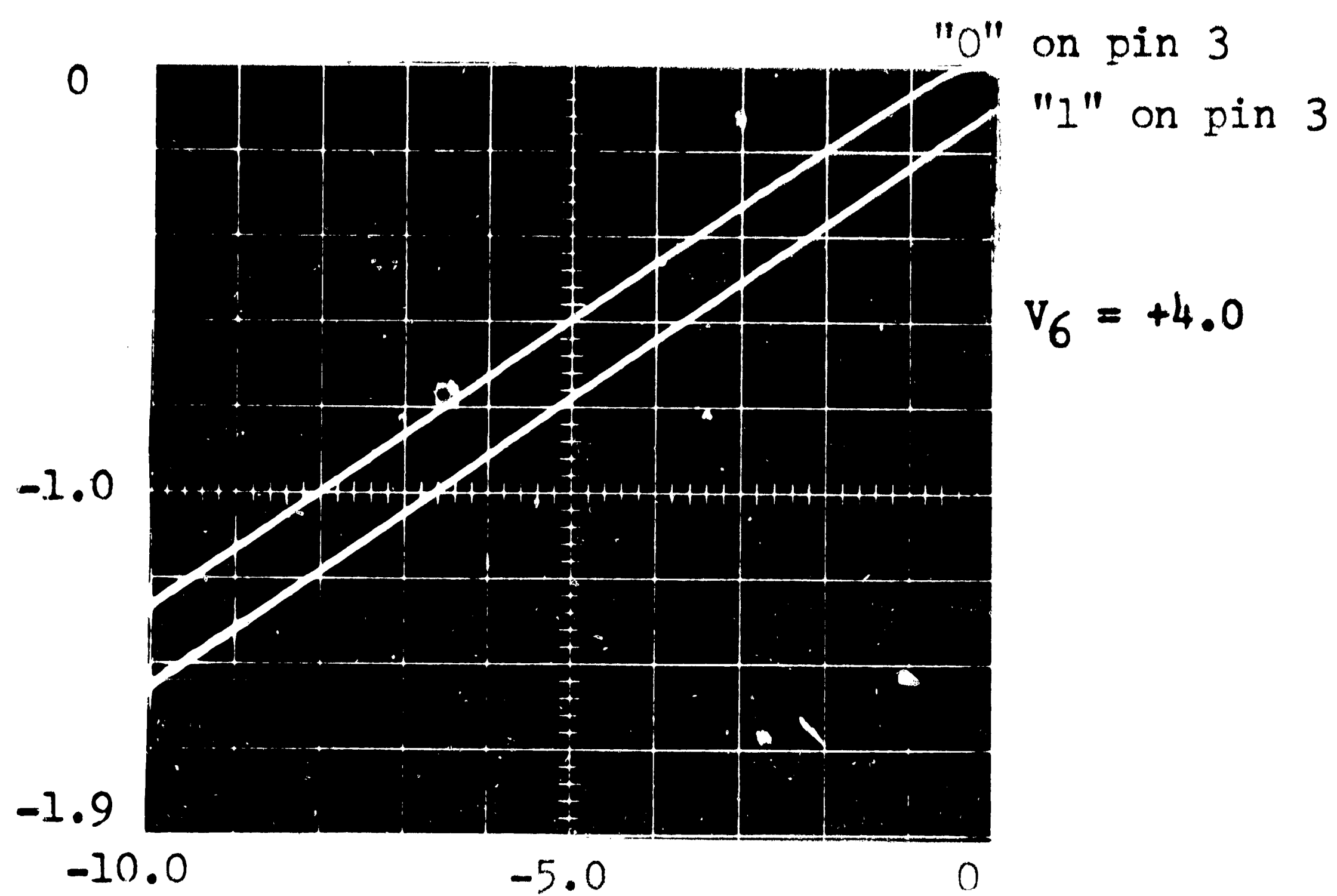
Output voltage on pins 2, 9 and 10
0.5 V/div.



0.5 V/div.
Supply Voltage on Pin 6

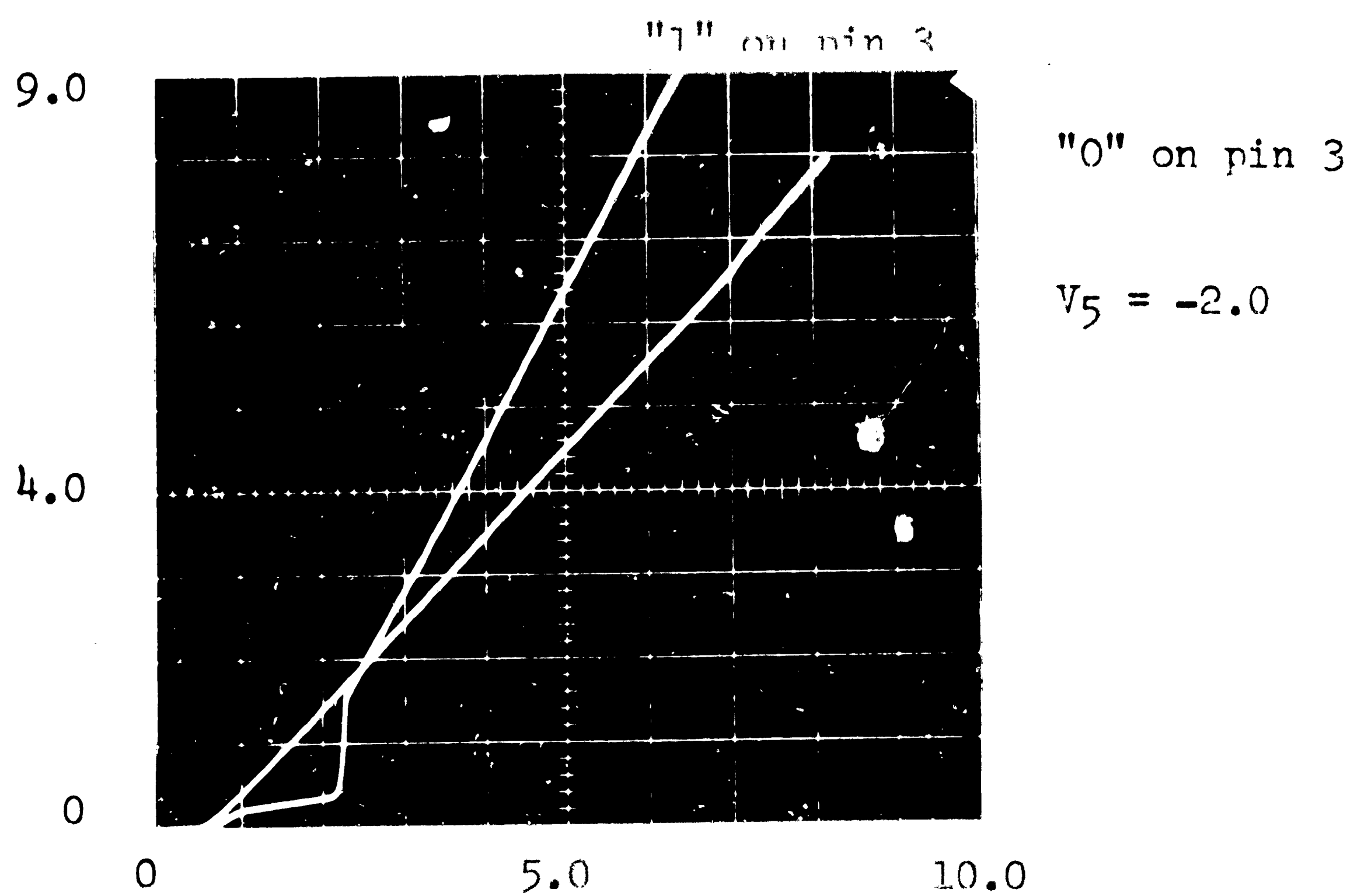
OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DTL 264D2

Current into Pin 5
0.2 ma/div.



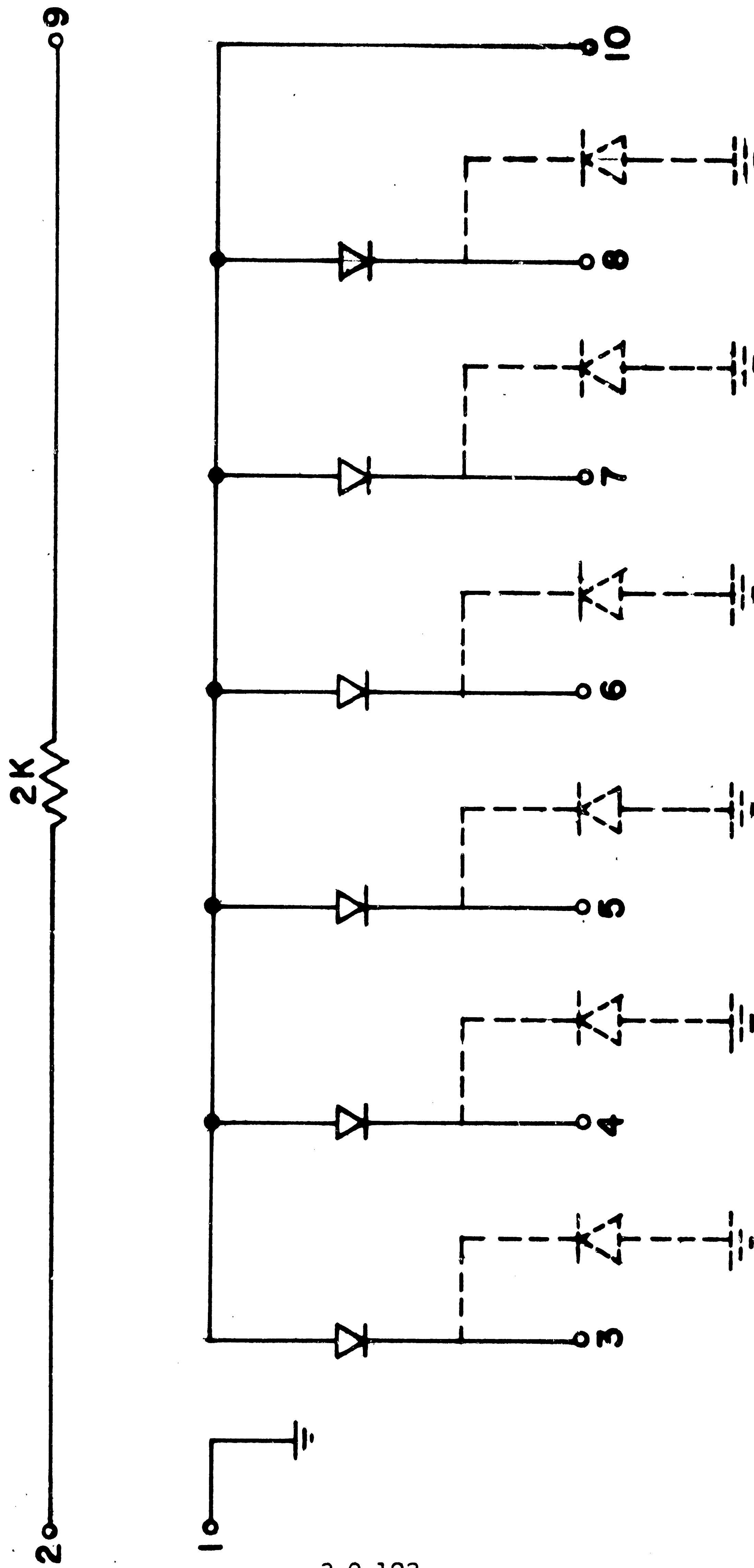
1.0 V/div.
Supply Voltage on Pin 5

Current into Pin 6
1 ma/div.



1 V/div.
Supply Voltage on Pin 6

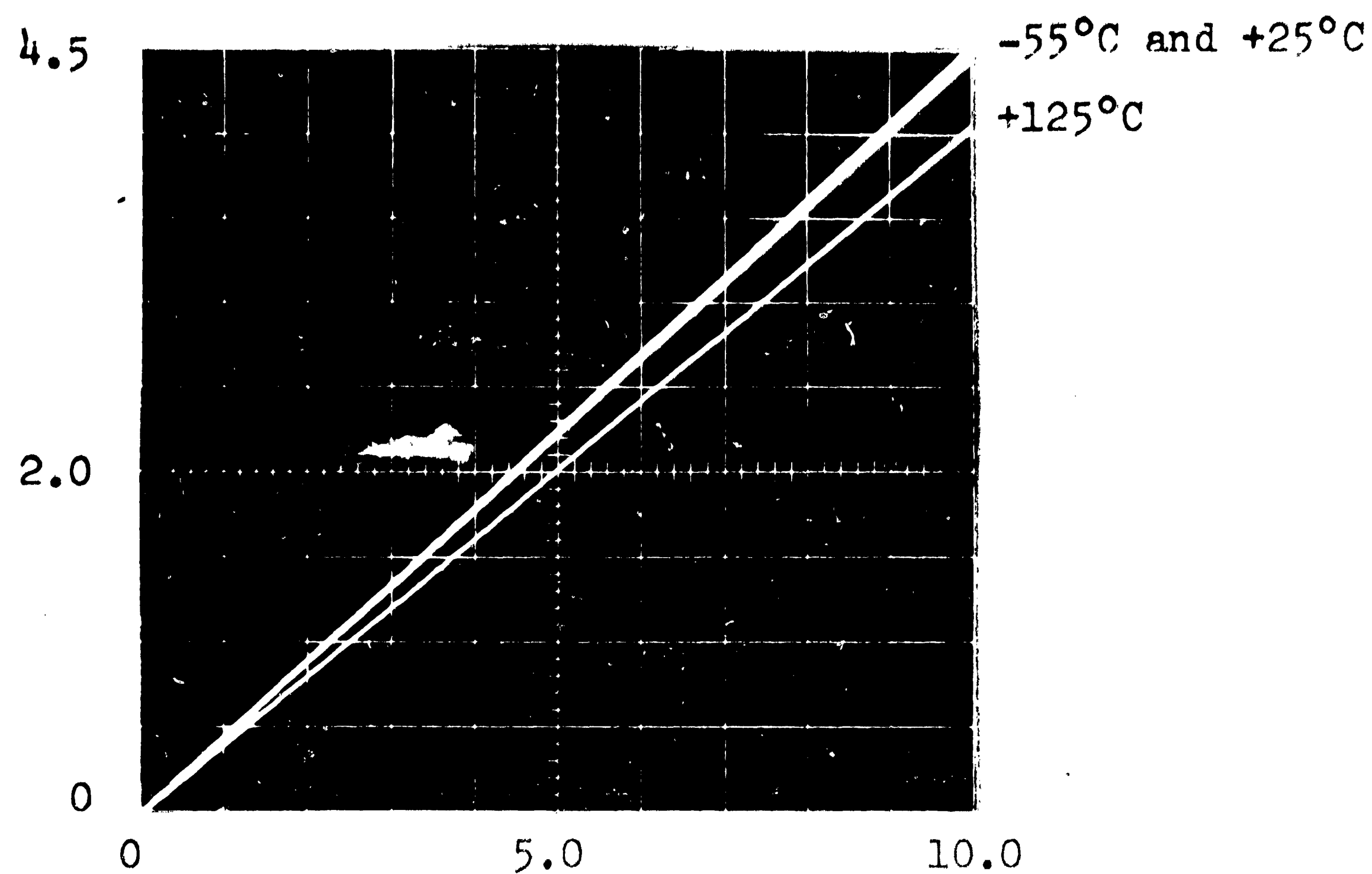
POWER DISSIPATION CURVES
DTL 264D2



3.2.123

254G6 6-INPUT DIODE AND GATE

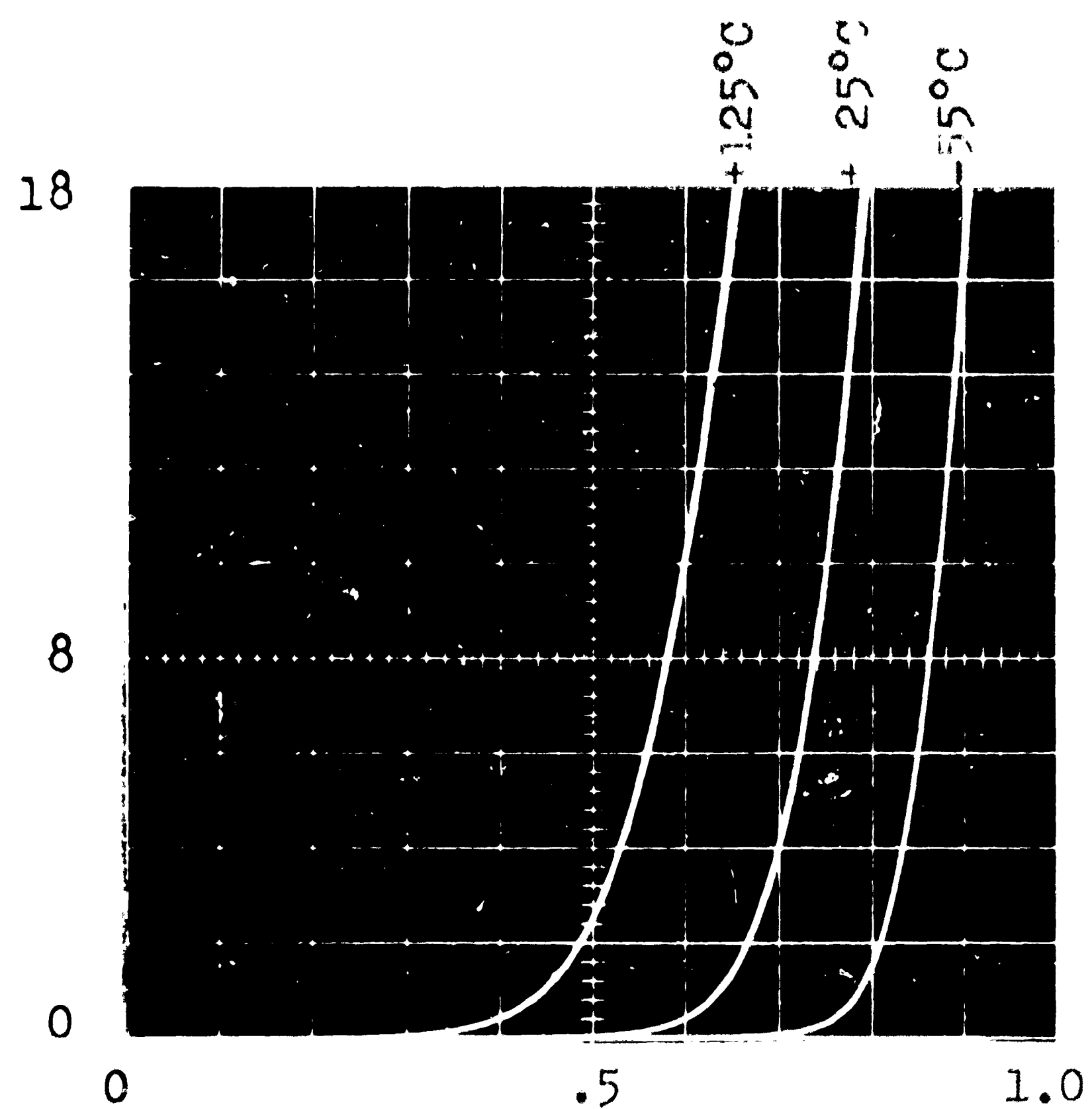
Current into Pin 2
0.5 ma/div.



1.0 V/div.
Voltage from Pin 2 to Pin 9

RESISTOR CHARACTERISTICS

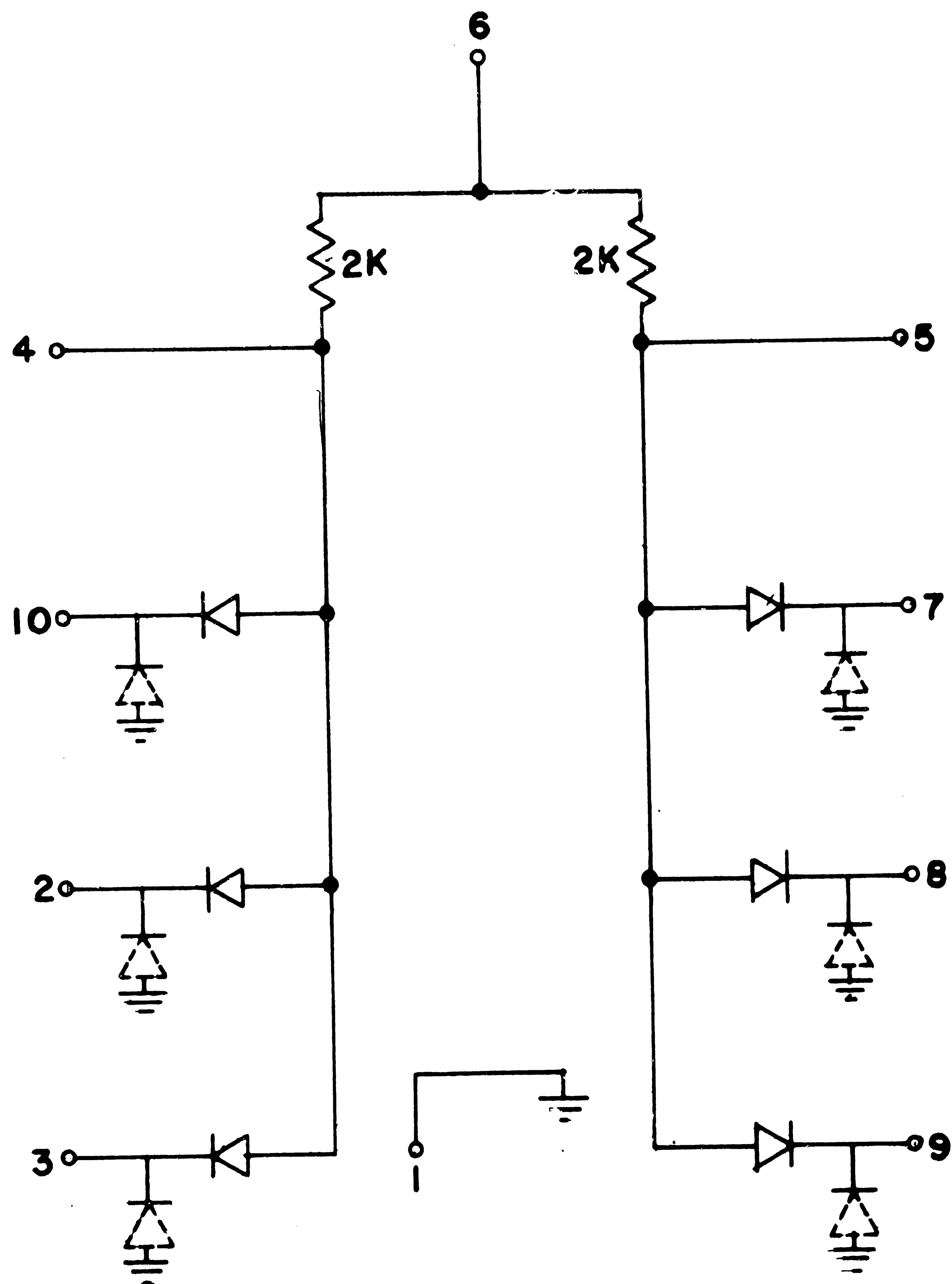
Current into Pin 10
2 ma/div.



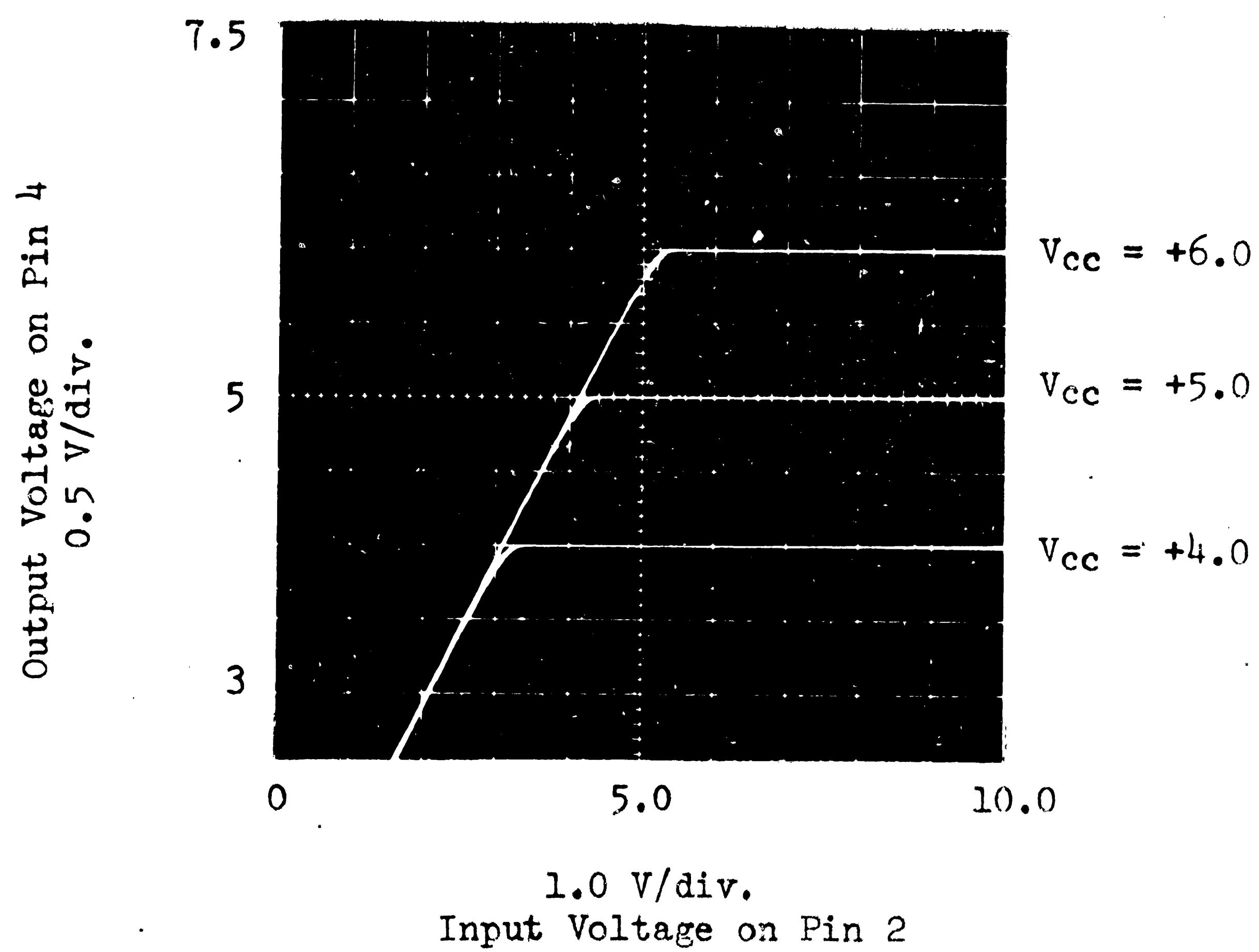
0.1 V/div.
Voltage from Pin 10 to Input Pins
(Pins 3, 4, 5, 6, 7, 8 tied common)

DIODE FORWARD CHARACTERISTICS
DTL 254G6

3.2.124

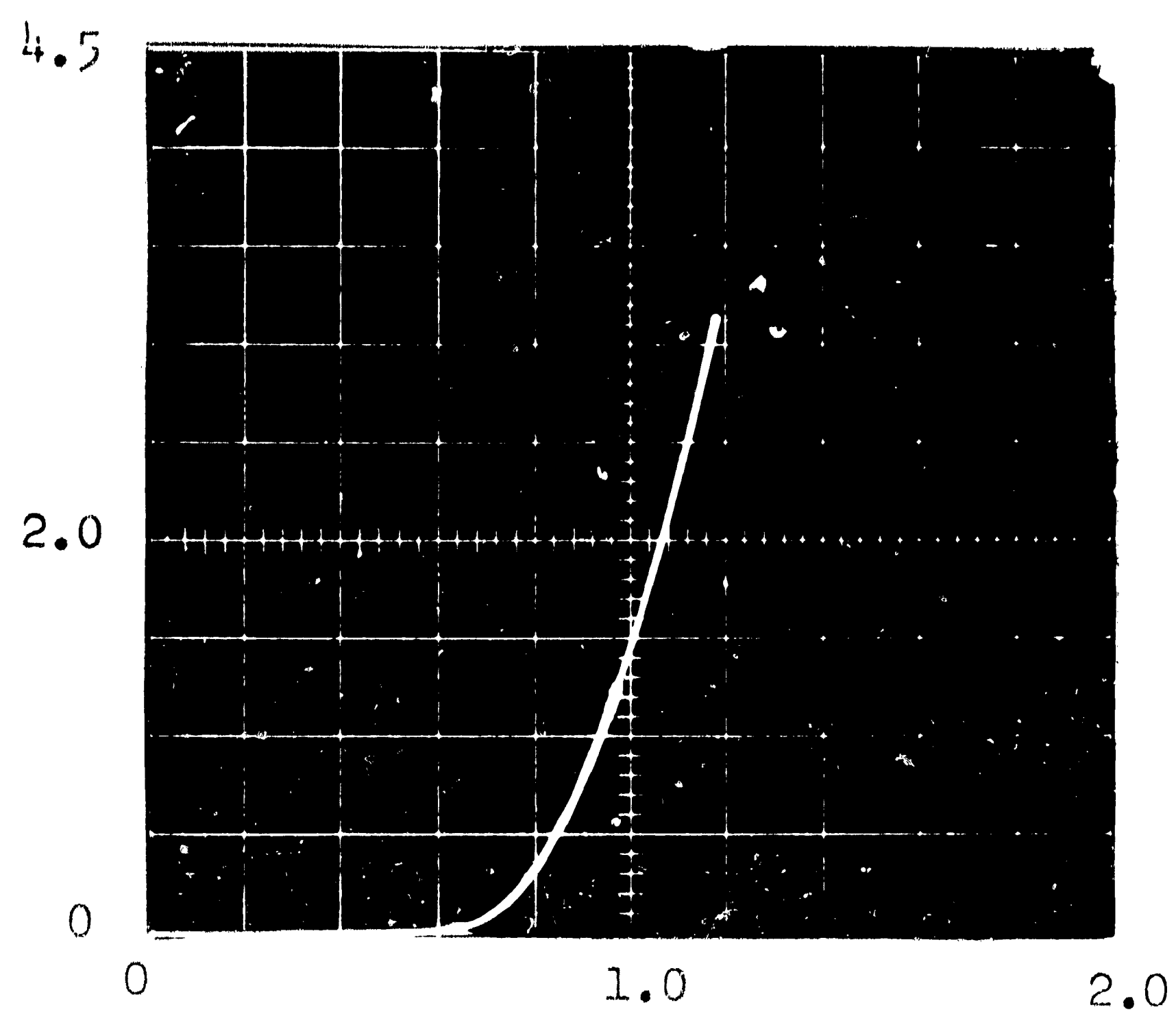


254D3 DUAL 3-INPUT DIODE AND GATE



INPUT - OUTPUT CHARACTERISTICS
DTL 254D3

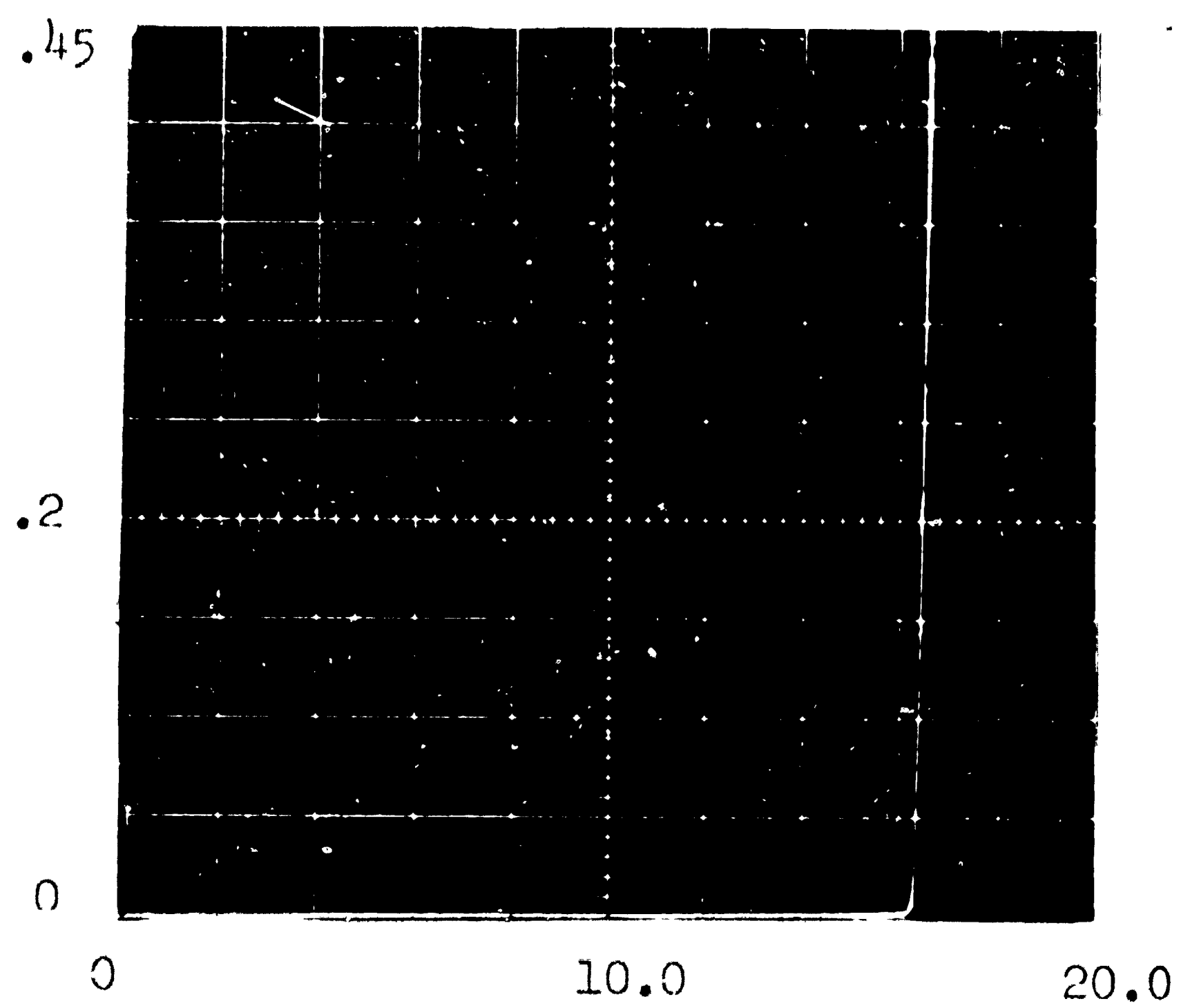
Current into Pin 4
5.0 ma/div.



0.2 V/div.
Voltage from Pin 4 to Pin 10

FORWARD CHARACTERISTICS

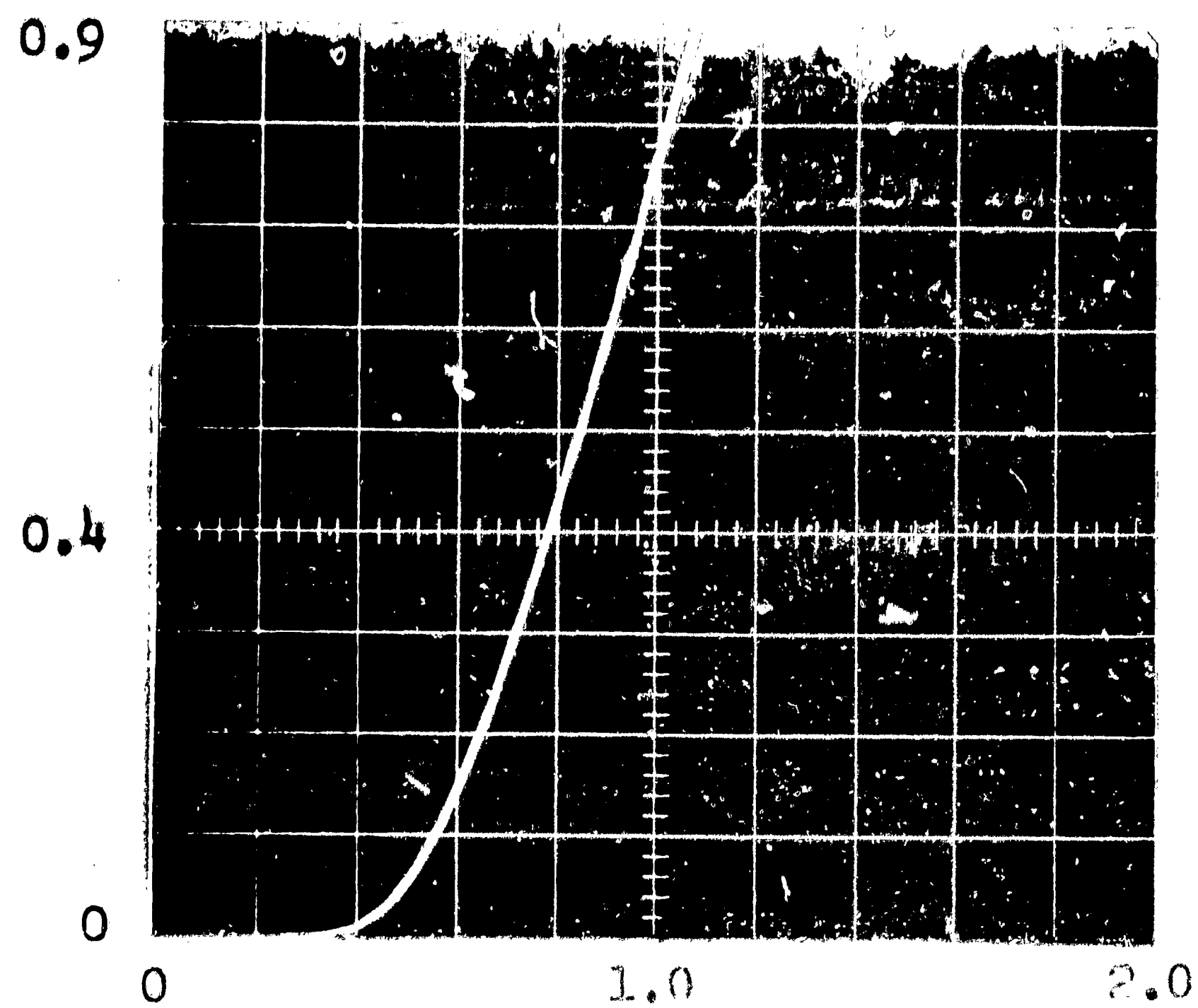
Current into Pins 10, 2 and 3
0.05 ma/div.



2.0 V/div.
Voltage from Common Input
Pins 10, 2 and 3 to Pin 4

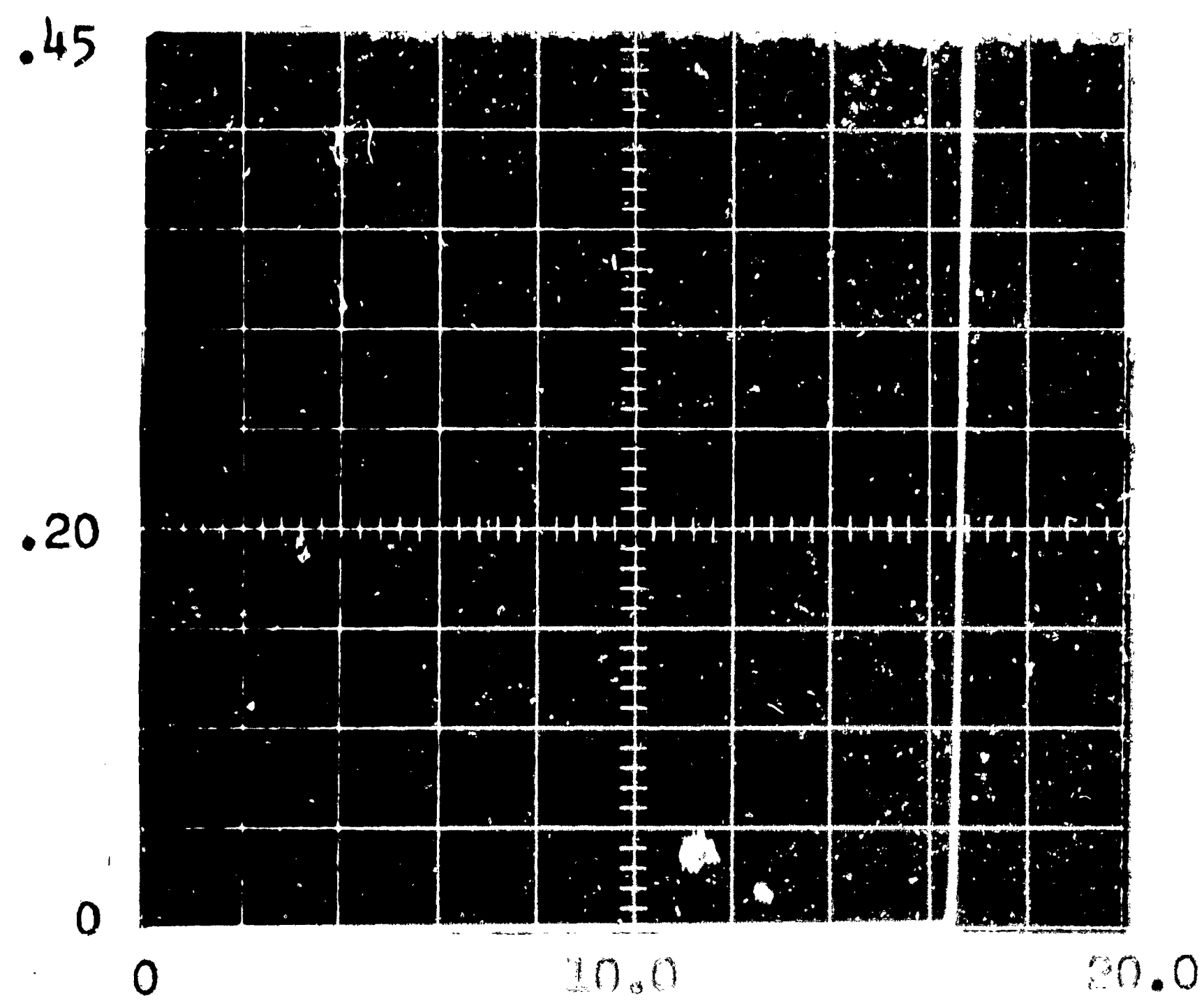
REVERSE CHARACTERISTICS
INPUT DIODE CHARACTERISTICS
DTL 254D3

Current into Pin 1
0.1 ma/div.



0.2 V/div.
Voltage from Pin 1 to Pin 10
FORWARD CHARACTERISTICS

Current into Pin 10
0.05 ma/div.

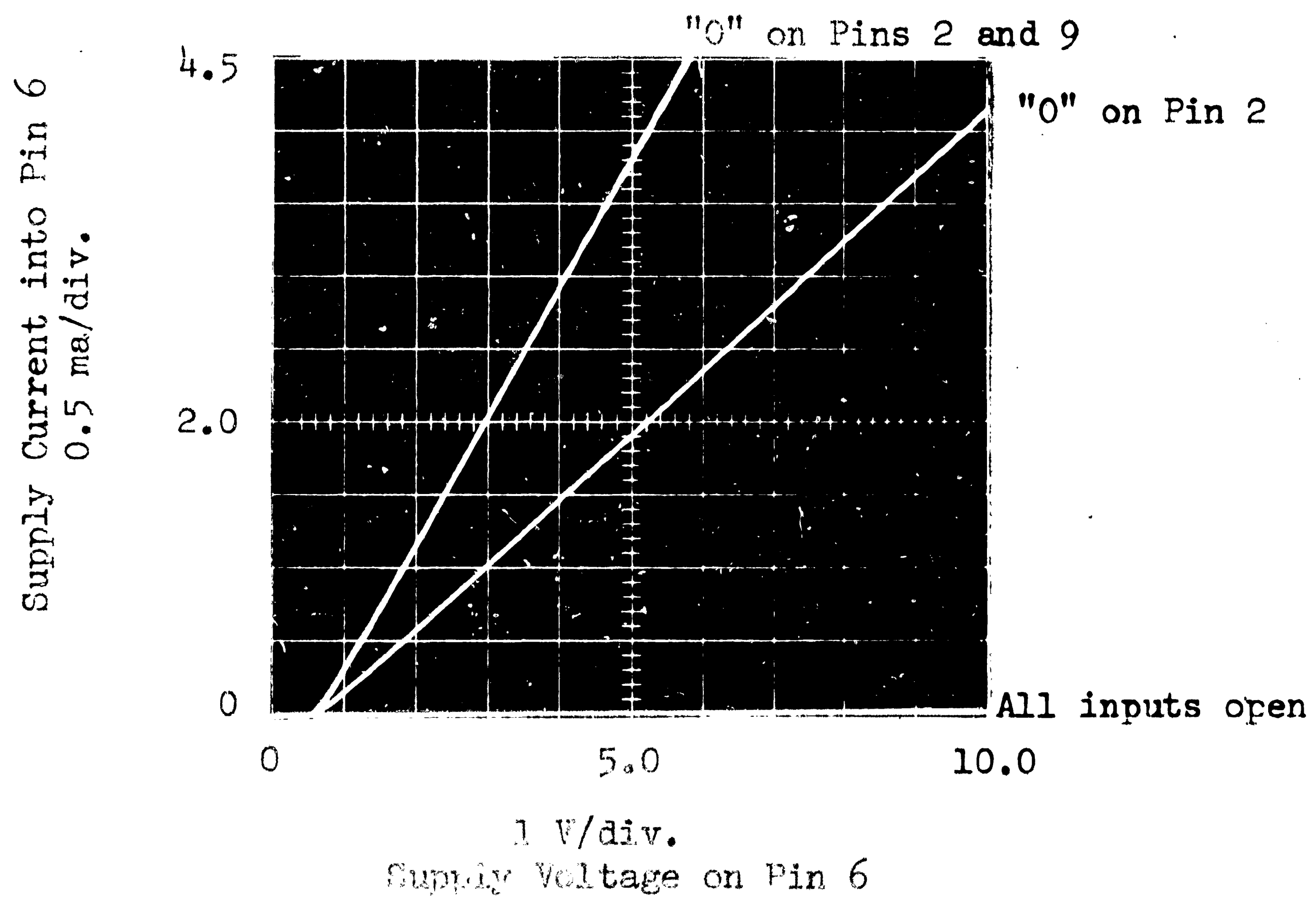


2.0 V/div.
Voltage from Pin 10 to Pin 1

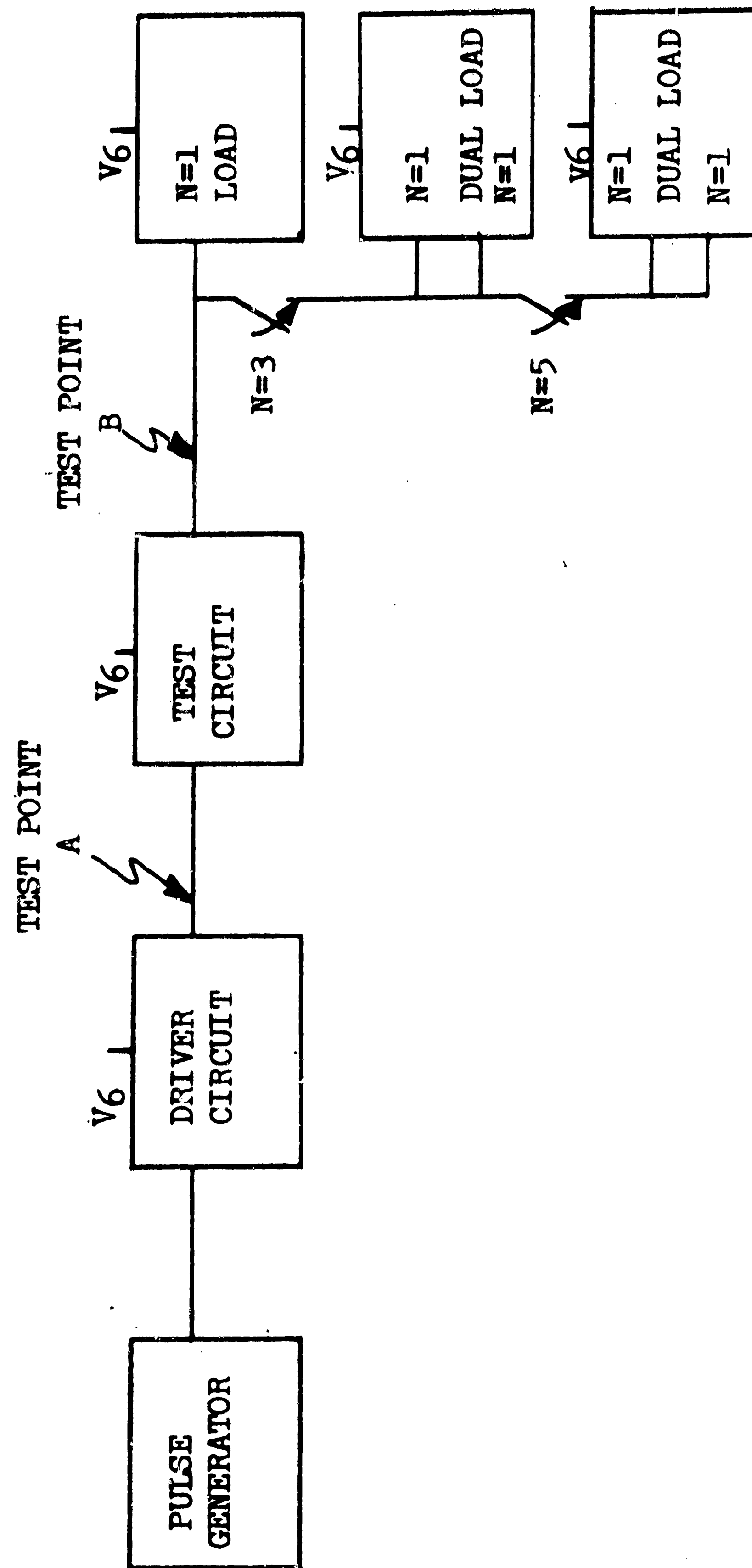
REVERSE CHARACTERISTICS

ISOLATION DIODE CHARACTERISTICS
DEL 25403

3.2.128



POWER DISSIPATION
DEL 254D3

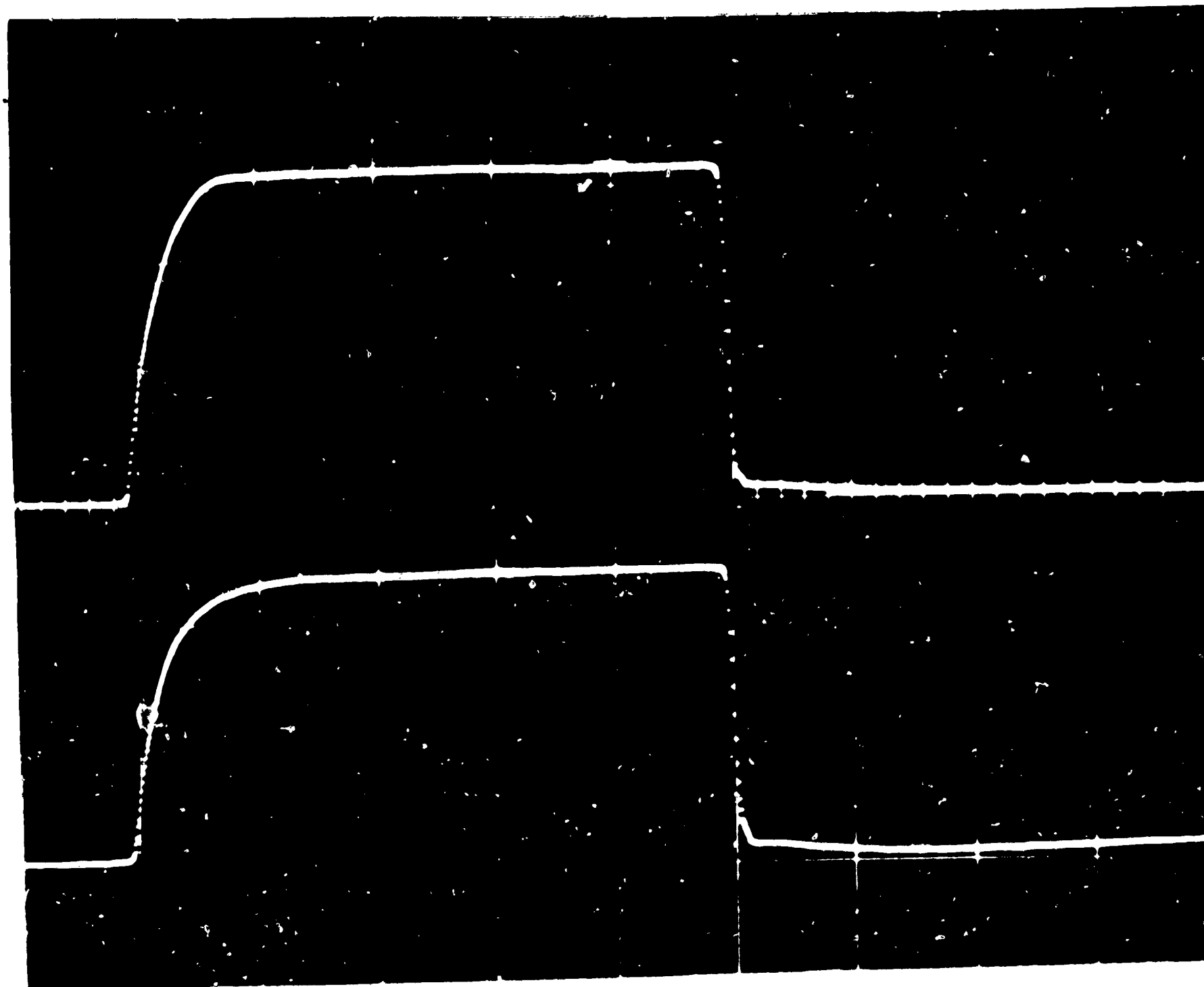


TEST CIRCUIT FOR DIODE AND GATE 254D3

GENERAL MICRO-ELECTRONICS

Type DL No. 254D3 Temp. +25°C Vcc +4.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>506.</u>	<u>501.</u>	<u>500.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.84</u>	<u>1.60</u>	<u>2.40</u>	<u>2.82</u>
T_r	<u>53.</u>	<u>37.</u>	<u>60.</u>	<u>45.</u>
T_f	<u>12.</u>	<u>12.</u>	<u>11.</u>	<u>12.</u>
T_d		<u>0.</u>	<u>0.</u>	<u>2.</u>
T_s		<u>4.</u>	<u>2.</u>	<u>1.</u>
T_{pd}		<u>2.</u>	<u>1.5</u>	<u>2.0</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DL No. 254D₃ Temp. -40°C Vcc +4.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>508.</u>	<u>502.</u>	<u>500.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.84</u>	<u>1.36</u>	<u>2.22</u>	<u>2.84</u>
T _r	<u>59.</u>	<u>33.</u>	<u>58.</u>	<u>52.</u>
T _f	<u>11.</u>	<u>11.</u>	<u>11.</u>	<u>11.</u>
T _d		<u>1.0</u>	<u>1.2</u>	<u>2.0</u>
T _s		<u>4.0</u>	<u>2.8</u>	<u>1.0</u>
T _{pd}		<u>2.0</u>	<u>1.4</u>	<u>1.5</u>

Type DL No. 254D₃ Temp. -55°C Vcc 4.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>509.</u>	<u>503.</u>	<u>500.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.90</u>	<u>1.31</u>	<u>2.22</u>	<u>2.90</u>
T _r	<u>64.</u>	<u>34.</u>	<u>61.</u>	<u>55.</u>
T _f	<u>11.</u>	<u>13.</u>	<u>11.</u>	<u>11.</u>
T _d		<u>1.0</u>	<u>1.0</u>	<u>1.6</u>
T _s		<u>4.6</u>	<u>3.0</u>	<u>1.0</u>
T _{pd}		<u>2.0</u>	<u>1.5</u>	<u>1.5</u>

GENERAL MICRO-ELECTRONICS

Type DL No. 254D₃ Temp. +85°C Vcc +4.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>505.</u>	<u>500.</u>	<u>501.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.85</u>	<u>1.87</u>	<u>2.61</u>	<u>2.82</u>
T _r	<u>56.</u>	<u>44.</u>	<u>66.</u>	<u>46.</u>
T _f	<u>13.</u>	<u>13.</u>	<u>13.</u>	<u>12.</u>
T _d		<u>1.0</u>	<u>1.5</u>	<u>1.0</u>
T _s		<u>4.0</u>	<u>1.0</u>	<u>1.0</u>
T _{pd}		<u>1.5</u>	<u>1.5</u>	<u>2.0</u>

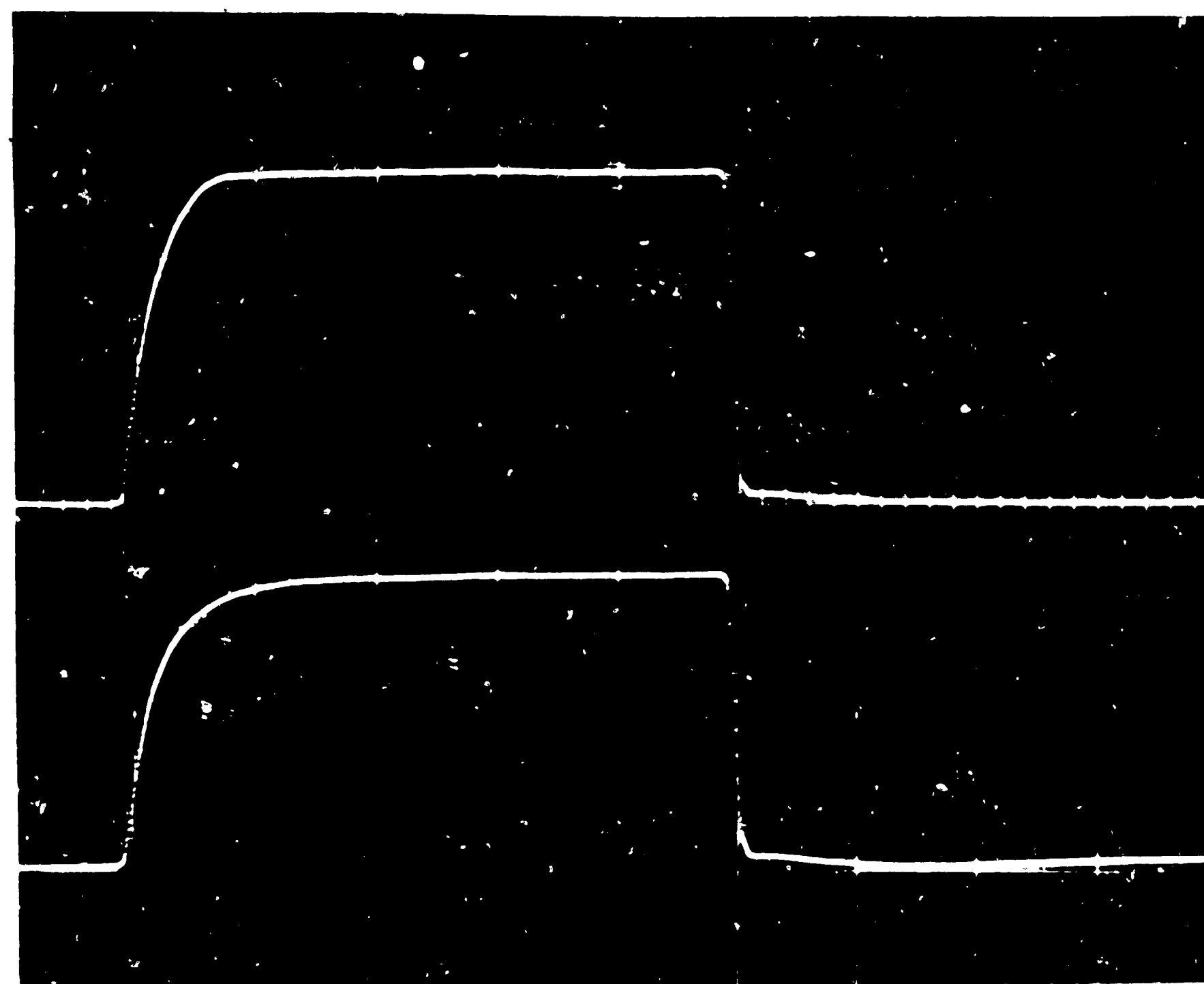
Type DL No. 254D₃ Temp. +125°C Vcc +4.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>505.</u>	<u>502.</u>	<u>502.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.83</u>	<u>1.98</u>	<u>2.64</u>	<u>2.80</u>
T _r	<u>59.</u>	<u>51.</u>	<u>62.</u>	<u>47.</u>
T _f	<u>13.</u>	<u>14.</u>	<u>13.</u>	<u>13.</u>
T _d		<u>1.3</u>	<u>2.0</u>	<u>2.0</u>
T _s		<u>3.0</u>	<u>2.0</u>	<u>1.0</u>
T _{pd}		<u>2.0</u>	<u>2.5</u>	<u>2.0</u>

GENERAL MICRO-ELECTRONICS

Type DL No. 254D3 Temp. +25°C Vcc 4.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>505.</u>	<u>499.</u>	<u>500.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.84</u>	<u>1.60</u>	<u>2.44</u>	<u>2.42</u>
T_r	<u>54.</u>	<u>40.</u>	<u>67.</u>	<u>49.</u>
T_f	<u>12.</u>	<u>12.</u>	<u>11.</u>	<u>12.</u>
T_d		<u>0.</u>	<u>2.0</u>	<u>2.0</u>
T_s		<u>4.0</u>	<u>3.0</u>	<u>1.2</u>
T_{pd}		<u>2.0</u>	<u>2.0</u>	<u>2.0</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DL No. 254D₃ Temp. -40°C Vcc +4.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>507.</u>	<u>502.</u>	<u>499.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.82</u>	<u>1.34</u>	<u>2.24</u>	<u>2.86</u>
T _r	<u>58.</u>	<u>37.</u>	<u>66.</u>	<u>55.</u>
T _f	<u>11.</u>	<u>12.</u>	<u>11.</u>	<u>12.</u>
T _d		<u>1.0</u>	<u>1.8</u>	<u>2.0</u>
T _s		<u>4.0</u>	<u>2.9</u>	<u>1.0</u>
T _{pd}		<u>2.0</u>	<u>2.0</u>	<u>2.0</u>

Type DL No. 254D₃ Temp. -55°C Vcc 4.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>508.</u>	<u>502.</u>	<u>499.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.88</u>	<u>1.30</u>	<u>2.16</u>	<u>2.83</u>
T _r	<u>59.</u>	<u>38.</u>	<u>67.</u>	<u>54.</u>
T _f	<u>11.</u>	<u>12.</u>	<u>11.</u>	<u>12.</u>
T _d		<u>1.0</u>	<u>1.0</u>	<u>2.0</u>
T _s		<u>4.6</u>	<u>3.0</u>	<u>1.0</u>
T _{pd}		<u>2.5</u>	<u>1.5</u>	<u>2.0</u>

GENERAL MICRO-ELECTRONICS

Type DL No. 254D₃ Temp. +85°C Vcc +4.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>505.</u>	<u>499.</u>	<u>501.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.75</u>	<u>1.83</u>	<u>2.56</u>	<u>2.76</u>
T _r	<u>54.</u>	<u>49.</u>	<u>70.</u>	<u>48.</u>
T _f	<u>12.</u>	<u>13.</u>	<u>13.</u>	<u>12.</u>
T _d		<u>1.2</u>	<u>2.0</u>	<u>1.6</u>
T _s		<u>4.0</u>	<u>1.5</u>	<u>1.0</u>
T _{pd}		<u>2.0</u>	<u>2.0</u>	<u>2.0</u>

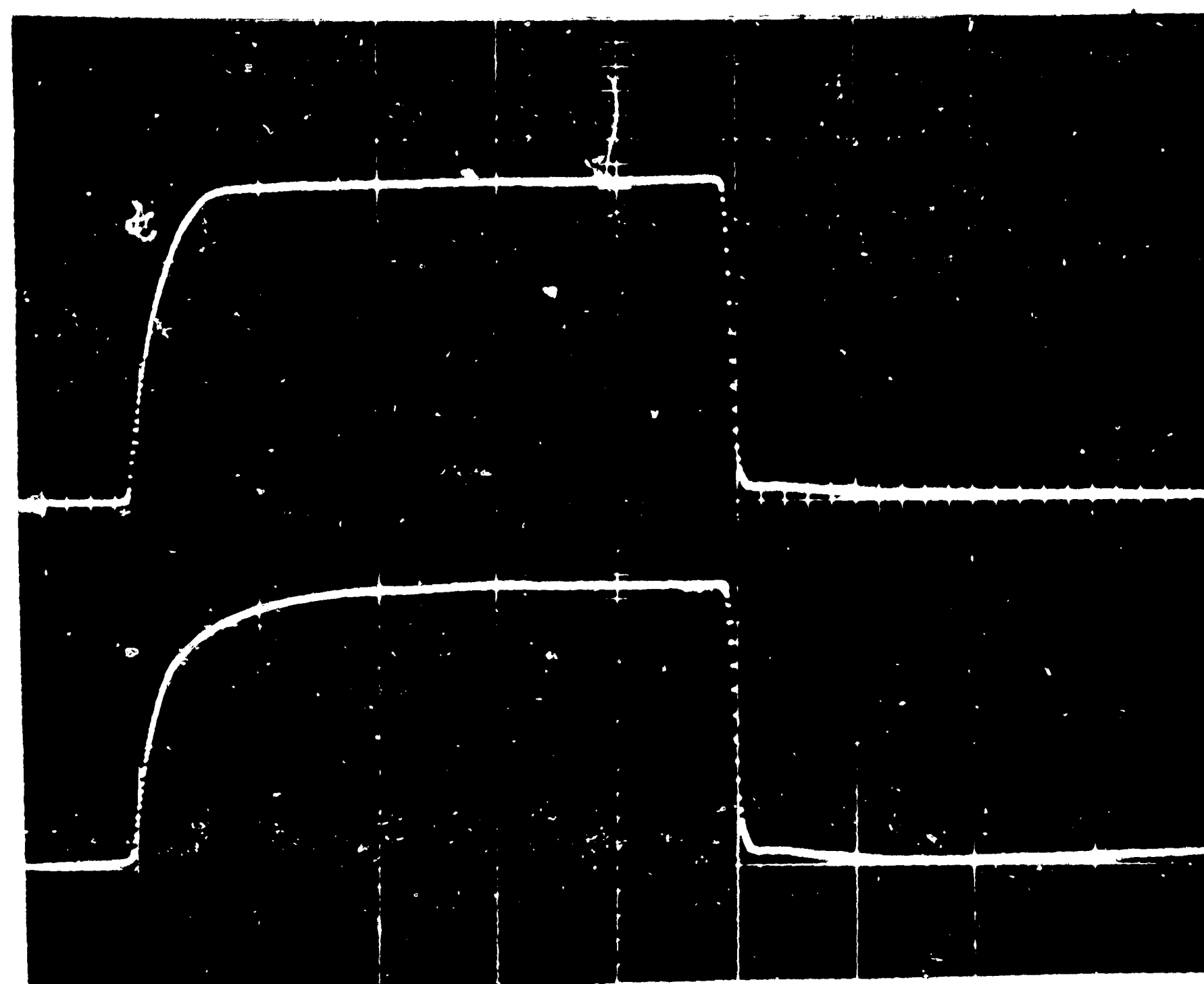
Type DL No. 254D₃ Temp. +125°C Vcc +4.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>502.</u>	<u>499.</u>	<u>500.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.82</u>	<u>2.0</u>	<u>2.62</u>	<u>2.78</u>
T _r	<u>58.</u>	<u>54.</u>	<u>66.</u>	<u>49.</u>
T _f	<u>12.8</u>	<u>13.</u>	<u>13.</u>	<u>12.</u>
T _d		<u>2.0</u>	<u>2.0</u>	<u>2.0</u>
T _s		<u>4.0</u>	<u>1.0</u>	<u>1.6</u>
T _{pd}		<u>1.5</u>	<u>2.5</u>	<u>2.0</u>

GENERAL MICRO-ELECTRONICS

Type DL No. 254D₃ Temp. +25°C Vcc 4.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>505.</u>	<u>500.</u>	<u>497.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.84</u>	<u>1.58</u>	<u>2.26</u>	<u>2.68</u>
T _r	<u>51.</u>	<u>33.</u>	<u>84.</u>	<u>56.</u>
T _f	<u>13.</u>	<u>13.</u>	<u>13.</u>	<u>13.</u>
T _d		<u>0.</u>	<u>1.0</u>	<u>1.6</u>
T _s		<u>4.2</u>	<u>2.0</u>	<u>1.0</u>
T _{pd}		<u>2.0</u>	<u>2.0</u>	<u>2.5</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DL No. 254D3 Temp. -40°C Vcc +4.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>509.</u>	<u>502.</u>	<u>497.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.92</u>	<u>1.37</u>	<u>2.12</u>	<u>2.82</u>
T _r	<u>60.</u>	<u>31.</u>	<u>86.</u>	<u>69.</u>
T _f	<u>12.</u>	<u>14.</u>	<u>12.</u>	<u>12.</u>
T _d		<u>1.0</u>	<u>1.0</u>	<u>2.0</u>
T _s		<u>4.0</u>	<u>3.5</u>	<u>1.0</u>
T _{pd}		<u>2.5</u>	<u>1.5</u>	<u>3.0</u>

Type DL No. 254D3 Temp. -55°C Vcc +4.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>511.</u>	<u>503.</u>	<u>497.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.86</u>	<u>1.26</u>	<u>2.0</u>	<u>2.82</u>
T _r	<u>62.</u>	<u>29.</u>	<u>86.</u>	<u>74.</u>
T _f	<u>12.</u>	<u>12.</u>	<u>11.</u>	<u>12.</u>
T _d		<u>1.0</u>	<u>1.0</u>	<u>2.0</u>
T _s		<u>5.0</u>	<u>3.0</u>	<u>1.0</u>
T _{pd}		<u>2.5</u>	<u>1.9</u>	<u>3.5</u>

GENERAL MICRO-ELECTRONICS

Type DL No. 254D3 Temp. +85°C Vcc +4.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>506.</u>	<u>503.</u>	<u>500.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.80</u>	<u>1.87</u>	<u>1.32</u>	<u>1.72</u>
T _r	<u>55.</u>	<u>40.</u>	<u>62.</u>	<u>56.</u>
T _f	<u>13.</u>	<u>13.</u>	<u>12.5</u>	<u>13.</u>
T _d		<u>1.0</u>	<u>2.0</u>	<u>2.0</u>
T _s		<u>4.0</u>	<u>2.7</u>	<u>1.6</u>
T _{pd}		<u>2.0</u>	<u>2.0</u>	<u>2.3</u>

Type DL No. 254D3 Temp. +125°C Vcc +4.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>3.0</u>	Vcc <u>4.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>504.</u>	<u>501.</u>	<u>500.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>2.78</u>	<u>2.02</u>	<u>2.50</u>	<u>2.70</u>
T _r	<u>57.</u>	<u>47.</u>	<u>71.</u>	<u>56.</u>
T _f	<u>13.</u>	<u>14.</u>	<u>14.</u>	<u>14.</u>
T _d		<u>2.0</u>	<u>2.0</u>	<u>2.0</u>
T _s		<u>3.0</u>	<u>2.0</u>	<u>2.0</u>
T _{pd}		<u>2.3</u>	<u>2.7</u>	<u>3.0</u>

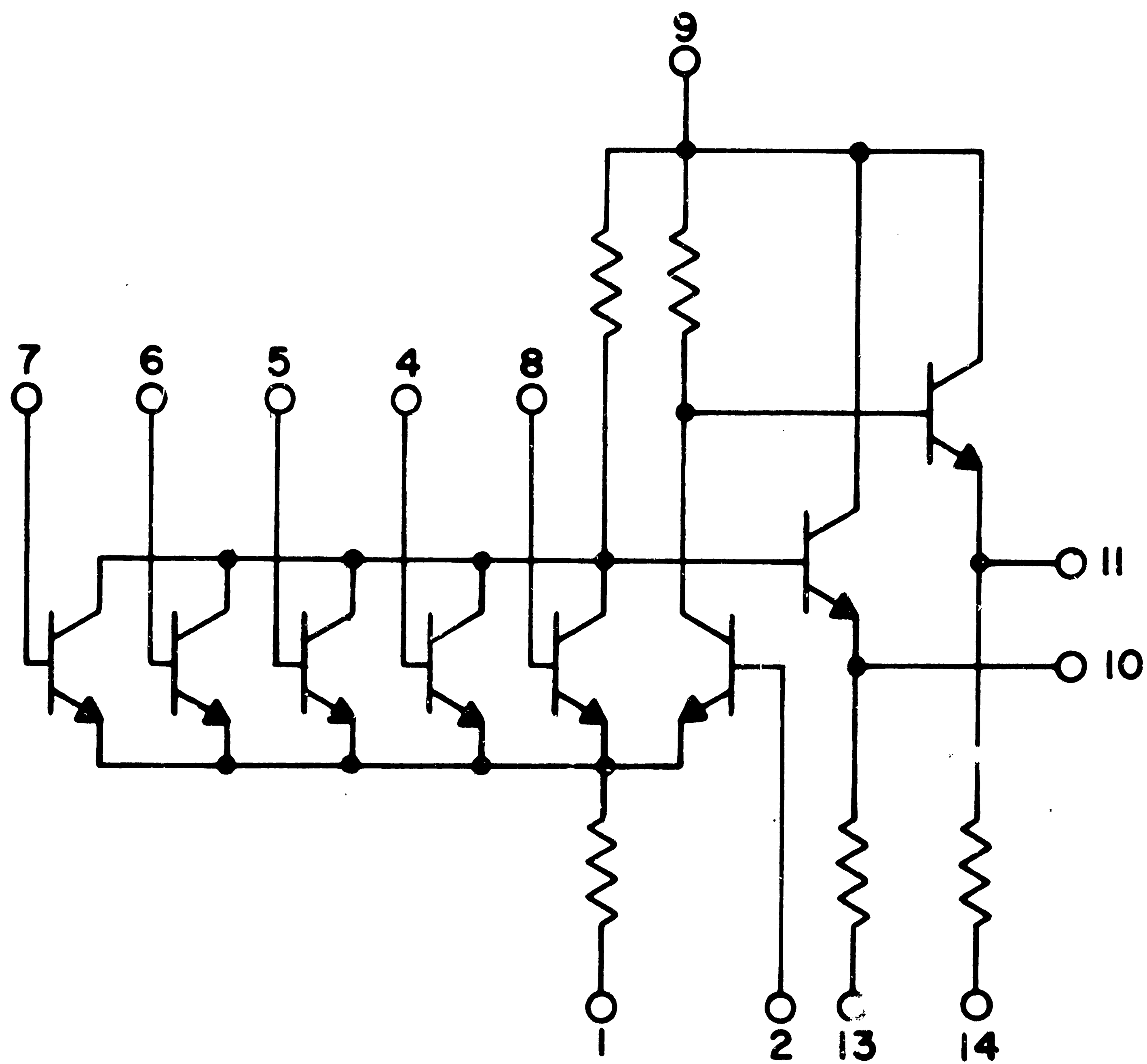
EVALUATION

The General Microelectronics CML Gate is a five-input OR/NOR Gate. The gate requires 3 power supplies for an input and output based on zero volts d-c. For this condition the supplies are: $V_9 = 2.0$, $V_1, 13, 14 = -2.5$, and $V_2 = +1.0$. The circuit is packaged in a 14 lead flat-pack or a 10 pin TO-5 can.

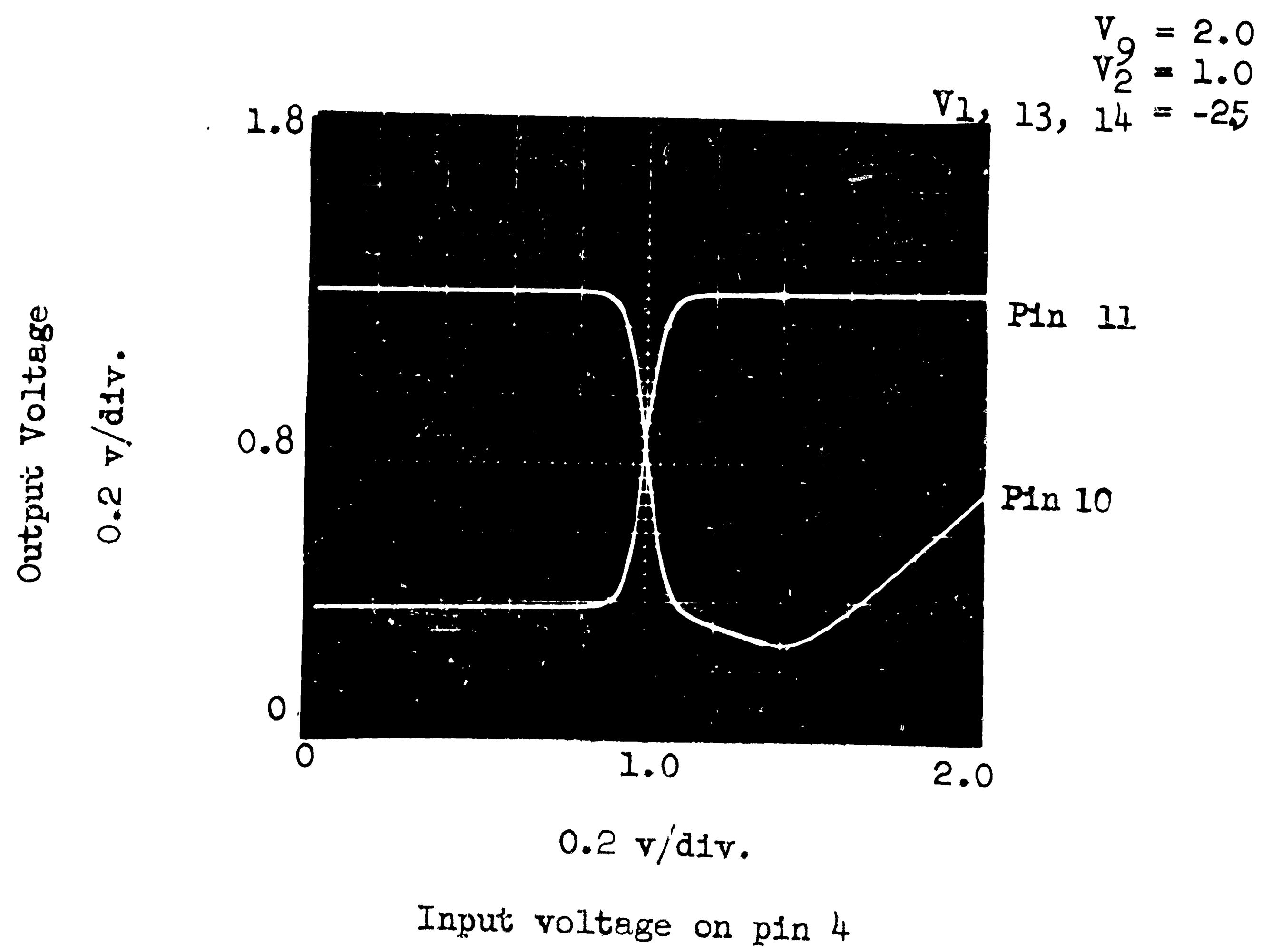
Typical curves were plotted on a transistor curve tracer.

DYNAMIC TEST PROCEDURE

1. The testing circuit block diagram is shown preceeding the dynamic data.
2. The input pulse was set to have a repetition rate of 1 MC and a pulse width of 500 ns. The temperature was regulated at +25°C with a load of 1 on the test circuit.
3. The supplies were set at $V_9 = +2.0$, $V_1, 13, 14 = -2.5$, and $V_2 = +1.0$.
4. The above procedure was repeated for temperatures of -55°C, -40°C, +25°C, +85°C, and +125°C.
5. The above procedure was repeated for a load of 3.



543G5 5 - INPUT CML GATE ELEMENT



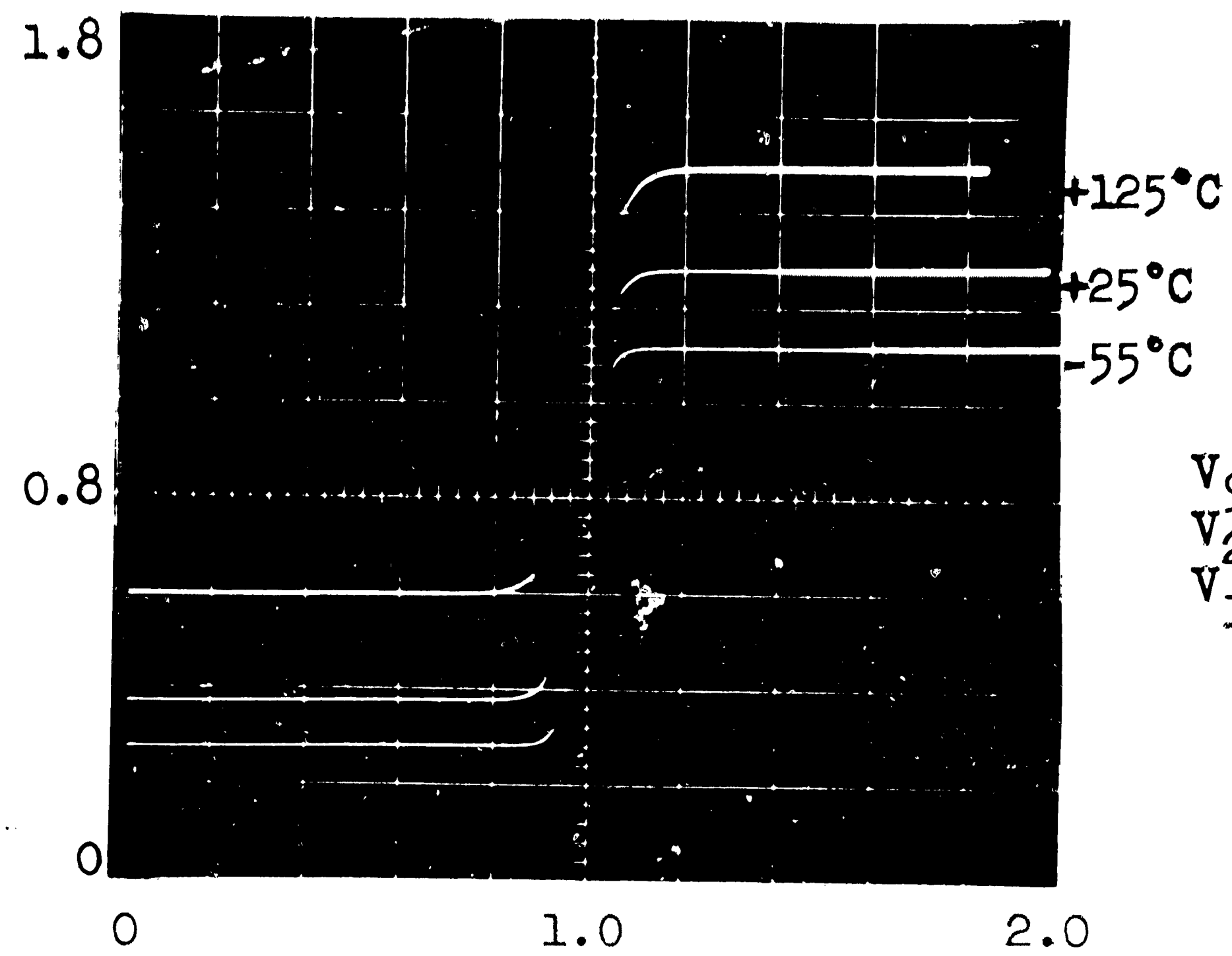
INPUT OUTPUT CHARACTERISTICS

CML - 543G5

3.2.143

Output voltage on pin 11

0.2 v/div.



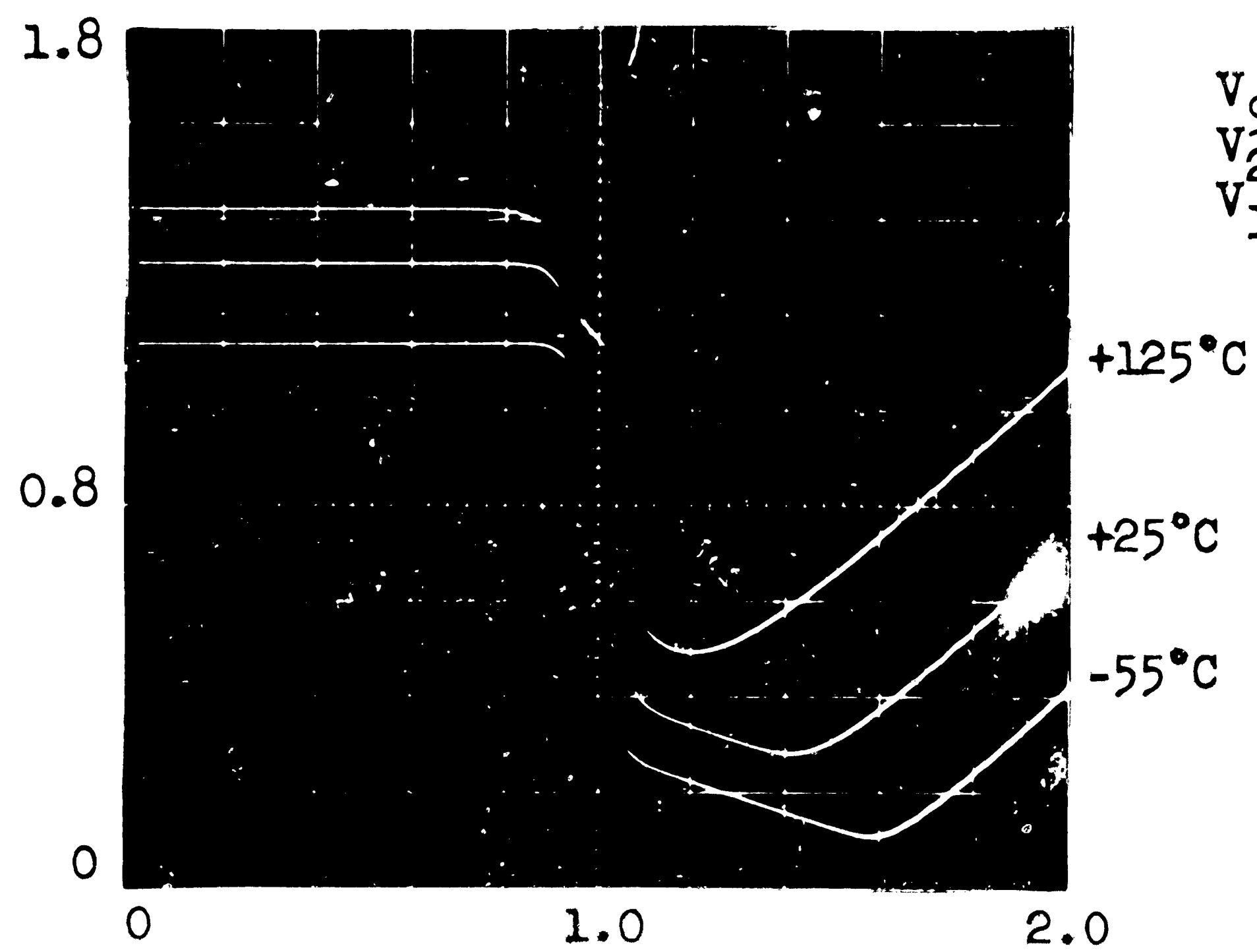
$V_9 = 2.0$
 $V_2 = 1.0$
 $V_{1, 13, 14} = -2.5$

0.2 v/div.

Input voltage on pin 4

Output voltage on pin 10

0.2 v/div.



$V_9 = 2.0$
 $V_2 = 1.0$
 $V_{1, 13, 14} = -2.5$

0.2 v/div.

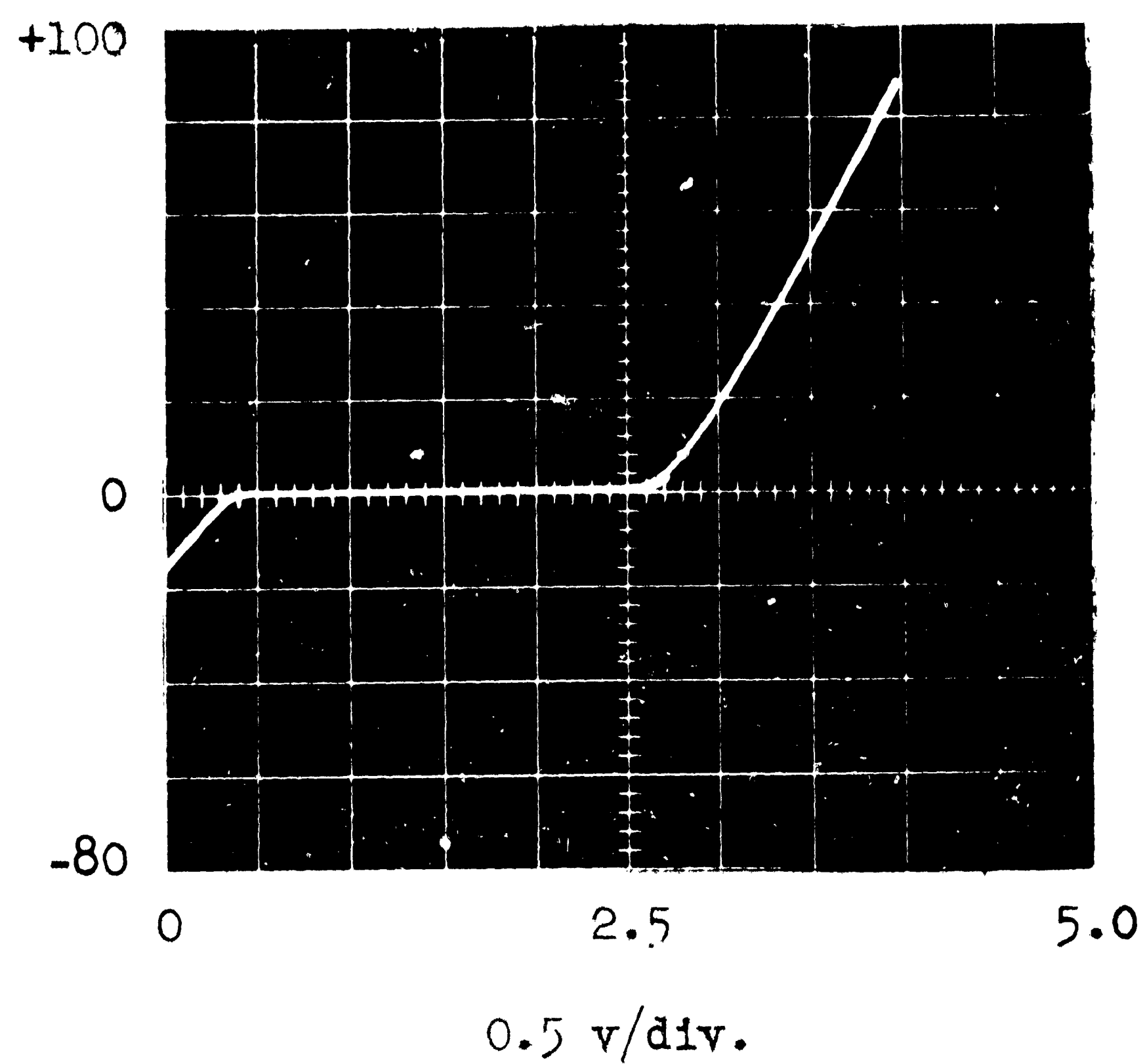
Input voltage on pin 4

INPUT OUTPUT CHARACTERISTICS

CML 543G5

3.2.144

Output current into pin 11
20 ma/div.

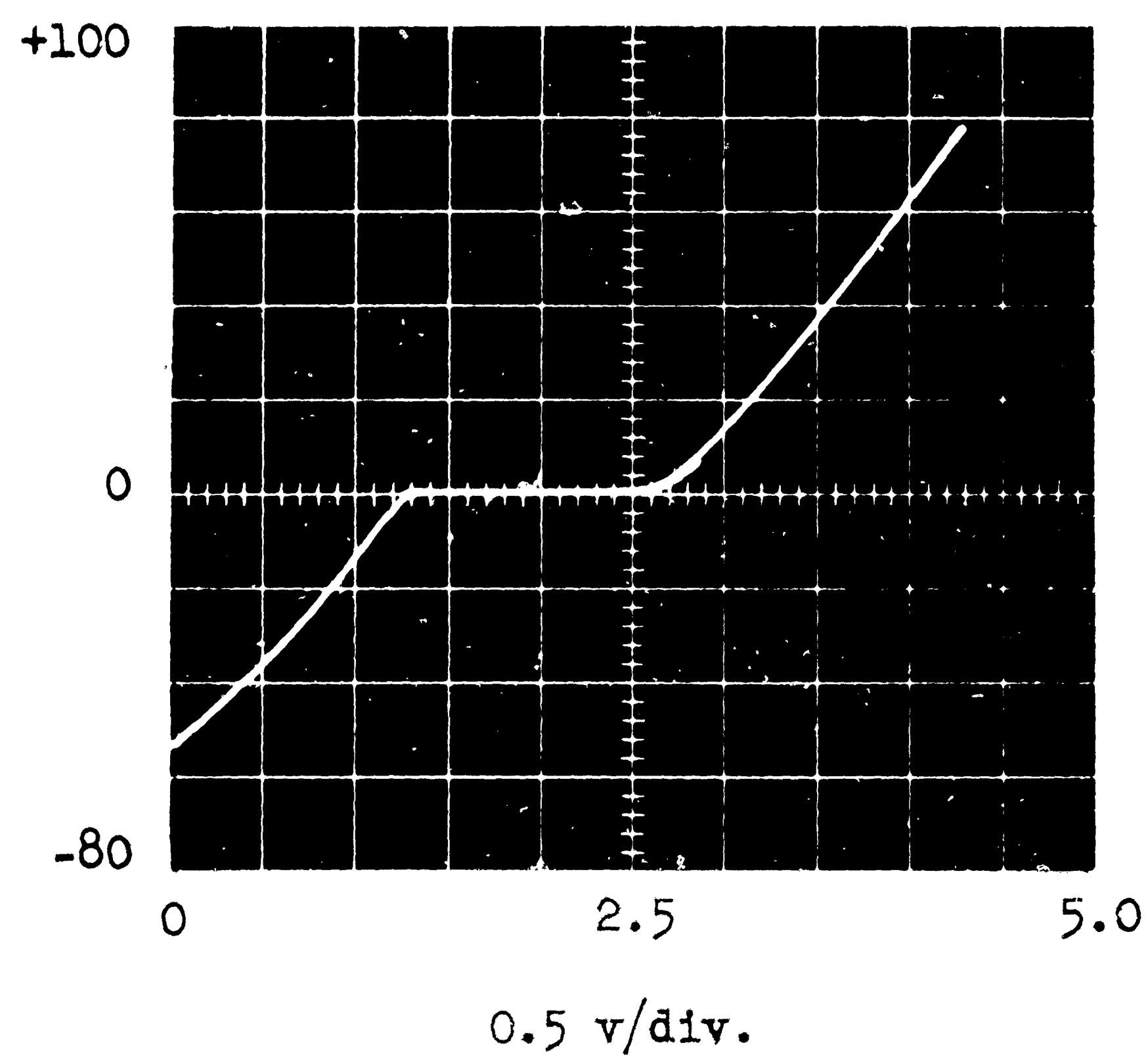


$V_9 = 2.0$
 $V_2 = 1.0$
 $V_{1, 13, 14} = -2.5$

"0" on Inputs

Output voltage on pin 11

Output current into pin 10
20 ma/div.



$V_9 = 2.0$
 $V_2 = 1.0$
 $V_{1, 13, 14} = -2.5$

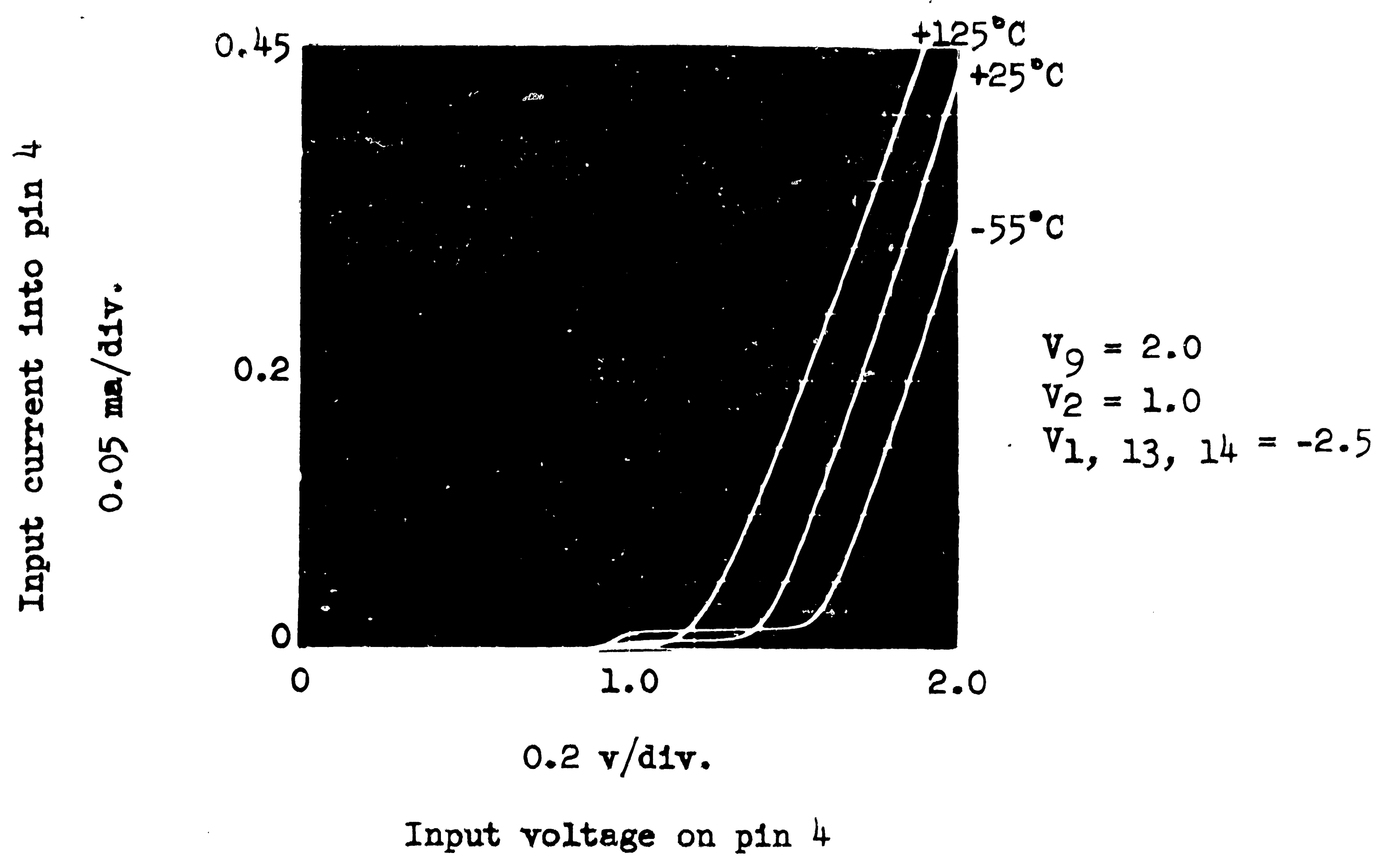
"0" on Inputs

Output voltage on pin 10

OUTPUT CHARACTERISTICS

CML 543G5

3.2.145

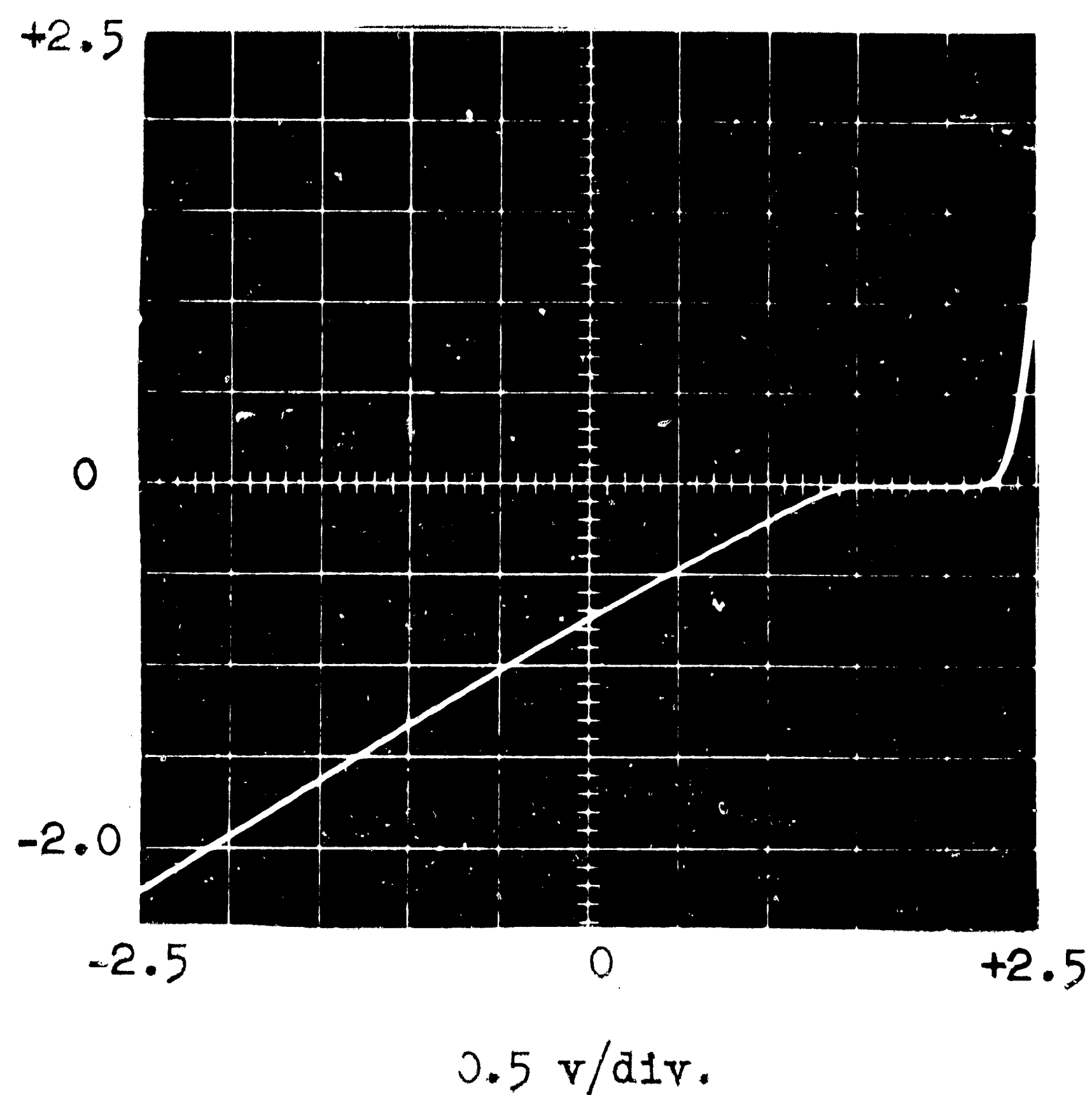


INPUT CHARACTERISTICS

CML 543G5

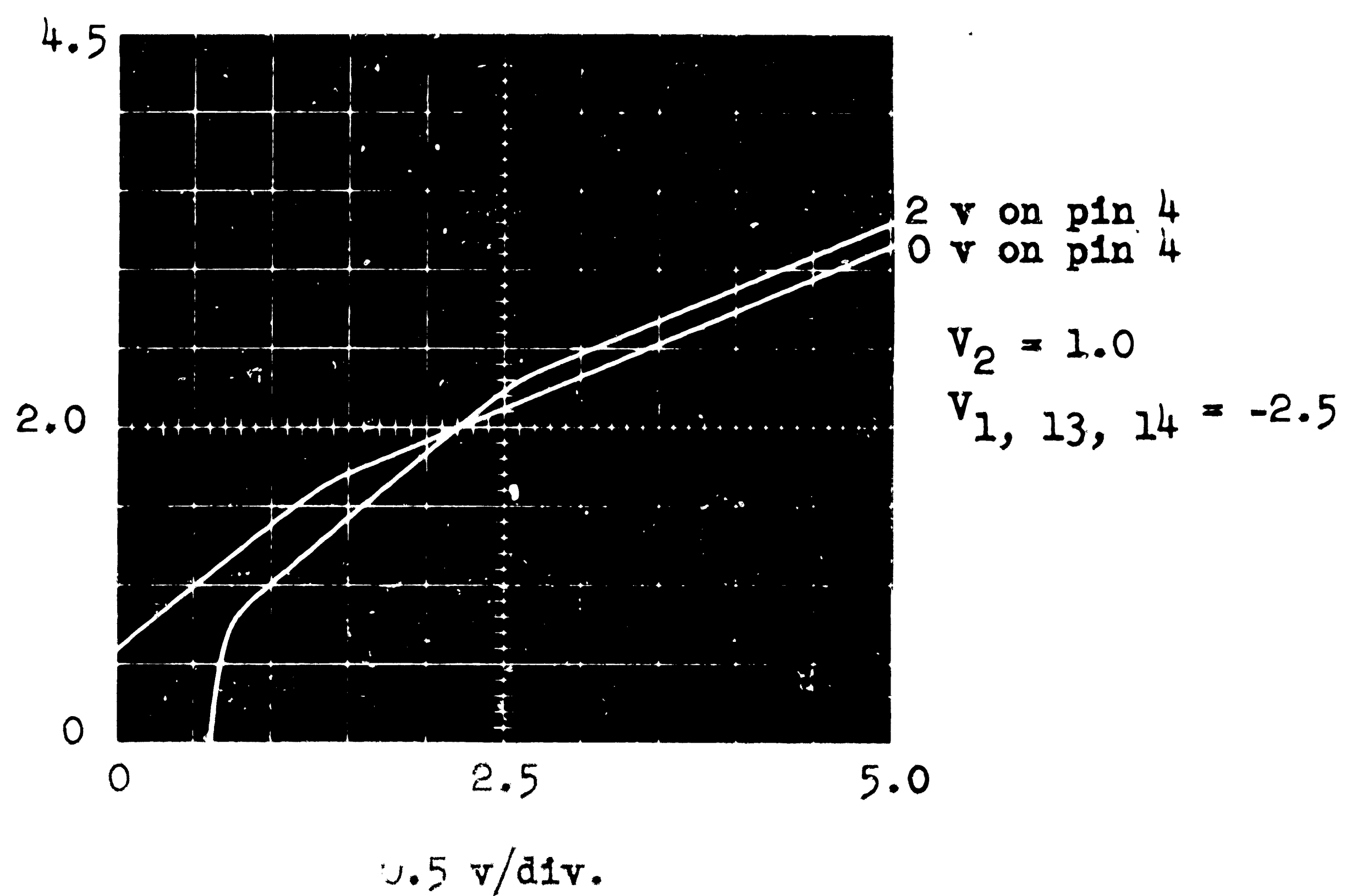
3.2.146

Current into pins 1, 13, 14
0.5 mA/div.



Supply voltage on pins 1, 13, 14

Current into pin 9
0.5 mA/div.

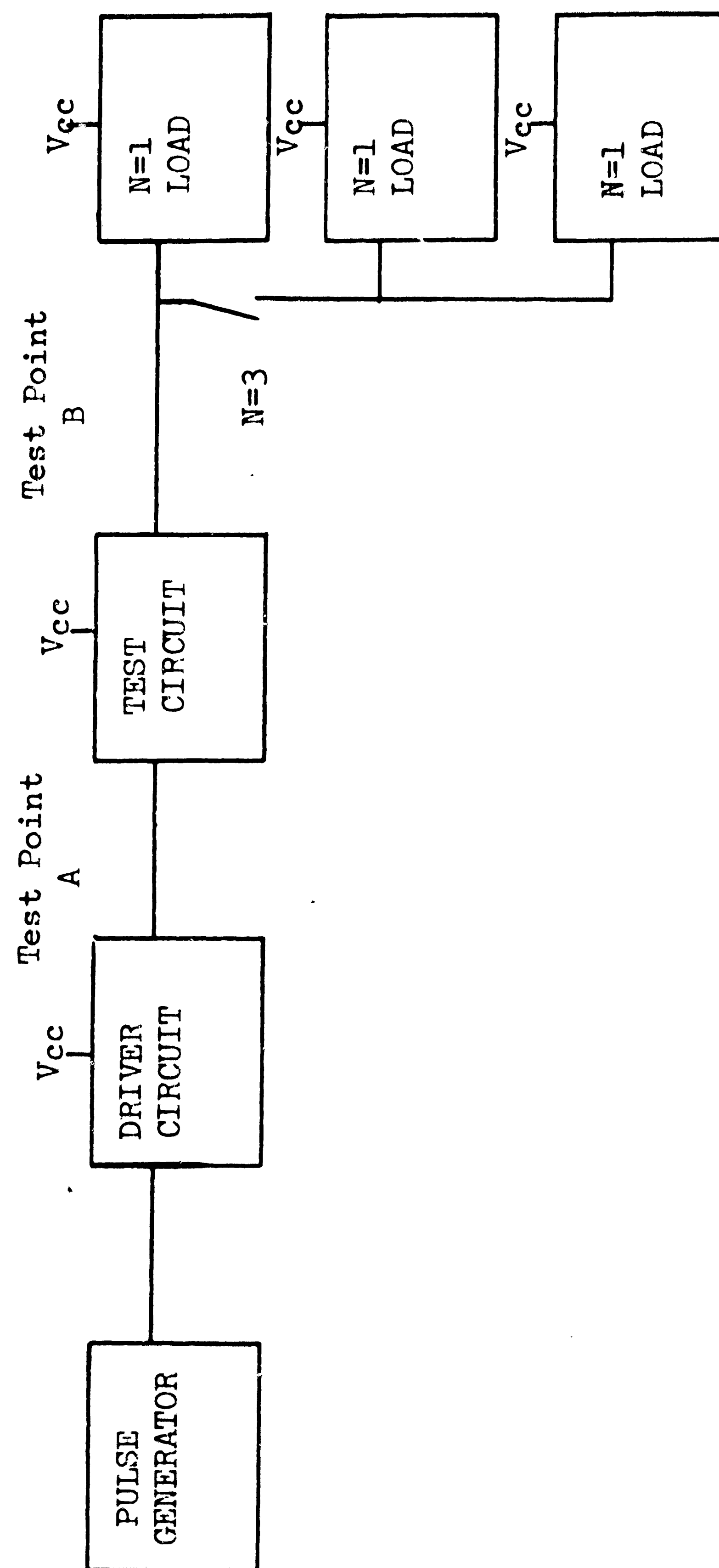


Supply voltage on pin 9

POWER DISSIPATION CURVES

CML 543G5

3.2.147

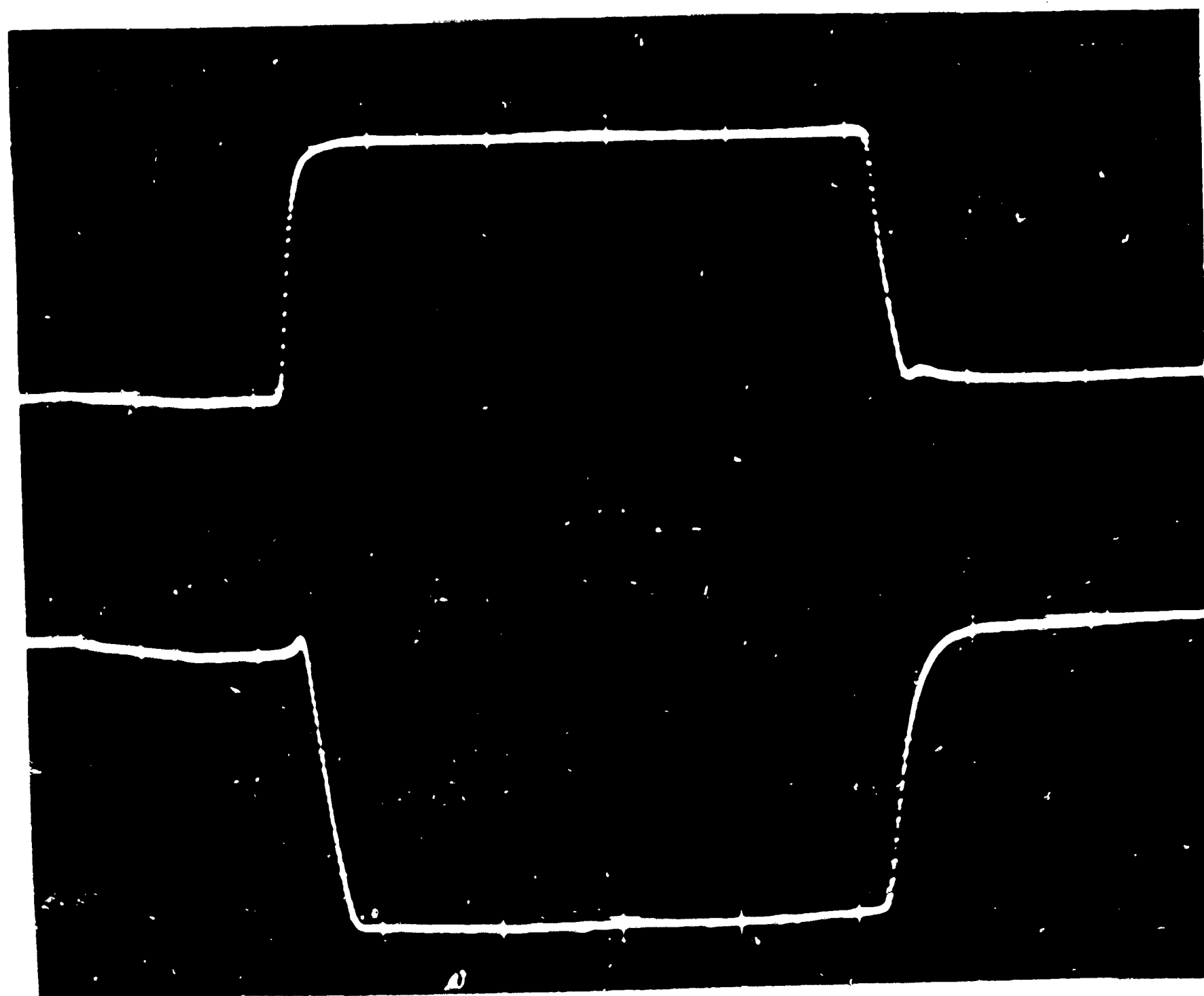


TEST CIRCUIT FOR CML 543G5

GENERAL MICRO-ELECTRONICS

Type CML No. 543G5 Temp. +25°C V_0 +2.0 V_2 -2.5 V_1 +1.0 N= 1

	TEST CKT. INPUT	TEST CKT. OUTPUT
		V_0 <u>+2.0</u>
		V_2 <u>-2.5</u>
		V_1 <u>+1.0</u>
Pulse Width	<u>500.</u>	<u>487.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>0.83</u>	<u>1.06</u>
T_r	<u>16.6</u>	<u>55.</u>
T_f	<u>21.3</u>	<u>29.4</u>
T_d		<u>14.3</u>
T_s		<u>5.7</u>
T_{pd}		<u>15.</u>



Test Circuit Input

Test Circuit Output

NOTE: Pins 1, 13 and 14 are tied common and referred to as Pin 1

GENERAL MICRO-ELECTRONICS

Type CML No. 543G5 Temp -40°C V_9 +2.0 V_2 -2.5 V_1 +1.0 N= 1

	TEST CKT INPUT	TEST CKT OUTPUT
		V_9 <u>+2.0</u>
		V_2 <u>-2.5</u>
		V_1 <u>+1.0</u>
Pulse Width	<u>500.</u>	<u>478.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>0.796</u>	<u>0.918</u>
T_r	<u>15.7</u>	<u>47.5</u>
T_f	<u>21.2</u>	<u>27.2</u>
T_d		<u>18.4</u>
T_s		<u>3.2</u>
T_{pd}		<u>15.5</u>

Type CML No. 543G5 Temp -40°C V_1 +2.0 V_4 -2.5 V_5 +1.0 N= 1

	TEST CKT INPUT	TEST CKT OUTPUT
		V_1 <u>+2.0</u>
		V_4 <u>-2.5</u>
		V_5 <u>+1.0</u>
Pulse Width	<u>500.</u>	<u>474.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>0.76</u>	<u>0.86</u>
T_r	<u>15.5</u>	<u>50.</u>
T_f	<u>22.</u>	<u>46.</u>
T_d		<u>19.</u>
T_s		<u>3.0</u>
T_{pd}		<u>17.</u>

GENERAL MICRO-ELECTRONICS

Type CML No. 543G5 Temp +85°C V_9 +2.0 V_2 -2.5 V_1 +1.0 N= 1

	TEST CKT INPUT	TEST CKT OUTPUT
		V_9 <u>+2.0</u>
		V_2 <u>-2.5</u>
		V_1 <u>+1.0</u>
Pulse Width	<u>500.</u>	<u>497.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>0.872</u>	<u>1.08</u>
T_r	<u>19.</u>	<u>74.</u>
T_f	<u>24.</u>	<u>31.</u>
T_d		<u>14.</u>
T_s		<u>15.</u>
T_{pd}		<u>21.</u>

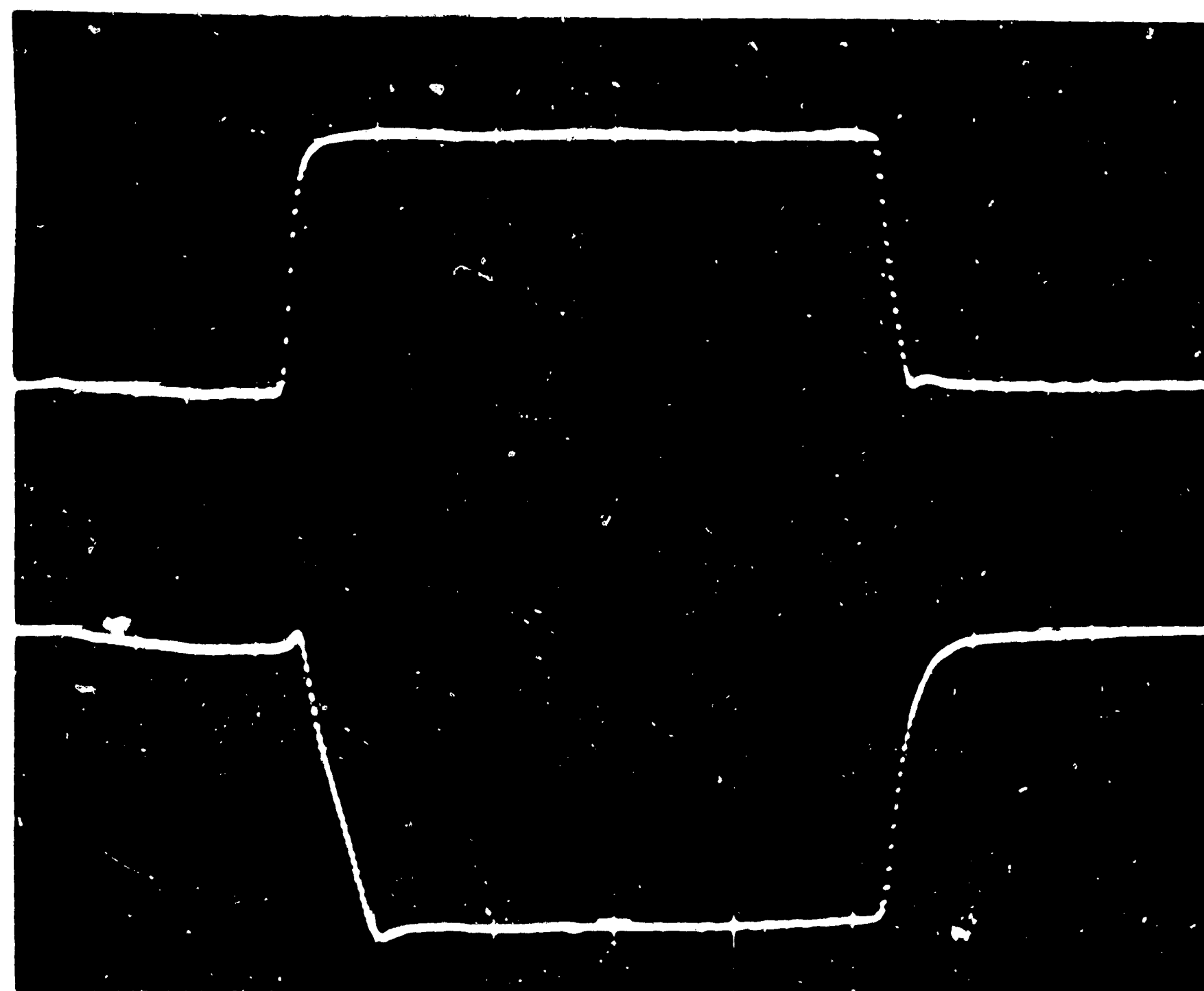
Type CML No. 543G5 Temp +125°C V_1 +2.0 V_4 -2.5 V_5 +1.0 N= 1

	TEST CKT INPUT	TEST CKT OUTPUT
		V_1 <u>+2.0</u>
		V_4 <u>-2.5</u>
		V_5 <u>+1.0</u>
Pulse Width	<u>500.</u>	<u>507.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude.	<u>0.75</u>	<u>0.76</u>
T_r	<u>21.</u>	<u>72.</u>
T_f	<u>22.</u>	<u>25.</u>
T_d		<u>11.</u>
T_s		<u>24.</u>
T_{pd}		<u>21.</u>

GENERAL MICRO-ELECTRONICS

Type CML No. 543G5 Temp. +25°C V_9 +2.0 V_2 -2.5 V_1 +1.0 N= 3

	TEST CKT. INPUT	TEST CKT. OUTPUT
		V_9 <u>+2.0</u>
		V_2 <u>-2.5</u>
		V_1 <u>+1.0</u>
Pulse Width	<u>500.</u>	<u>479.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>0.84</u>	<u>1.02</u>
T_r	<u>17.1</u>	<u>58.</u>
T_f	<u>21.7</u>	<u>47.8</u>
T_d		<u>15.</u>
T_s		<u>6.0</u>
T_{pd}		<u>21.</u>



Test Circuit Input

Test Circuit Output

GENERAL MICRO-ELECTRONICS

Type CML No. 543G5 Temp -40°C V_0 +2.0 V_2 -2.5 V_1 +1.0 N= 3

	TEST CKT INPUT	TEST CKT OUTPUT
		V_0 <u>+2.0</u>
		V_2 <u>-2.5</u>
		V_1 <u>+1.0</u>
Pulse Width	<u>500.</u>	<u>470.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>0.792</u>	<u>0.912</u>
T_r	<u>15.7</u>	<u>50.</u>
T_f	<u>21.1</u>	<u>43.</u>
T_d		<u>19.7</u>
T_s		<u>3.5</u>
T_{pd}		<u>20.</u>

Type CML No. 543G5 Temp -55°C V_1 +2.0 V_4 -2.5 V_5 +1.0 N= 3

	TEST CKT INPUT	TEST CKT OUTPUT
		V_1 <u>+2.0</u>
		V_4 <u>-2.5</u>
		V_5 <u>+1.0</u>
Pulse Width	<u>500.</u>	<u>468.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>0.774</u>	<u>0.872</u>
T_r	<u>16.</u>	<u>50.</u>
T_f	<u>21.5</u>	<u>41.</u>
T_d		<u>21.</u>
T_s		<u>3.0</u>
T_{pd}		<u>20.</u>

GENERAL MICRO-ELECTRONICS

Type CML No. 543G5 Temp +85°C V_9 +2.0 V_2 -2.5 V_1 +1.0 N= 3

	TEST CKT INPUT	TEST CKT OUTPUT
		V_9 <u>+2.0</u>
		V_2 <u>-2.5</u>
		V_1 <u>+1.0</u>
Pulse Width	<u>500.</u>	<u>489.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>0.88</u>	<u>1.04</u>
T_r	<u>18.6</u>	<u>75.</u>
T_f	<u>24.</u>	<u>52.</u>
T_d		<u>16.</u>
T_s		<u>17.</u>
T_{pd}		<u>25.</u>

Type CML No. 543G5 Temp +125°C V_1 +2.0 V_4 -2.5 V_5 +1.0 N= 3

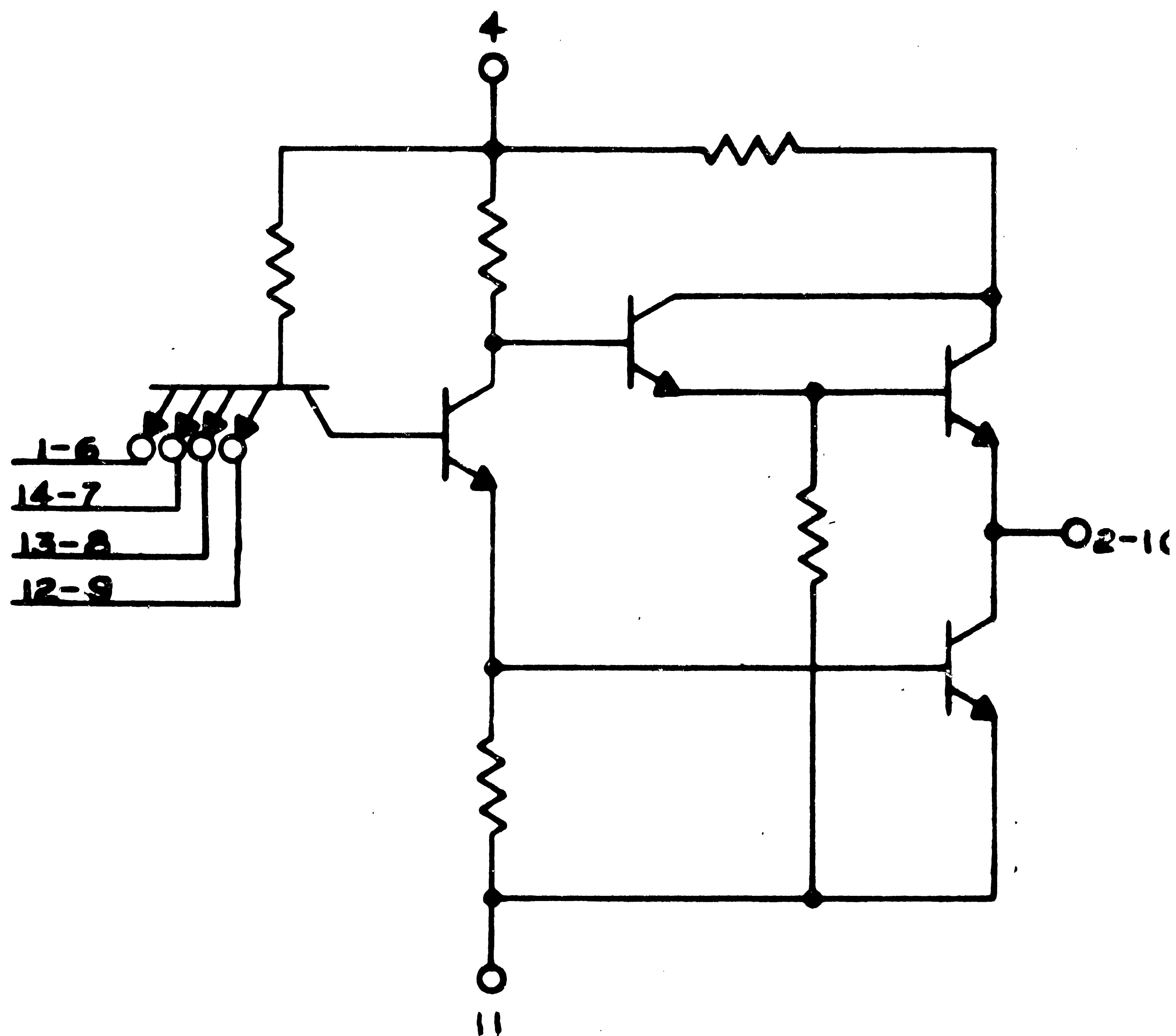
	TEST CKT INPUT	TEST CKT OUTPUT
		V_1 <u>+2.0</u>
		V_4 <u>-2.5</u>
		V_5 <u>+1.0</u>
Pulse Width	<u>500.</u>	<u>504.</u>
Repetition Rate	<u>1MC</u>	<u>1MC</u>
Pulse Amplitude	<u>0.75</u>	<u>0.74</u>
T_r	<u>21.</u>	<u>66.</u>
T_f	<u>22.</u>	<u>42.</u>
T_d		<u>11.3</u>
T_s		<u>25.</u>
T_{pd}		<u>25.</u>

EVALUATION

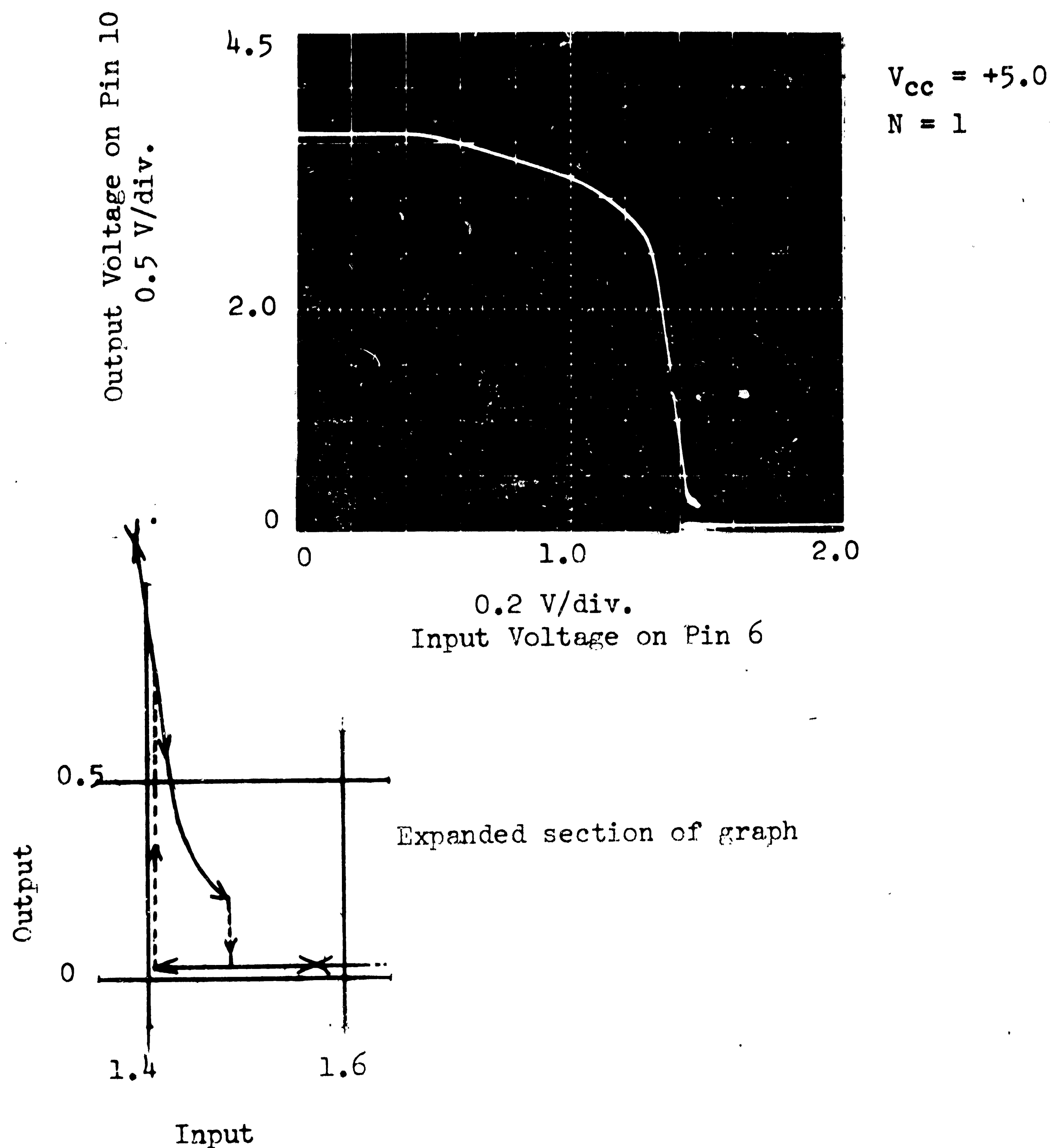
The General Microelectronics line of Transistor Transistor Logic (TTL) consists of two NAND Gates; the 265G8 which is an eight input gate and the 265D4 which is a dual four input gate. The circuits are typical TTL NAND Gates with an additional output non-inverting power stage enabling them to drive high fan-outs with high capacitive loading. Both circuits were tested statically on a transistor curve tracer.

DYNAMIC TEST PROCEDURE

1. The testing circuit block diagram is shown preceding the dynamic data for the 365D4.
2. The input pulse was set to have a repetition rate of 1 MC and a pulse width of 500 ns. The temperature was regulated at +25°C with a load of 1 on the test circuit.
3. V_{cc} was set at +4.5 V and data taken. Data was also taken for V_{cc} of 5.0 V and 5.5 V.
4. The above procedure was repeated for temperatures of -40°C, -55°C, +85°C and +125°C.
5. The above procedure was repeated for test circuit loads of $N = 5$ and $N = 10$.



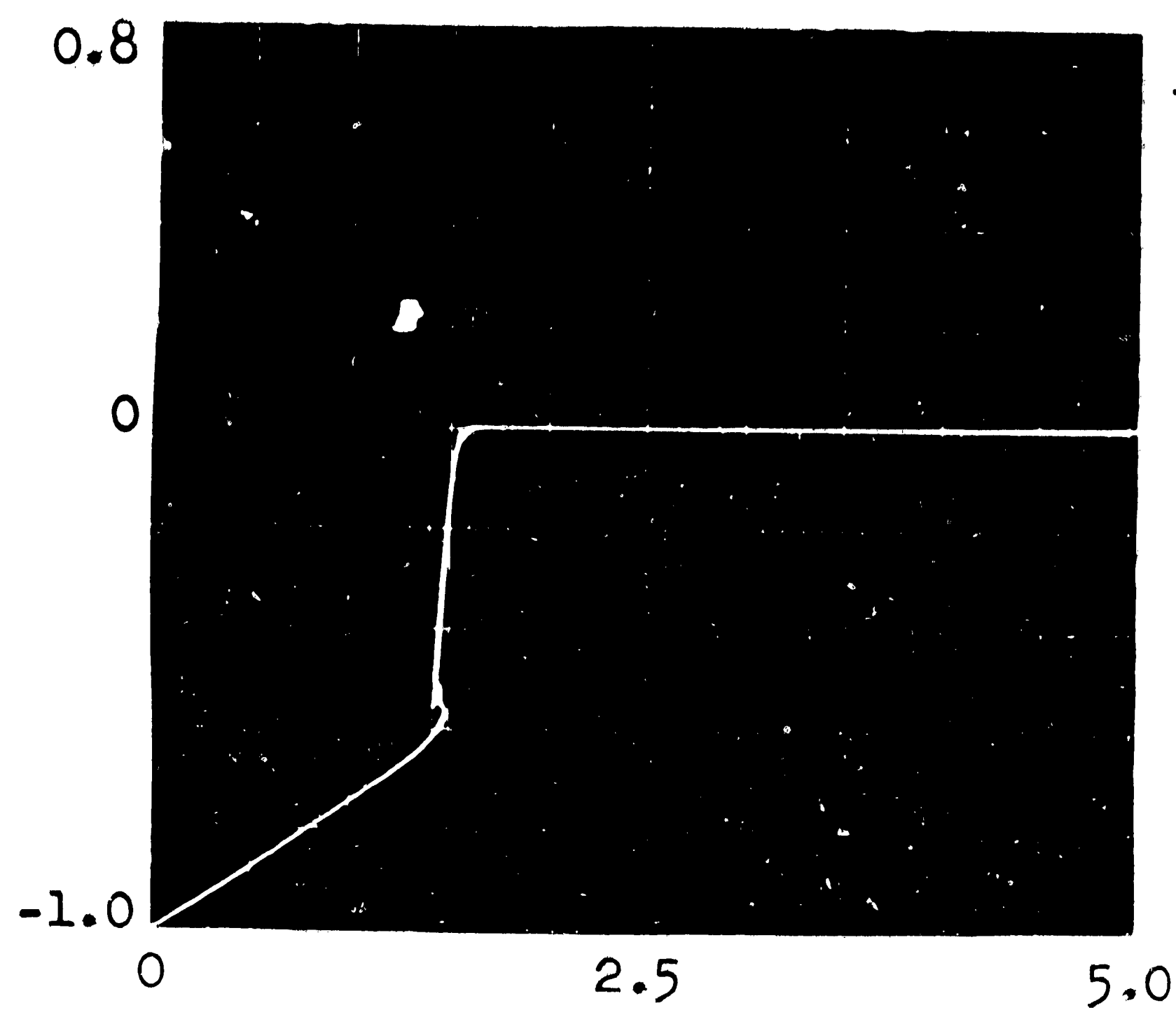
365D4 DUAL 4 - INPUT TTL GATE ELEMENT



NOTE: In the above graph, the output voltage followed the curve down to the knee where the input was approximately 1.44V. The output then dropped to the lowest potential. On the retrace the output stayed low until the input was down to approximately 1.40V where it rose vertically to meet the trace going high.

INPUT - OUTPUT CHARACTERISTICS
TTL 365D4

Input Current into pin 6
0.2 ma/div.

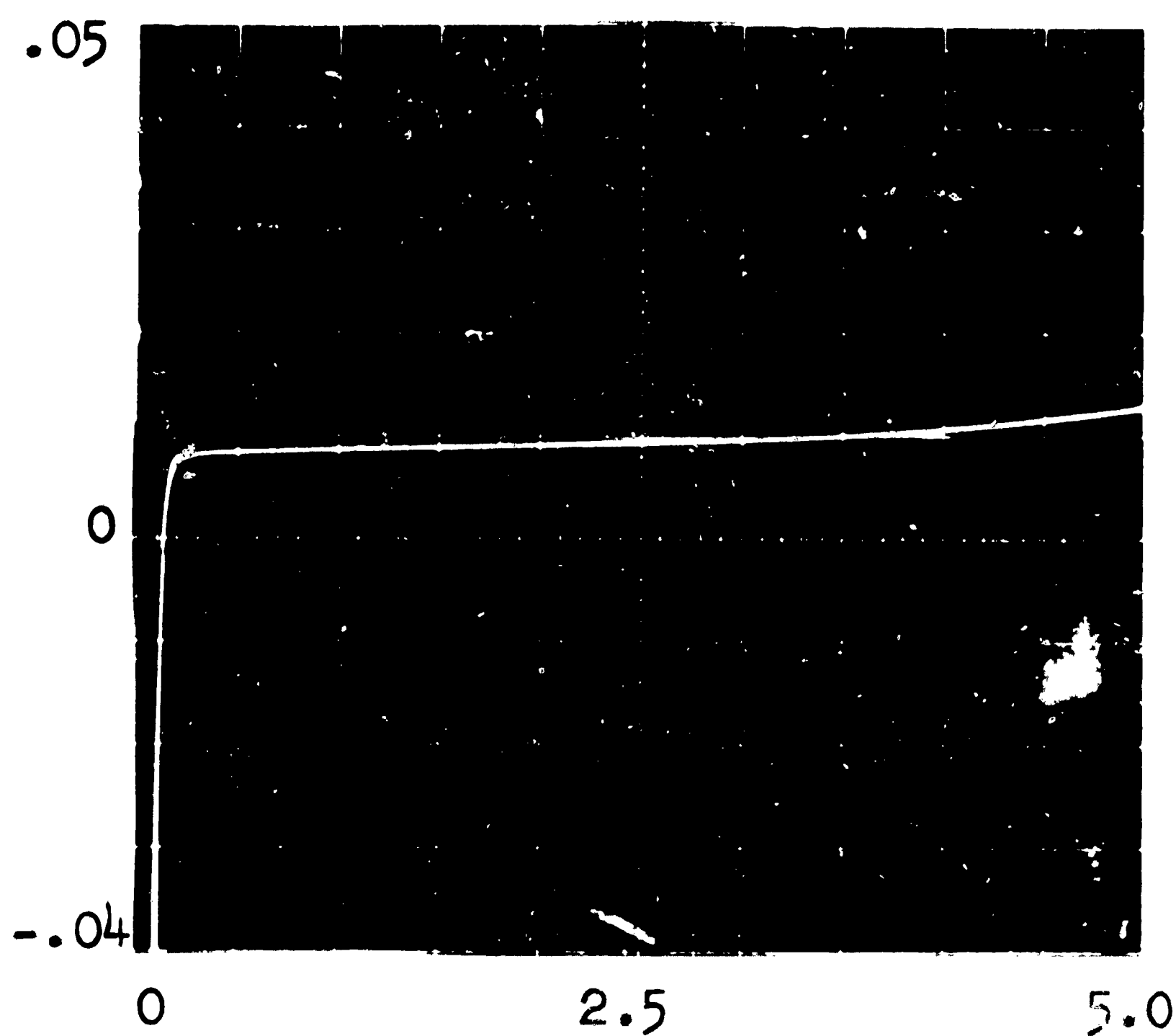


$V_{cc} = 5.0$
 $N = 1$

0.5 v/div.

Input voltage on pin 6

Input Current into pin 6
0.01 ma/div.



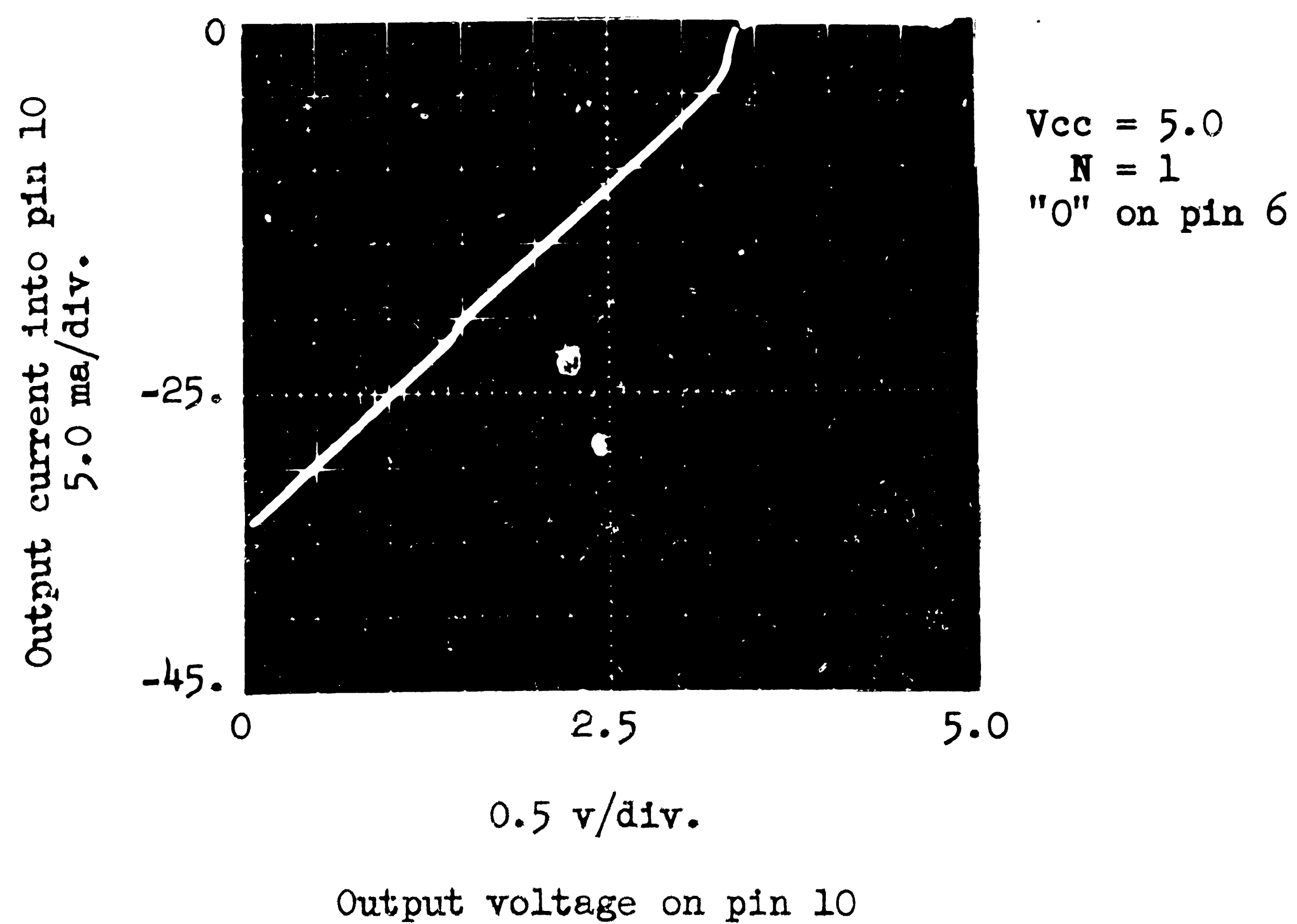
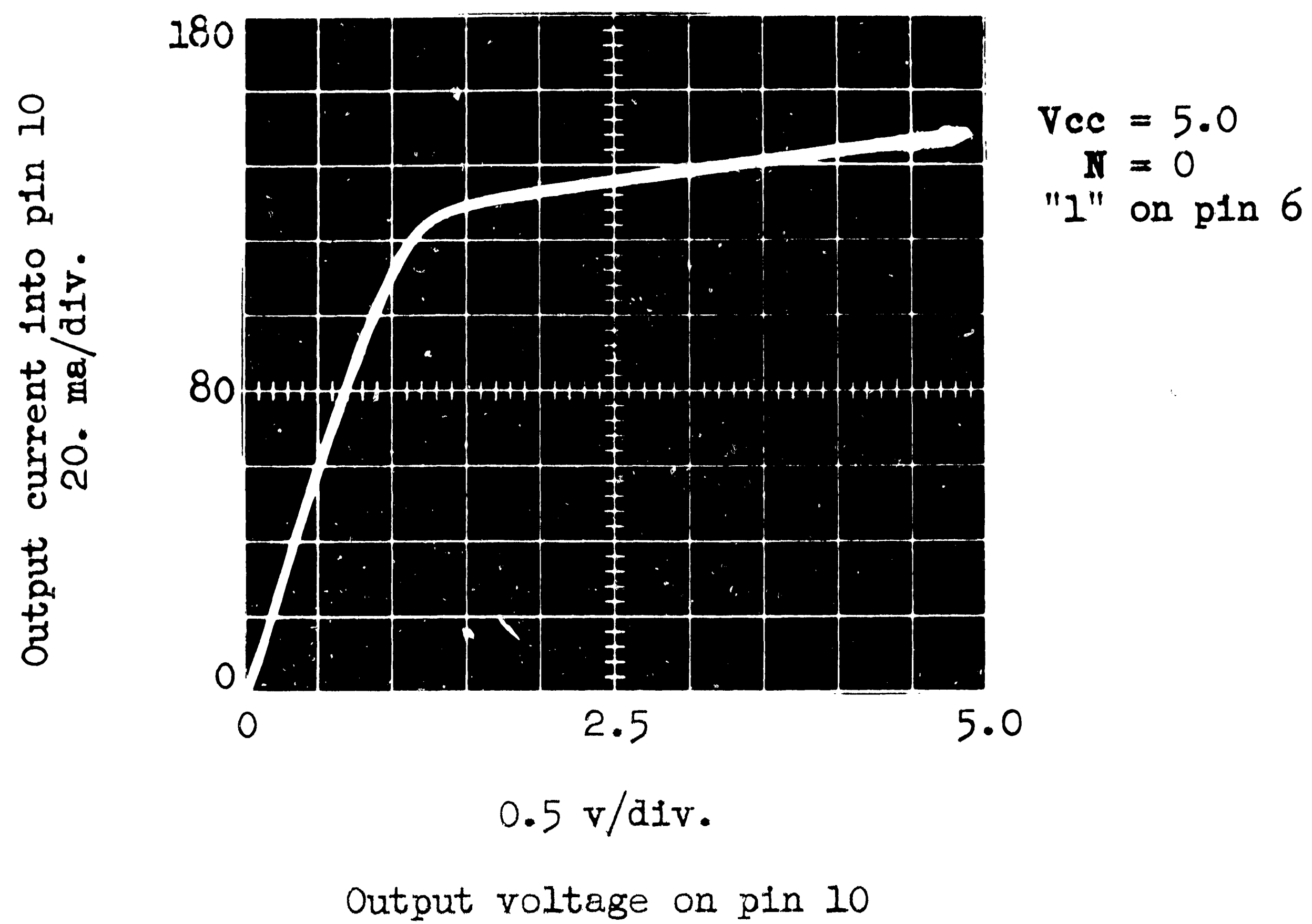
$V_{cc} = 5.0$
 $N = 1$
 $V_7 = 0$

0.5 v/div.

Input voltage on pin 6

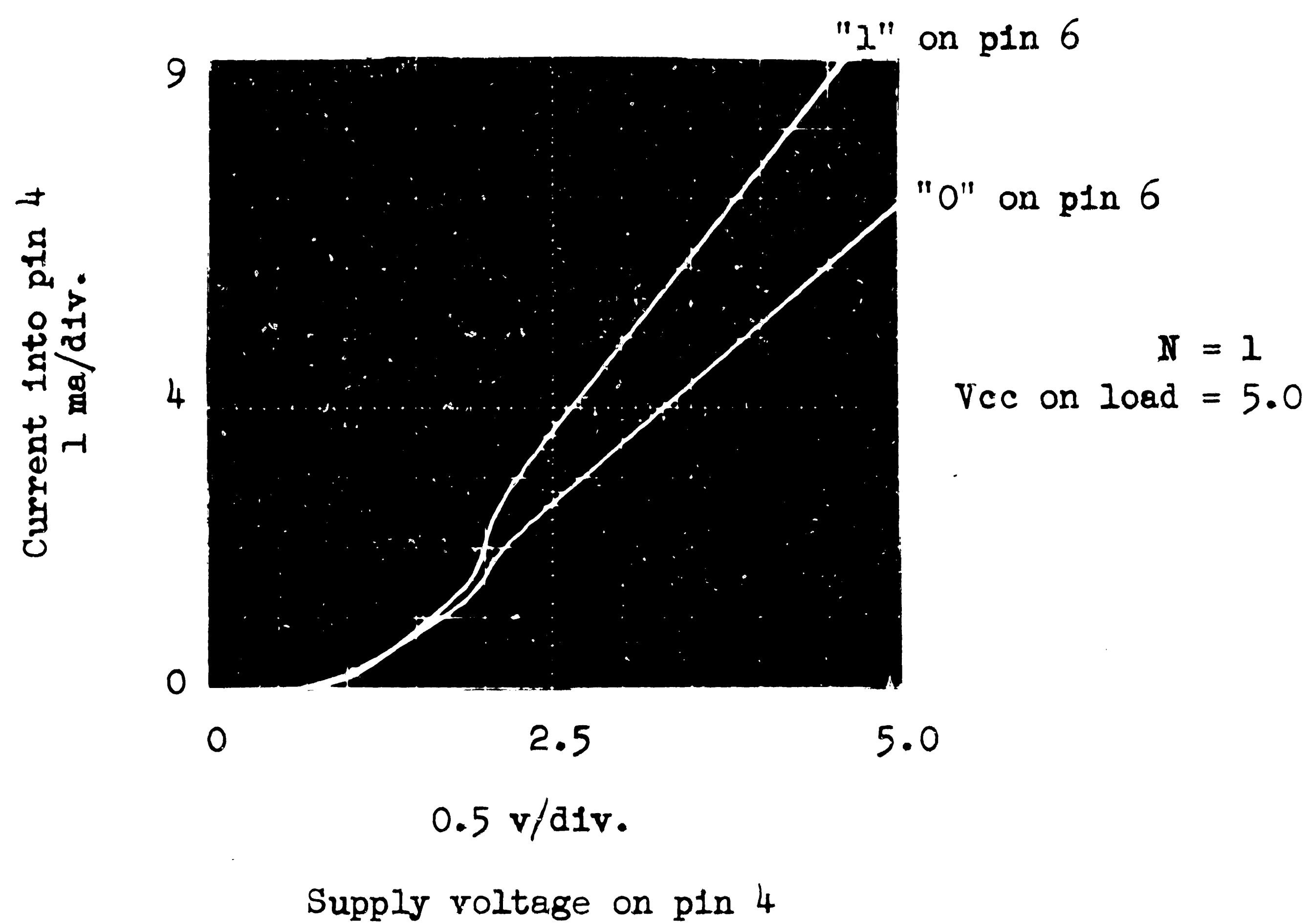
INPUT CHARACTERISTICS
TTL-365D4

3.2.158



OUTPUT CHARACTERISTICS
 TTL 365D4

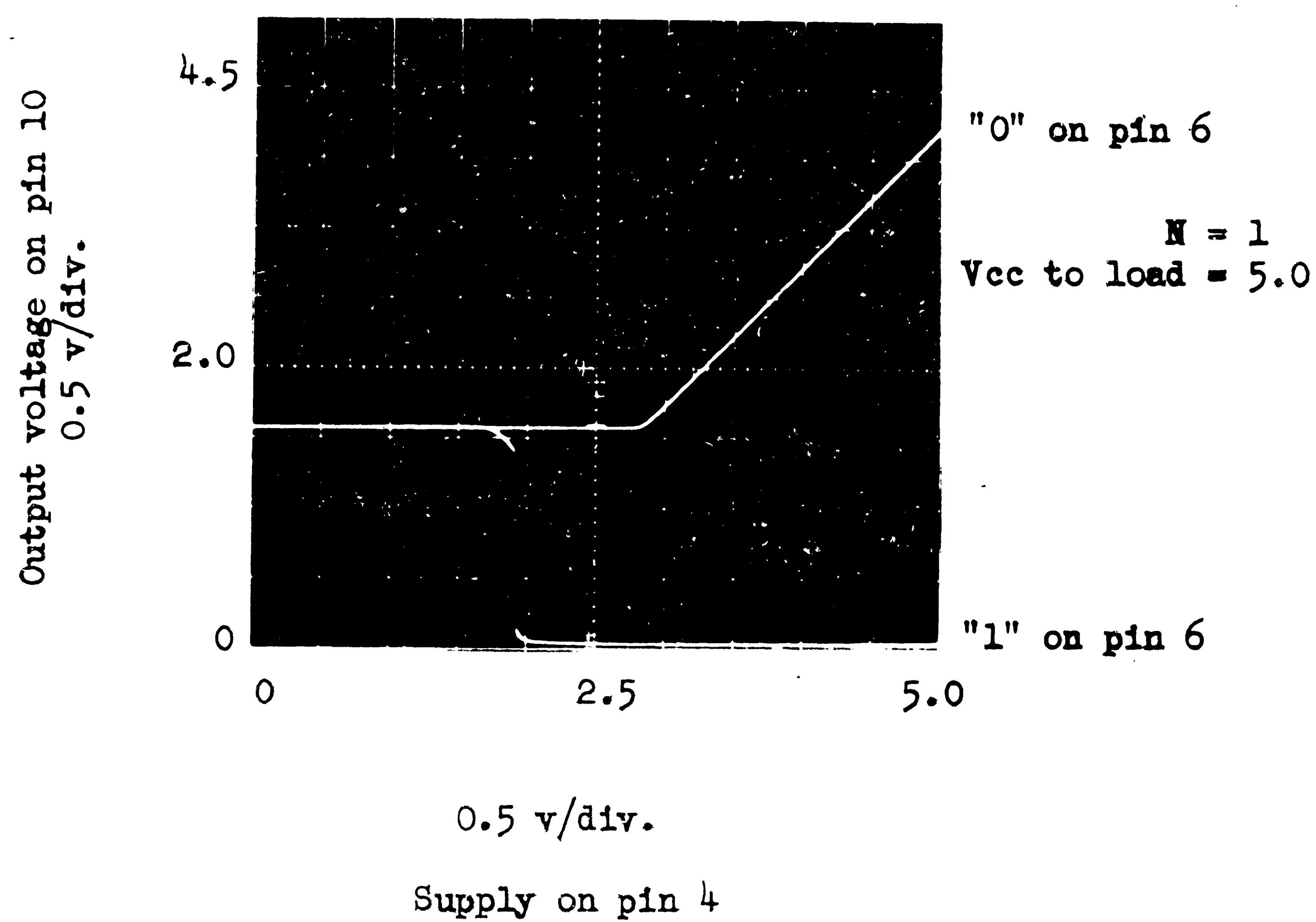
3.2.159



POWER DISSIPATION CURVES

TTL - 365D4

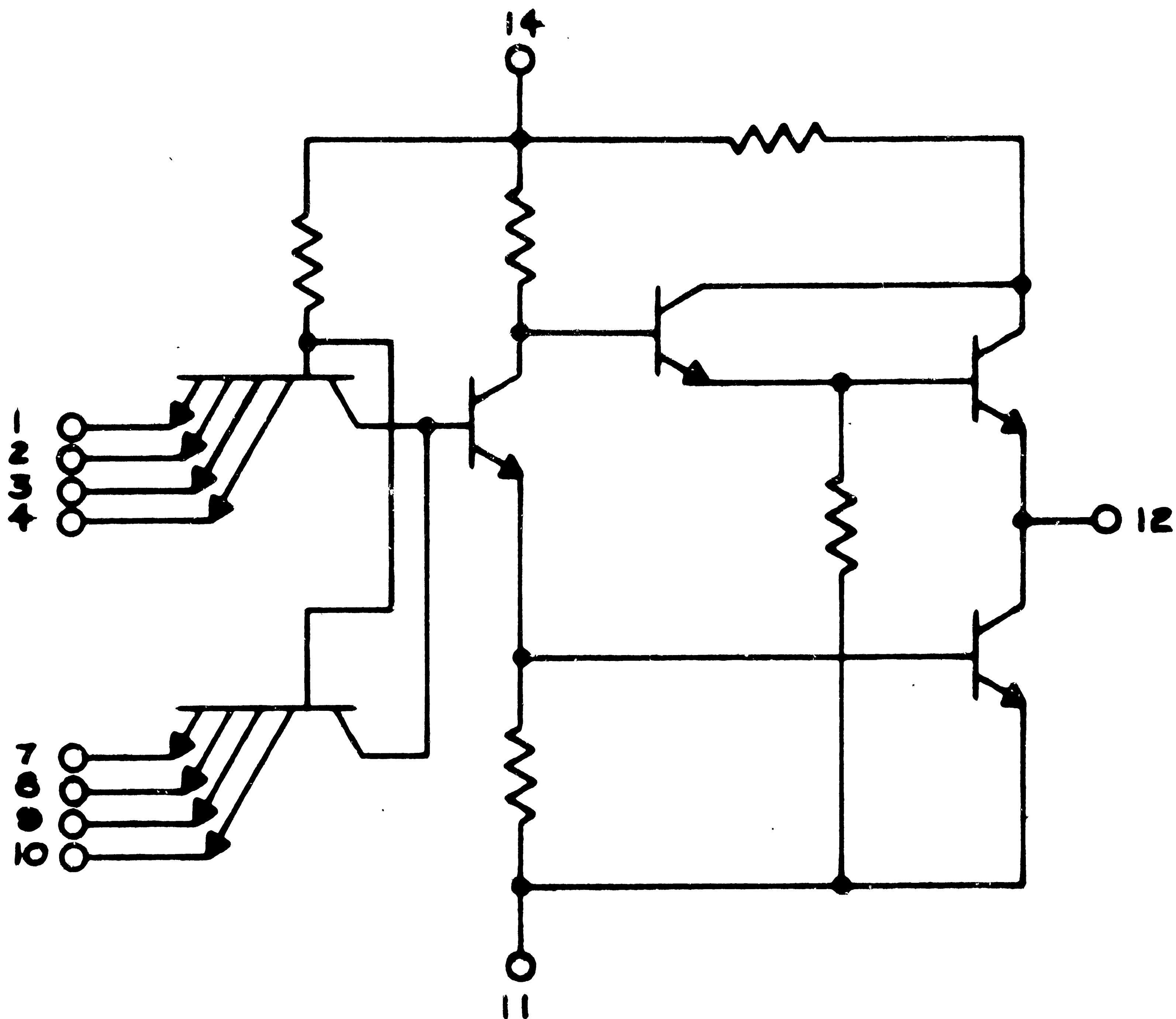
3.2.160



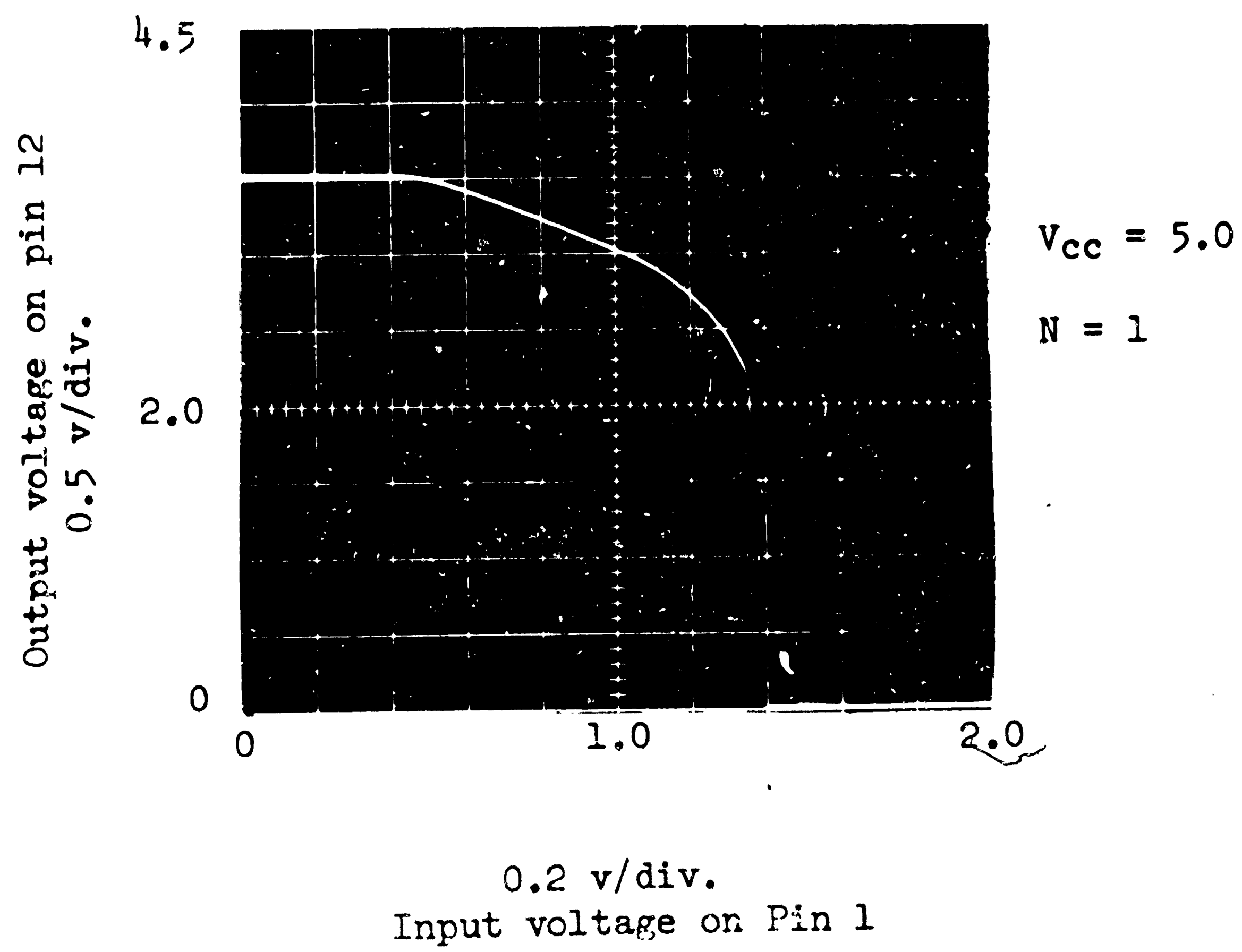
OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE

TTL 365D4

3.2.161



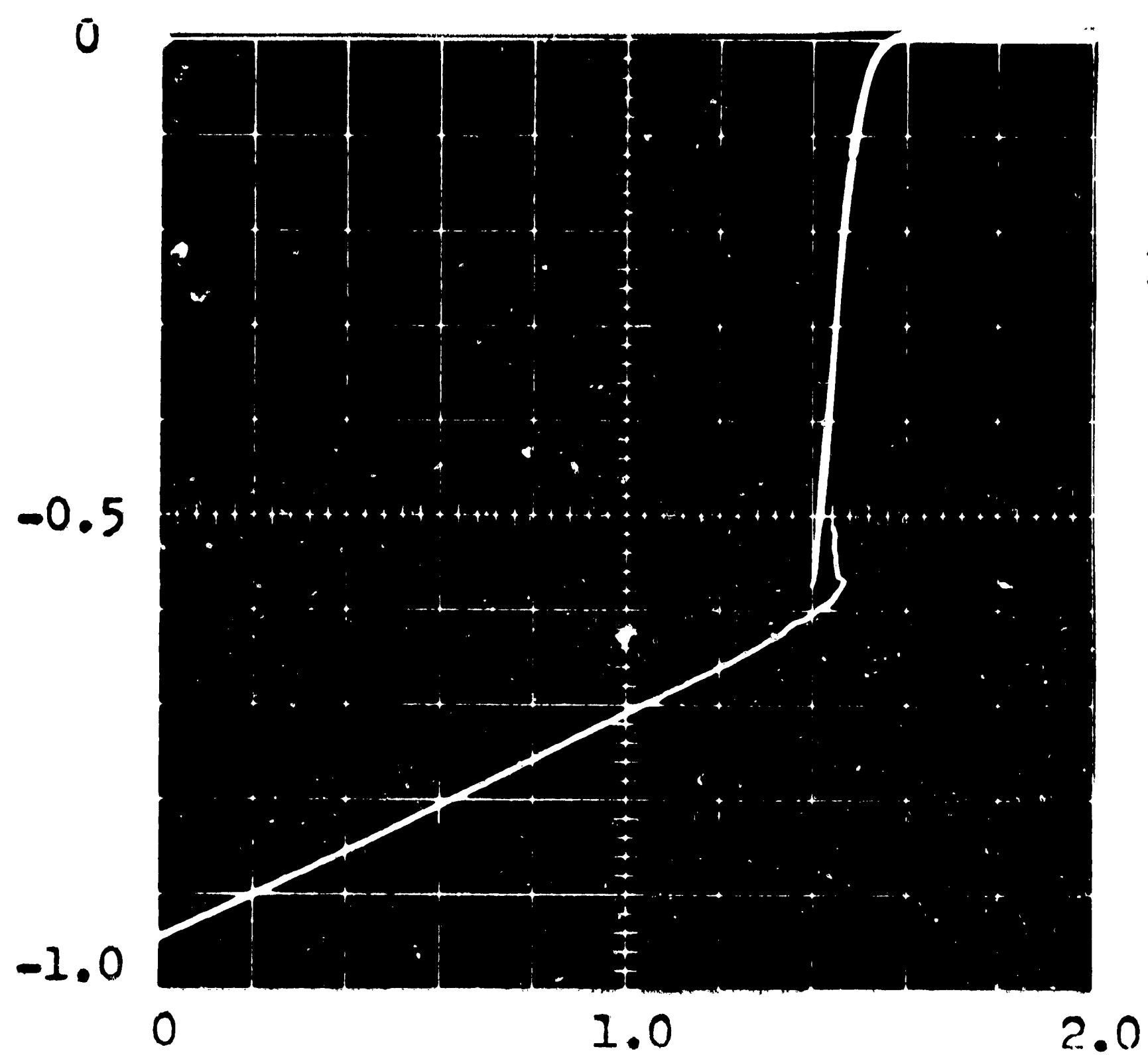
365G8 8 - INPUT TTL GATE ELEMENT



INPUT OUTPUT CHARACTERISTICS
TTL 365G8

3.2.163

Input current into Pin 1
0.1 ma/div.

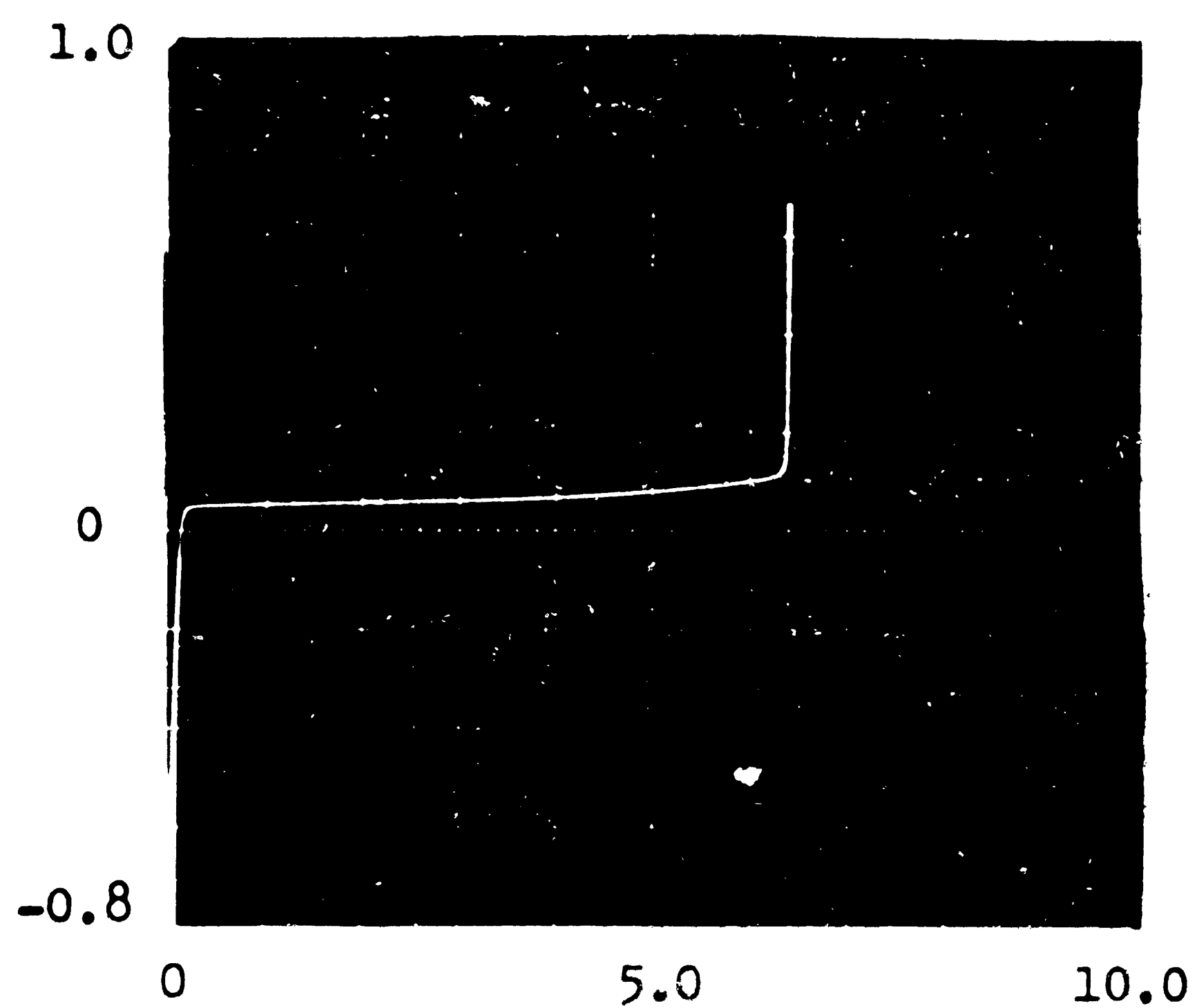


$V_{CC} = 5.0$

$N = 1$

0.2 v/div.
Input voltage on Pin 1

Input current into Pin 1
0.2 ma/div.



$V_{CC} = 5.0$

$N = 1$

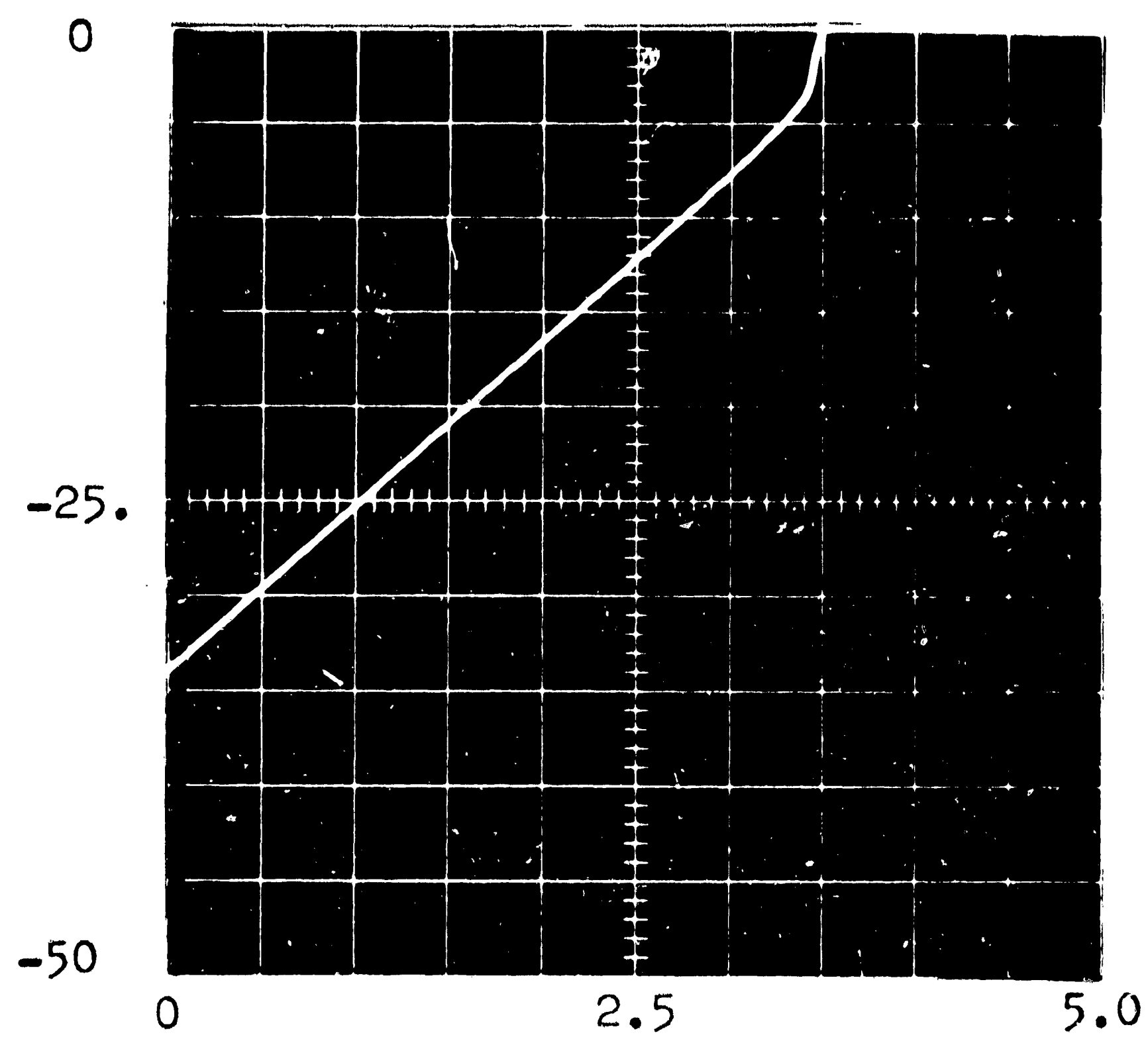
"0" on Pin 7

1 v/div.
Input voltage on Pin 1

INPUT CHARACTERISTICS
TTL 365G8

3.2.164

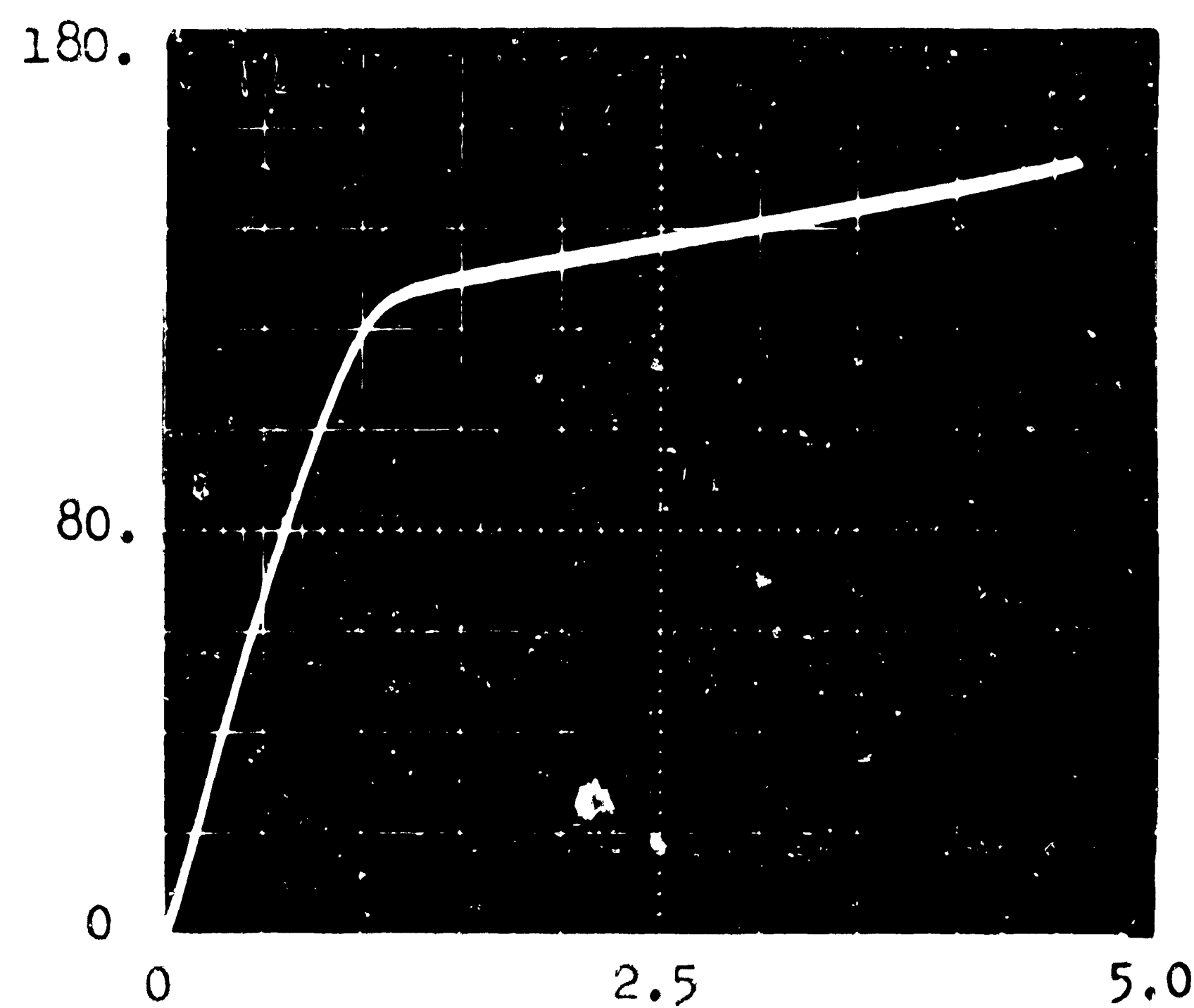
Output current into pin 12
5.0 ma/div.



$V_{cc} = 5.0$
"0" on Pin 1
No load

0.5 v/div.
Output voltage on Pin 12

Output current into pin 12
20. ma/div.



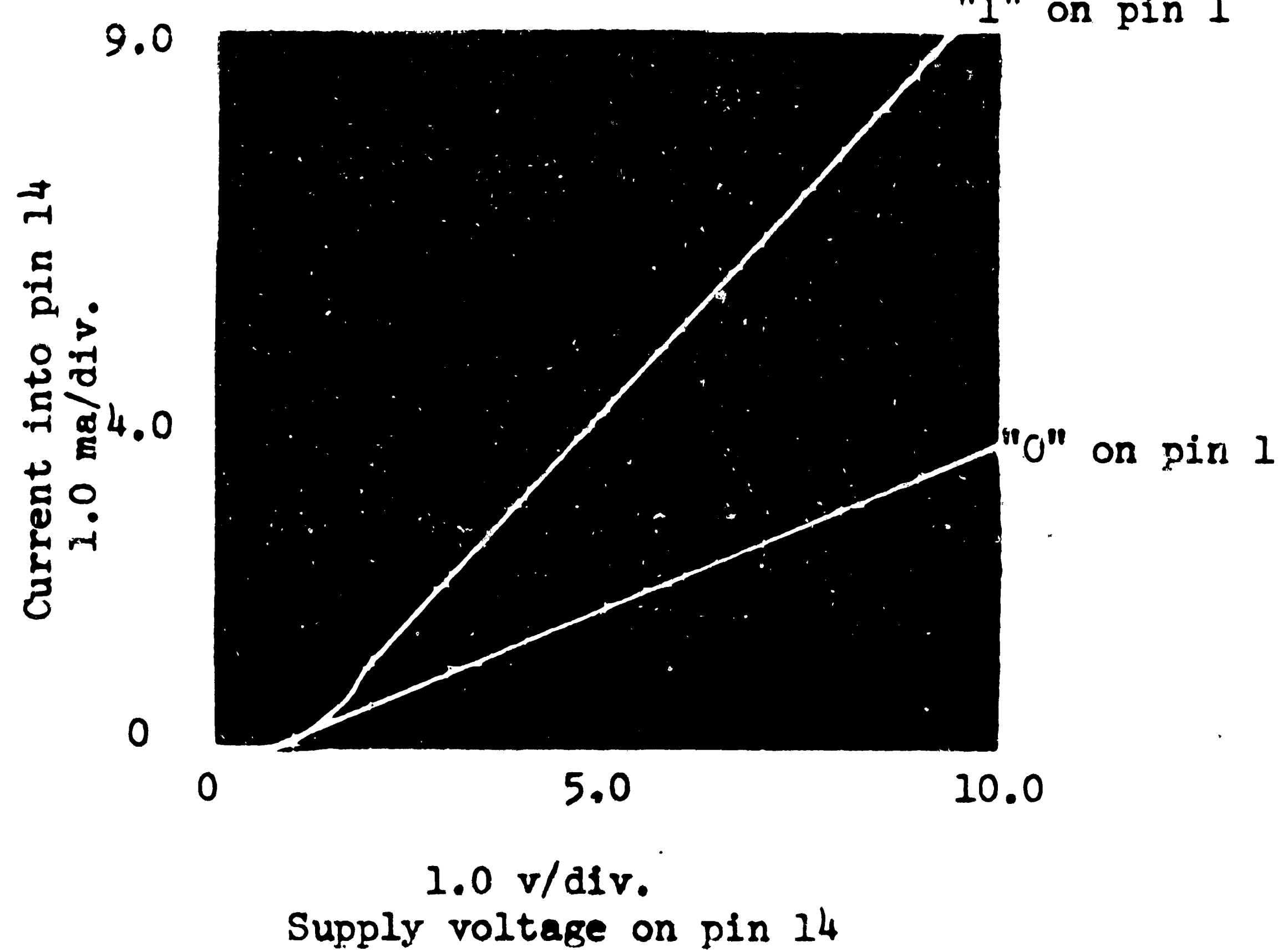
$V_{cc} = 5.0$
"1" on Pin 1
No load

OUTPUT CHARACTERISTICS
TTL 365G8

V_{cc} to load = 5.0

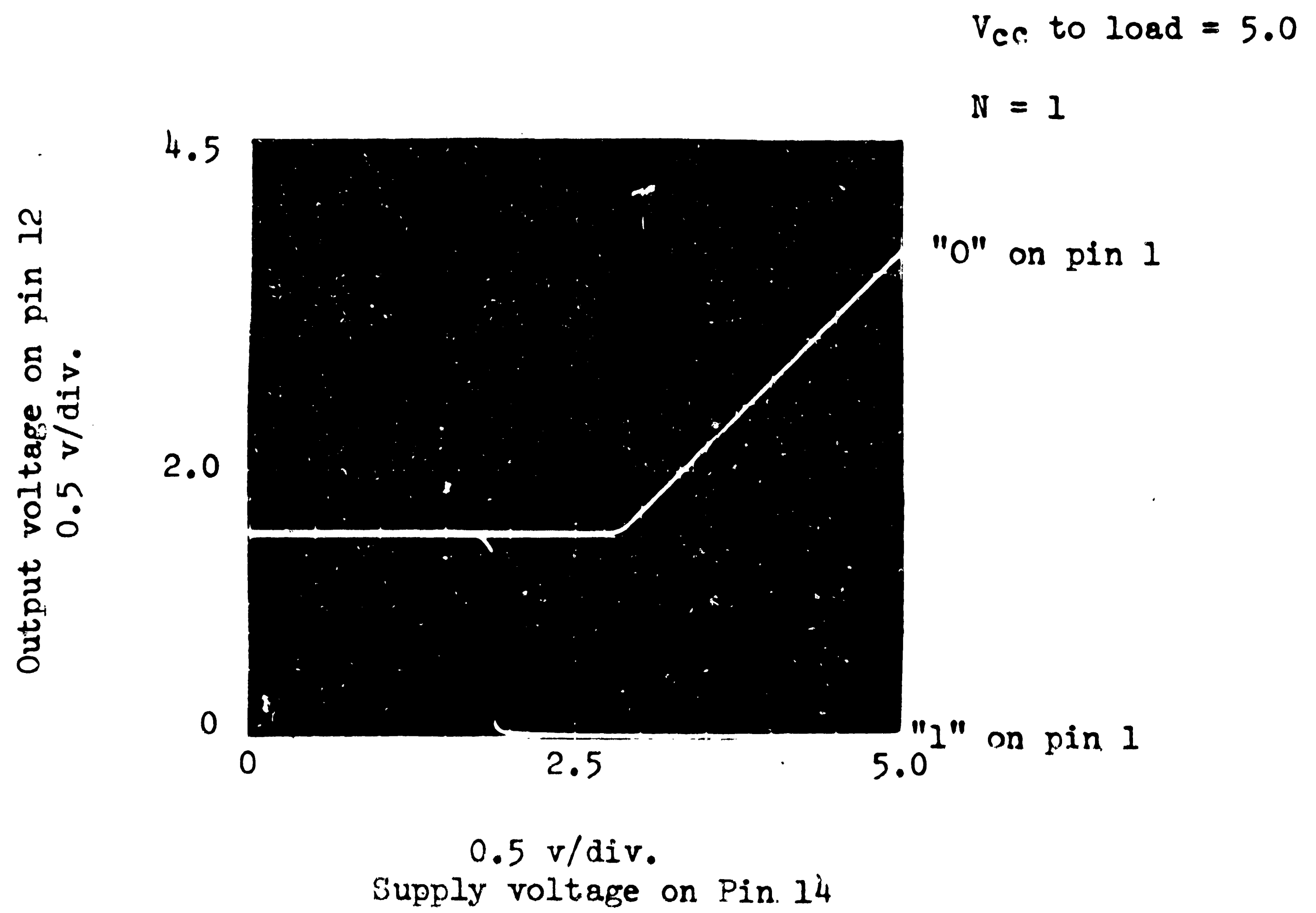
N = 1

"1" on pin 1

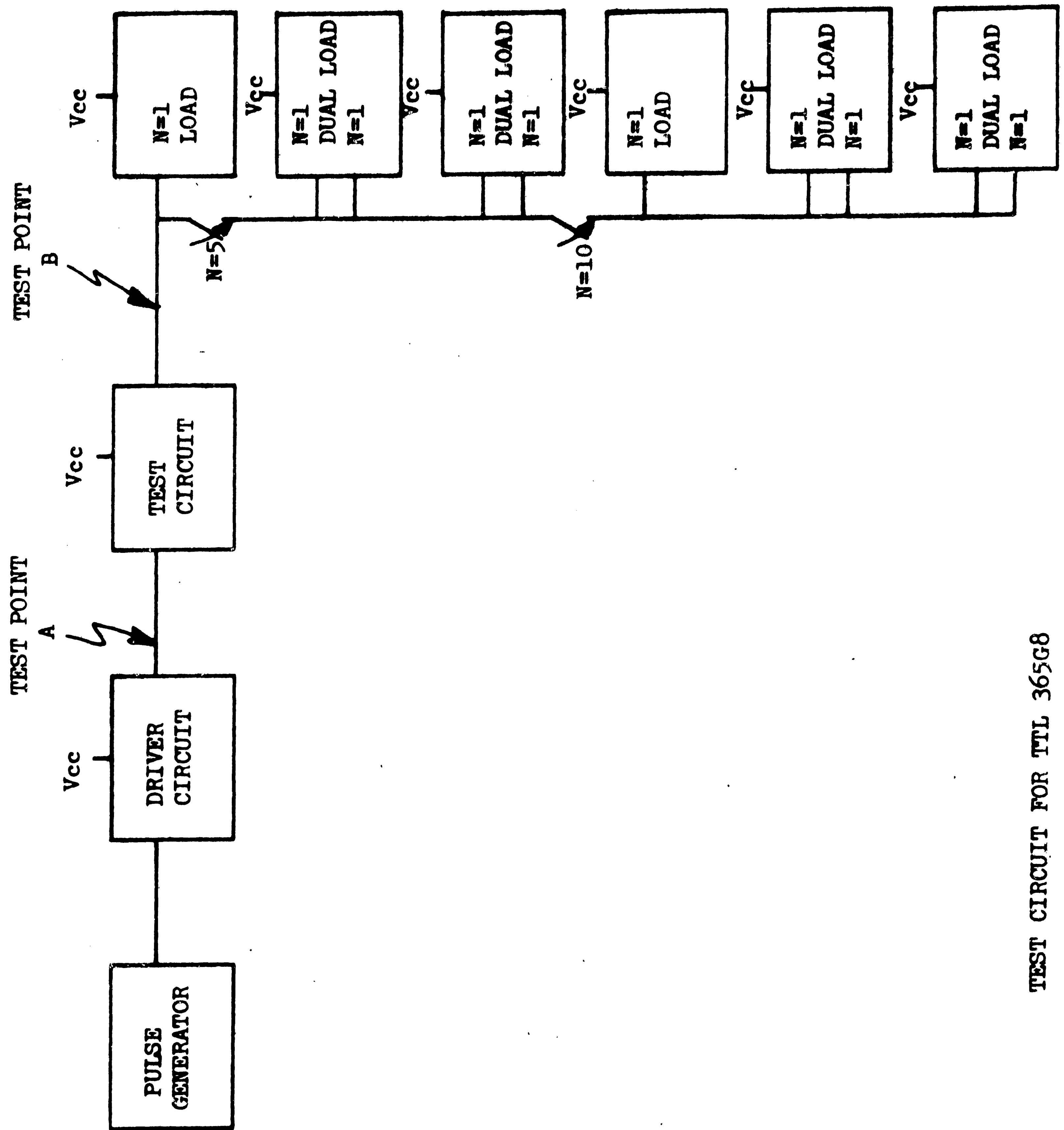


POWER DISSIPATION
TTL 365G8

3.2.166



OUTPUT VOLTAGE versus SUPPLY VOLTAGE
TTL 365G8

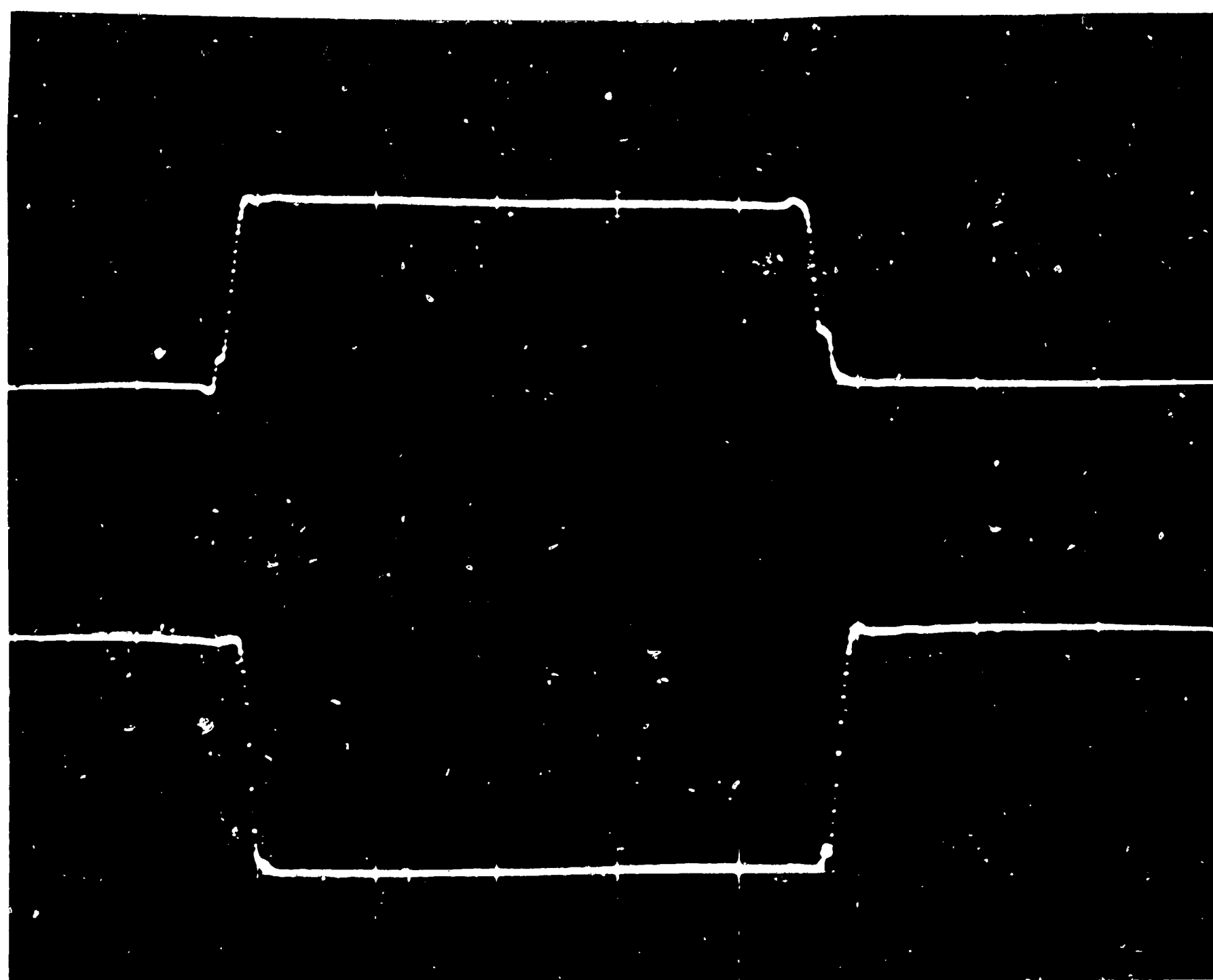


TEST CIRCUIT FOR TTL 365G8

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +25°C Vcc +5.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>502.</u>	<u>506.</u>	<u>508.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>3.6</u>	<u>4.25</u>	<u>4.95</u>	<u>5.65</u>
T_r	<u>21.</u>	<u>14.</u>	<u>14.</u>	<u>15.</u>
T_f	<u>22.</u>	<u>12.</u>	<u>11.</u>	<u>11.</u>
T_d		<u>23.</u>	<u>21.</u>	<u>19.</u>
T_s		<u>16.</u>	<u>19.</u>	<u>20.</u>
T_{pd}		<u>17.</u>	<u>17.</u>	<u>17.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type TTL No. 36508 Temp. -40°C Vcc +5.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>489.</u>	<u>494.</u>	<u>498.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>3.85</u>	<u>3.65</u>	<u>4.60</u>	<u>5.425</u>
T _r	<u>13.</u>	<u>14.</u>	<u>15.</u>	<u>16.</u>
T _f	<u>22.</u>	<u>15.</u>	<u>14.</u>	<u>13.</u>
T _d		<u>16.</u>	<u>19.</u>	<u>18.</u>
T _s		<u>10.</u>	<u>12.</u>	<u>12.8</u>
T _{pd}		<u>18.</u>	<u>17.</u>	<u>17.</u>

Type TTL No. 36508 Temp. -55°C Vcc 5.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>486.</u>	<u>491.</u>	<u>495</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>3.735</u>	<u>3.75</u>	<u>4.35</u>	<u>5.25</u>
T _r	<u>12.</u>	<u>13.</u>	<u>15.</u>	<u>16.</u>
T _f	<u>22.</u>	<u>15.</u>	<u>15.</u>	<u>13.</u>
T _d		<u>22.</u>	<u>19.</u>	<u>18.</u>
T _s		<u>11.</u>	<u>11.</u>	<u>12.</u>
T _{pd}		<u>18.</u>	<u>17.</u>	<u>17.</u>

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +85°C Vcc +5.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>511.</u>	<u>516.</u>	<u>520.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>4.0</u>	<u>4.30</u>	<u>4.90</u>	<u>5.50</u>
T _r	<u>31.</u>	<u>18.</u>	<u>20.</u>	<u>22.</u>
T _f	<u>23.</u>	<u>11.</u>	<u>11.0</u>	<u>12.</u>
T _d		<u>29.</u>	<u>28.</u>	<u>26.</u>
T _s		<u>22.</u>	<u>23.</u>	<u>25.</u>
T _{pd}		<u>19.</u>	<u>20.</u>	<u>20.</u>

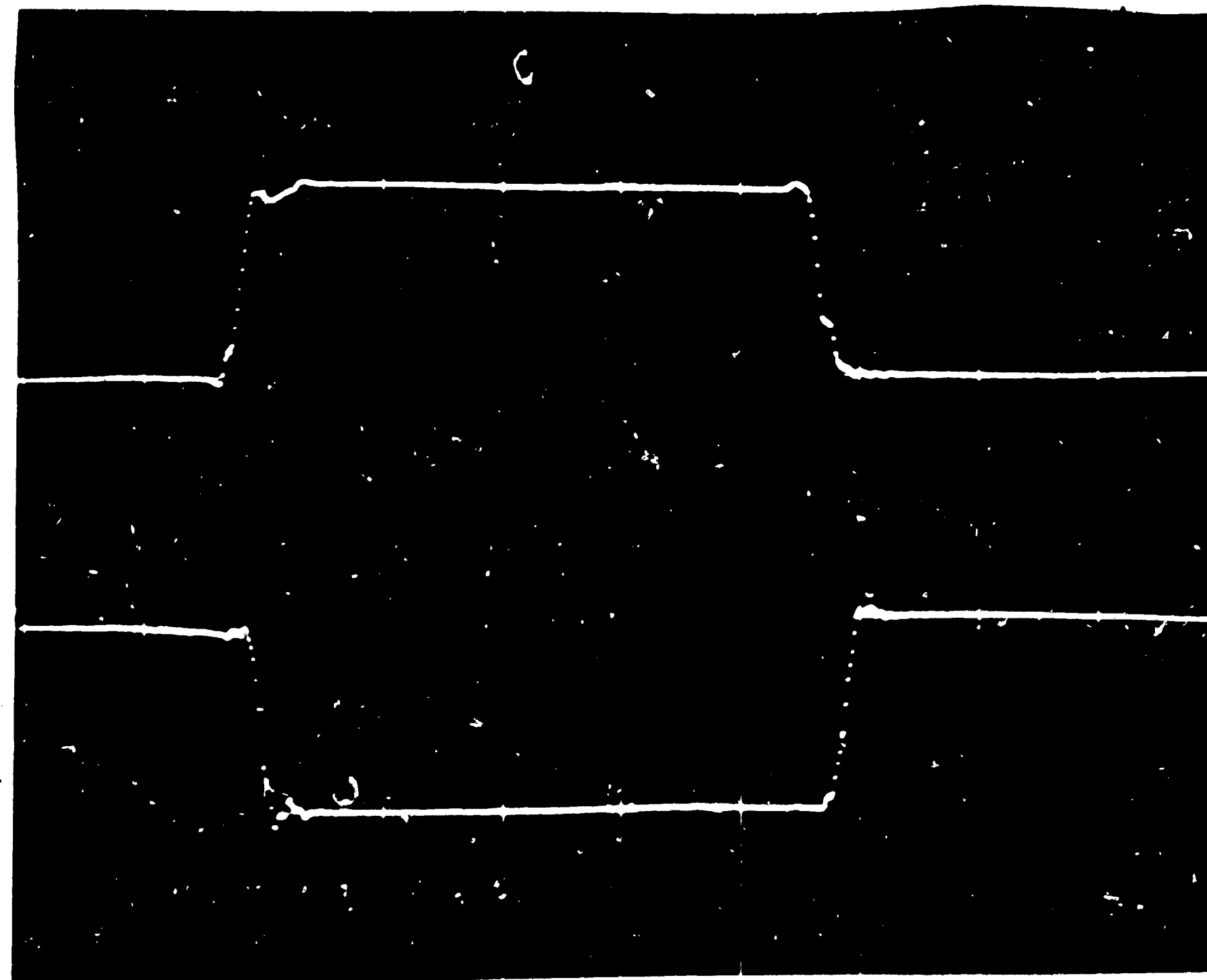
Type TTL No. 365G8 Temp. +125°C Vcc +5.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>532.</u>	<u>536.</u>	<u>540.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>4.15</u>	<u>4.25</u>	<u>4.85</u>	<u>5.40</u>
T _r	<u>41.</u>	<u>23.</u>	<u>23.</u>	<u>24.</u>
T _f	<u>26.</u>	<u>15.</u>	<u>16.</u>	<u>16.</u>
T _d		<u>32.</u>	<u>31.</u>	<u>30.</u>
T _s		<u>35.</u>	<u>39.</u>	<u>41.</u>
T _{pd}		<u>25.</u>	<u>26.</u>	<u>27.</u>

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +25°C Vcc +5.0 N = 5 ..

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>502.</u>	<u>505.</u>	<u>508.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>4.1</u>	<u>3.360</u>	<u>4.0</u>	<u>4.65</u>
T_r	<u>22.</u>	<u>15.</u>	<u>16.7</u>	<u>18.</u>
T_f	<u>22.</u>	<u>15.</u>	<u>16.</u>	<u>15.</u>
T_d		<u>23.</u>	<u>20.</u>	<u>20.</u>
T_s		<u>17.</u>	<u>18.</u>	<u>19.</u>
T_{pd}		<u>18.</u>	<u>18.</u>	<u>21.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. -40°C Vcc +5.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.0</u>
Pulse Width	<u>500.</u>	<u>488.</u>	<u>493.</u>	<u>498.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>3.90</u>	<u>3.075</u>	<u>3.70</u>	<u>4.50</u>
T _r	<u>14.</u>	<u>15.</u>	<u>16.</u>	<u>17.</u>
T _f	<u>23.</u>	<u>18.</u>	<u>18.</u>	<u>17.</u>
T _d		<u>24.</u>	<u>20.</u>	<u>19.</u>
T _s		<u>12.</u>	<u>13.</u>	<u>14.</u>
T _{pd}		<u>20.</u>	<u>17.</u>	<u>19.</u>

Type TTL No. 365G8 Temp. -55°C Vcc +5.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>484.</u>	<u>489.</u>	<u>492.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>3.775</u>	<u>2.95</u>	<u>3.65</u>	<u>4.35</u>
T _r	<u>12.</u>	<u>14.</u>	<u>16.</u>	<u>17.</u>
T _f	<u>24.</u>	<u>18.</u>	<u>19.</u>	<u>18.</u>
T _d		<u>25.</u>	<u>21.</u>	<u>19.</u>
T _s		<u>11.</u>	<u>12.</u>	<u>13.</u>
T _{pd}		<u>20.</u>	<u>20.</u>	<u>19.</u>

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +85°C Vcc +5.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>510.</u>	<u>516.</u>	<u>520.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>4.22</u>	<u>3.5</u>	<u>4.15</u>	<u>4.85</u>
T _r	<u>31.</u>	<u>20.</u>	<u>23.</u>	<u>27.</u>
T _f	<u>24.</u>	<u>16.5</u>	<u>16.</u>	<u>15.</u>
T _d		<u>29.</u>	<u>27.</u>	<u>27.</u>
T _s		<u>21.</u>	<u>23.</u>	<u>24.</u>
T _{pd}		<u>20.</u>	<u>20</u>	<u>22.</u>

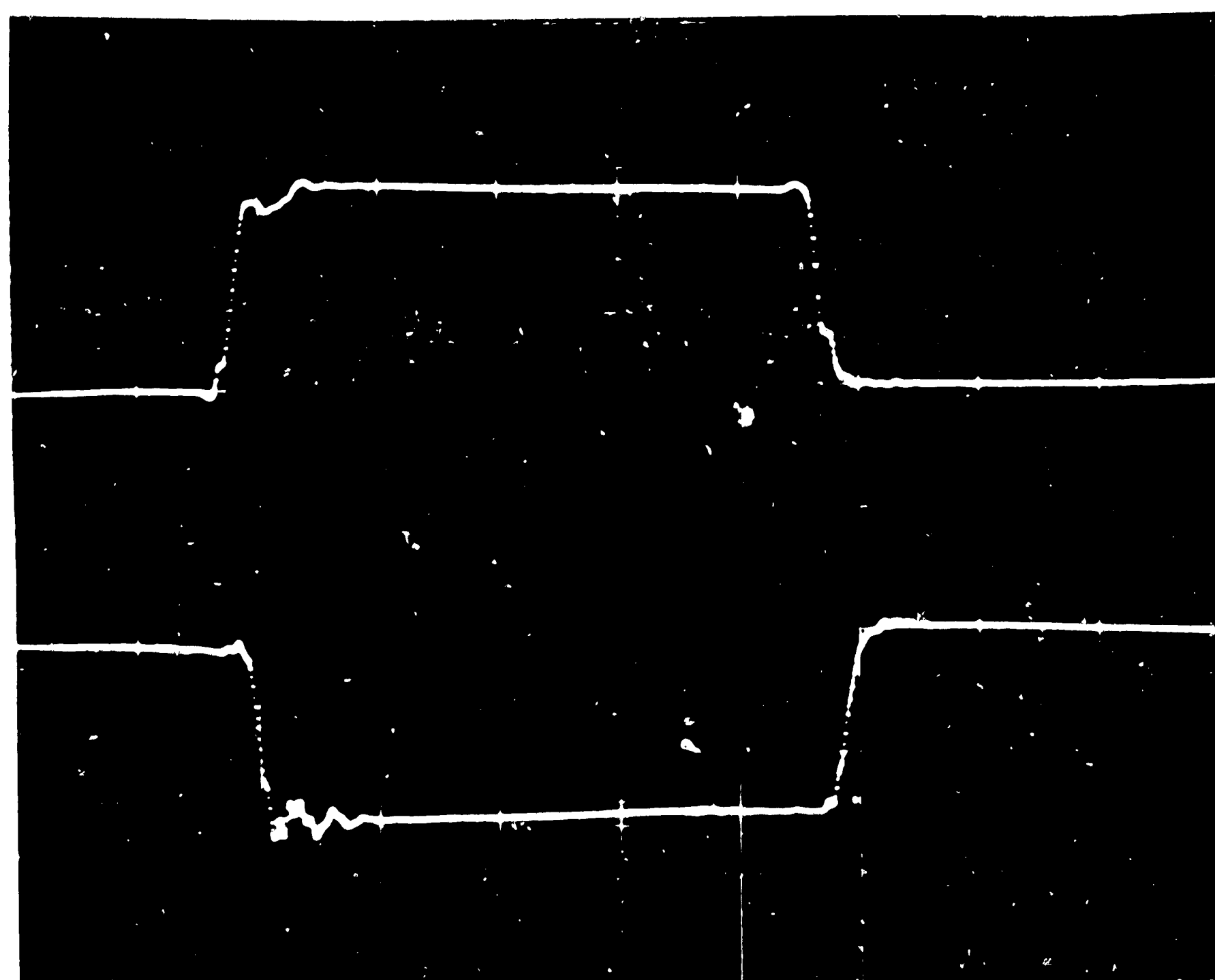
Type TTL No. 365G8 Temp. +125°C Vcc 5.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>529.</u>	<u>535.</u>	<u>538.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>4.25</u>	<u>3.670</u>	<u>4.275</u>	<u>4.85</u>
T _r	<u>41.</u>	<u>28.</u>	<u>25.</u>	<u>26.</u>
T _f	<u>26.</u>	<u>18.</u>	<u>18.</u>	<u>18.</u>
T _d		<u>32.</u>	<u>31.</u>	<u>30.</u>
T _s		<u>32.</u>	<u>39.</u>	<u>41.</u>
T _{pd}		<u>26.</u>	<u>28.</u>	<u>29.</u>

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +25°C Vcc +5.0 N = 10 ..

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>501.</u>	<u>505.</u>	<u>508.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC.</u>	<u>IMC</u>
Pulse Amplitude	<u>4.3</u>	<u>3.16</u>	<u>3.75</u>	<u>4.35</u>
T _r	<u>22.</u>	<u>19.</u>	<u>20.</u>	<u>23.</u>
T _f	<u>23.</u>	<u>18.3</u>	<u>17.</u>	<u>18.</u>
T _d		<u>25.</u>	<u>23.</u>	<u>20.</u>
T _s		<u>16.</u>	<u>19.</u>	<u>20.</u>
T _{pd}		<u>20.</u>	<u>20.</u>	<u>21.</u>



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. -40°C Vcc +5.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>486.</u>	<u>494.</u>	<u>496.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>4.15</u>	<u>2.85</u>	<u>3.51</u>	<u>4.15</u>
T _r	<u>16.</u>	<u>19.</u>	<u>22.</u>	<u>20.</u>
T _f	<u>24.</u>	<u>19.</u>	<u>21.</u>	<u>21.</u>
T _d		<u>26.</u>	<u>19.</u>	<u>18.</u>
T _s		<u>12.</u>	<u>12.</u>	<u>15.</u>
T _{pd}		<u>22.</u>	<u>22.</u>	<u>21.</u>

Type TTL No. 365G8 Temp. -55°C Vcc +5.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>483.</u>	<u>492.</u>	<u>495.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>4.05</u>	<u>2.80</u>	<u>3.35</u>	<u>3.95</u>
T _r	<u>14.</u>	<u>20.</u>	<u>20.</u>	<u>23.</u>
T _f	<u>24.</u>	<u>21.</u>	<u>21.</u>	<u>20.</u>
T _d		<u>18.</u>	<u>18.</u>	<u>17.</u>
T _s		<u>8.</u>	<u>9.</u>	<u>10.</u>
T _{pd}		<u>17.</u>	<u>19.</u>	<u>20.</u>

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +85°C Vcc +5.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>511.</u>	<u>515.</u>	<u>519.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>4.4</u>	<u>3.325</u>	<u>3.85</u>	<u>4.45</u>
T _r	<u>34.</u>	<u>34.</u>	<u>32.</u>	<u>33.</u>
T _f	<u>24.</u>	<u>18.</u>	<u>18.</u>	<u>17.5</u>
T _d		<u>30.</u>	<u>29.</u>	<u>28.</u>
T _s		<u>26.</u>	<u>23.</u>	<u>23.</u>
T _{pd}		<u>23.</u>	<u>23.</u>	<u>24.</u>

Type TTL No. 365G8 Temp. +125°C Vcc +5.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR		
		Vcc <u>4.5</u>	Vcc <u>5.0</u>	Vcc <u>5.5</u>
Pulse Width	<u>500.</u>	<u>529.</u>	<u>536.</u>	<u>541.</u>
Repetition Rate	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>	<u>IMC</u>
Pulse Amplitude	<u>4.45</u>	<u>3.5</u>	<u>4.05</u>	<u>4.625</u>
T _r	<u>44.</u>	<u>35.</u>	<u>34.</u>	<u>35.</u>
T _f	<u>26.</u>	<u>19.</u>	<u>19.</u>	<u>18.</u>
T _d		<u>34.</u>	<u>33.</u>	<u>32.</u>
T _s		<u>31.</u>	<u>39.</u>	<u>42.</u>
T _{pd}		<u>27.</u>	<u>31.</u>	<u>32.</u>

NOTES # 9.3.3

EVALUATION OF SYLVANIA DIGITAL INTEGRATED CIRCUITS

	Page
SNG-4B: Dual NAND/NOR Gate	3.3.3
SNG-5B: NAND/OR Gate	3.3.24
SNG-6B: High Fan-In NAND/NOR Gate	3.3.38
SNG-20: NAND/OR Gate (Voter Gate)	3.3.52
SFF-2B: Set-Reset Trigger Flip-Flop	3.3.61
SFF-3A: Set-Reset Trigger Flip-Flop	3.3.69

It is seldom that microcircuits are used individually, therefore testing was performed in a manner approaching system simulation.

1. Since the V_{CC} in a system is usually supplied by a single source, the question arises as to the amount of change in the circuit parameters which will be caused by a variation of V_{CC} . The three voltages selected for this test were 4.5, 5.0 and 5.5 since the manufacturer centered around 5.0 volts.

2. Loading was accomplished by means of dual SNG-4B units. In the standard test set-up for gates, the following two load conditions were imposed upon the test circuit: A load of "1" circuit and a load of "20" circuits. For this report, a load will be defined as that load presented by one input per each single gate circuit connected to the output of the circuit. Dual elements were used as loads, therefore each circuit represented a load of "2".

3. The input signals to the test circuit were produced by a driver circuit which was a dual element SNG-4B. This dual driver circuit which was driven from a pulse generator enabled a positive input to the test circuit since a negative going pulse was not available on the generator used.

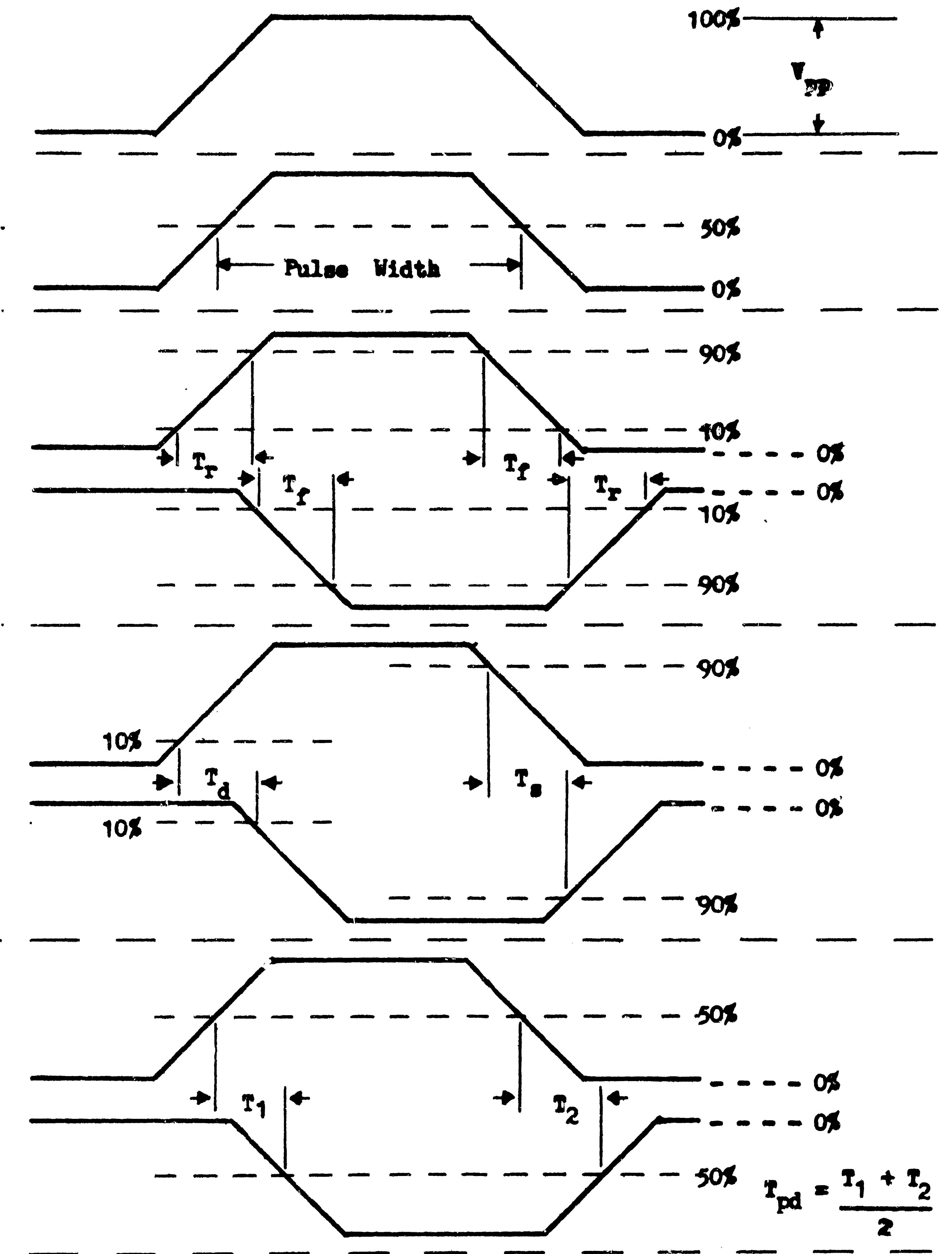
The driver circuit provided isolation between the generator and the test circuit as well as providing test circuit input variances as the V_{CC} to the entire system was varied.

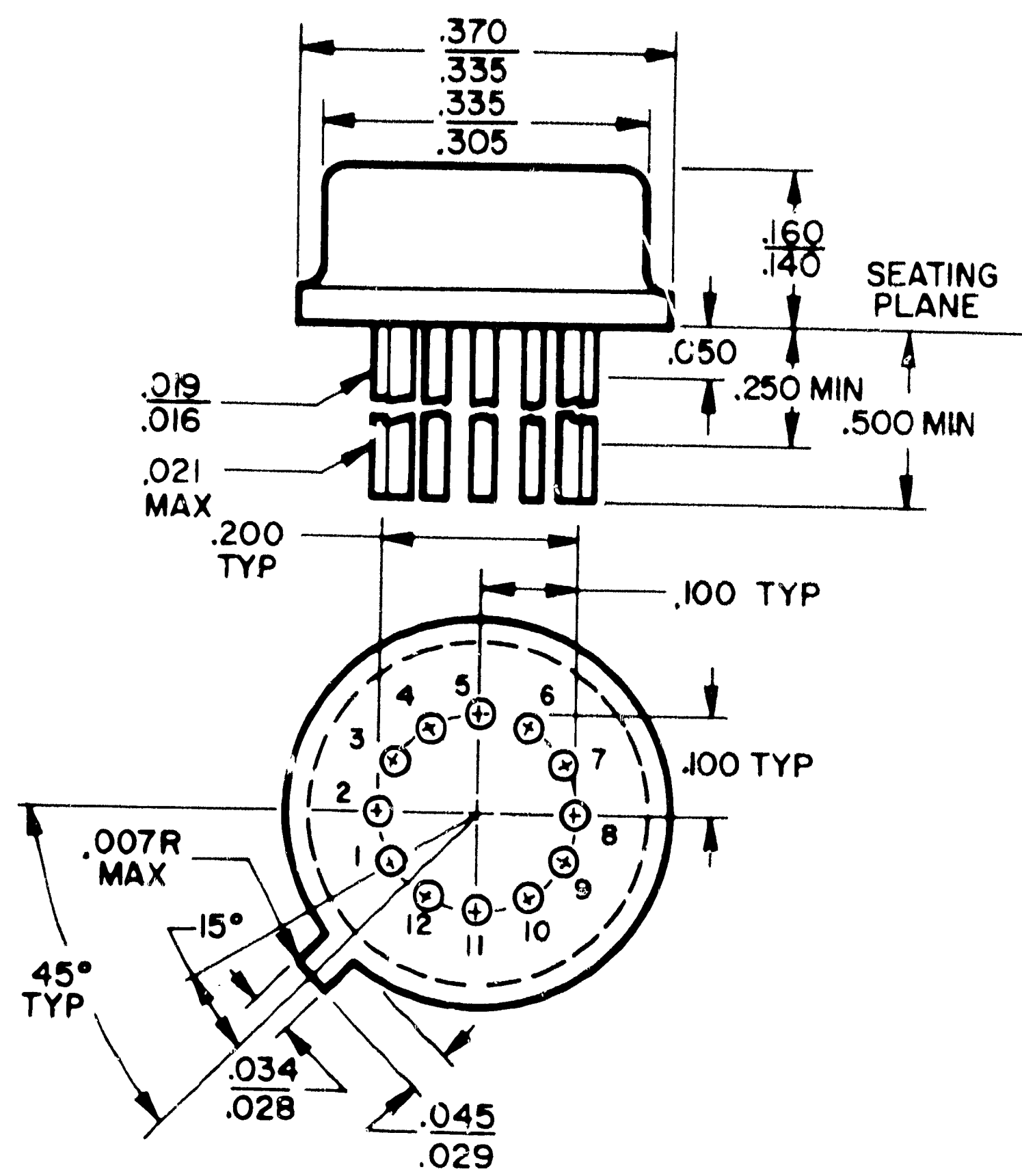
In the case of the flip-flops, which require alternate inputs, one signal was passed through a dual element for a positive input while the other was passed through a single element to produce a negative input. This provided alternate inputs with a time lag between them which was approximately equal to the propagation delay of "1" circuit. Measurements were made from the input traversing the most circuits before entering the test circuits. This ensured that the other input was already present and any effect on circuit operation was due to the input being monitored.

4. All of the elements of the system were subjected to the same temperature conditions. The temperatures used were: -55°C , -40°C , $+25^{\circ}\text{C}$, $+85^{\circ}\text{C}$, and $+125^{\circ}\text{C}$.

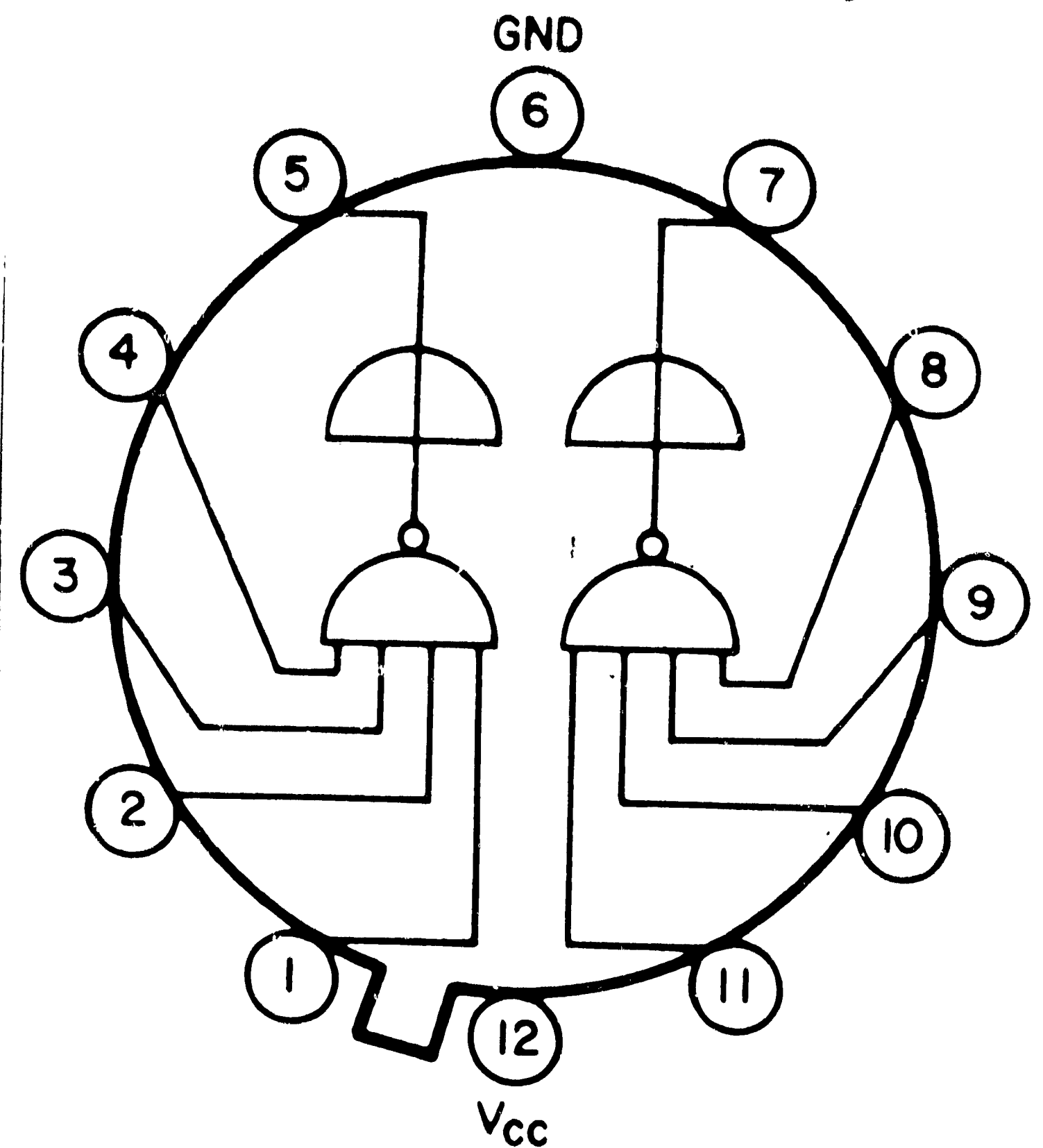
5. The test fixture used was constructed from a glass epoxy sheet on which the wiring was kept at a minimum. A 1.0 mfd capacitor was used between V_{CC} and ground on the surface of the board. Signals were taken from B.N.C. connectors mounted as close to the circuit loads as possible. The probes used for measuring circuit parameters were of the cathode follower type and are approximately 10 megohms shunted by 2.6 pfd to ground.

6. The measurements made in this section are illustrated on the following page.





12 LEAD TO-5



BOTTOM VIEW

SNG-4B

FOR SNG-4A INPUTS 9-A AND 3-G ARE NOT PRESENT

GENERAL GUIDE TO TESTING PROCEDURE USED FOR GATE CIRCUITS:

I. D.C. characteristics

II. Dynamic characteristics

A. Generator driven

1. Variation of frequency

2. Variation of V_{cc}

(1.) Variation of temperature

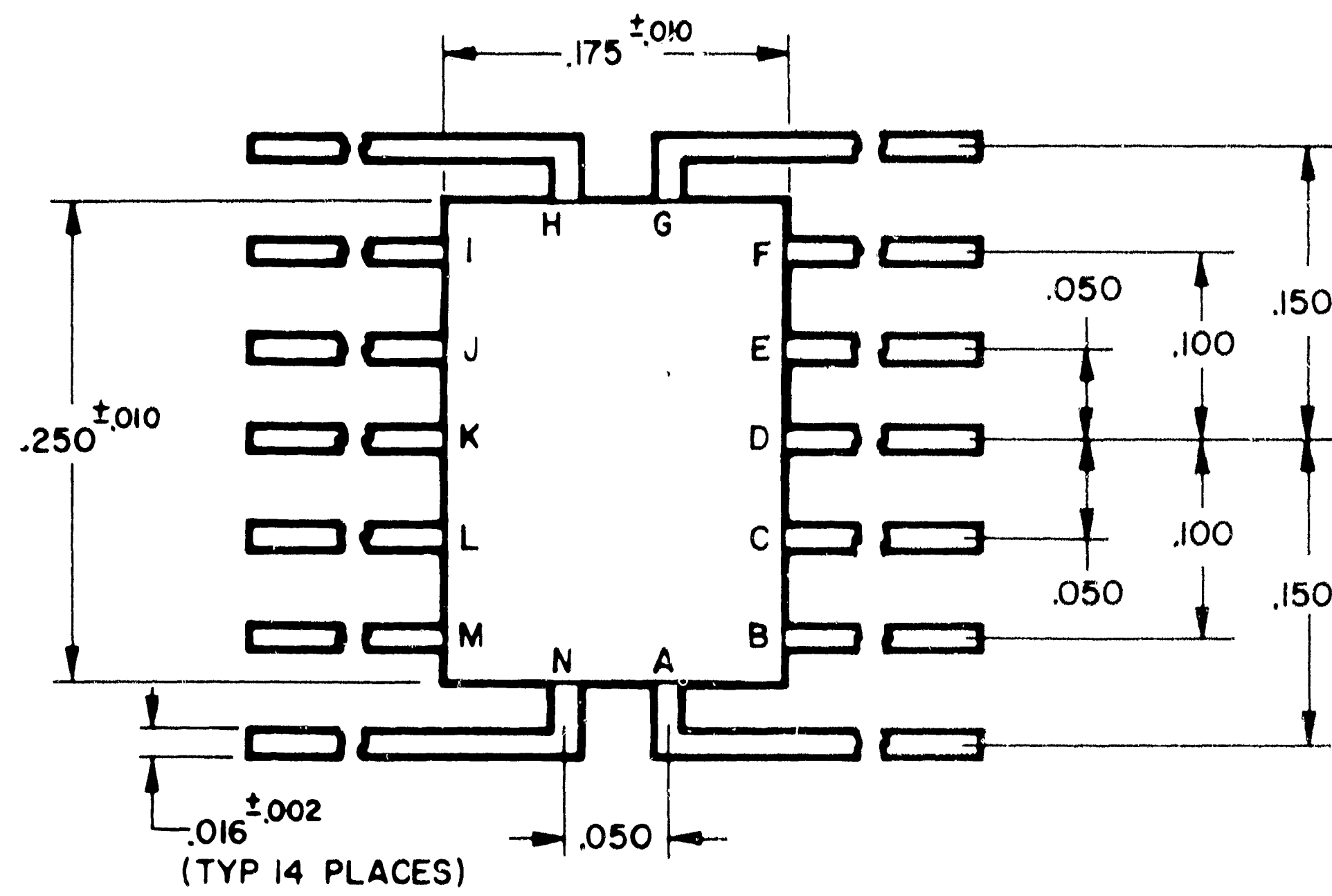
2. Variation of loads

B. Ring counter driven

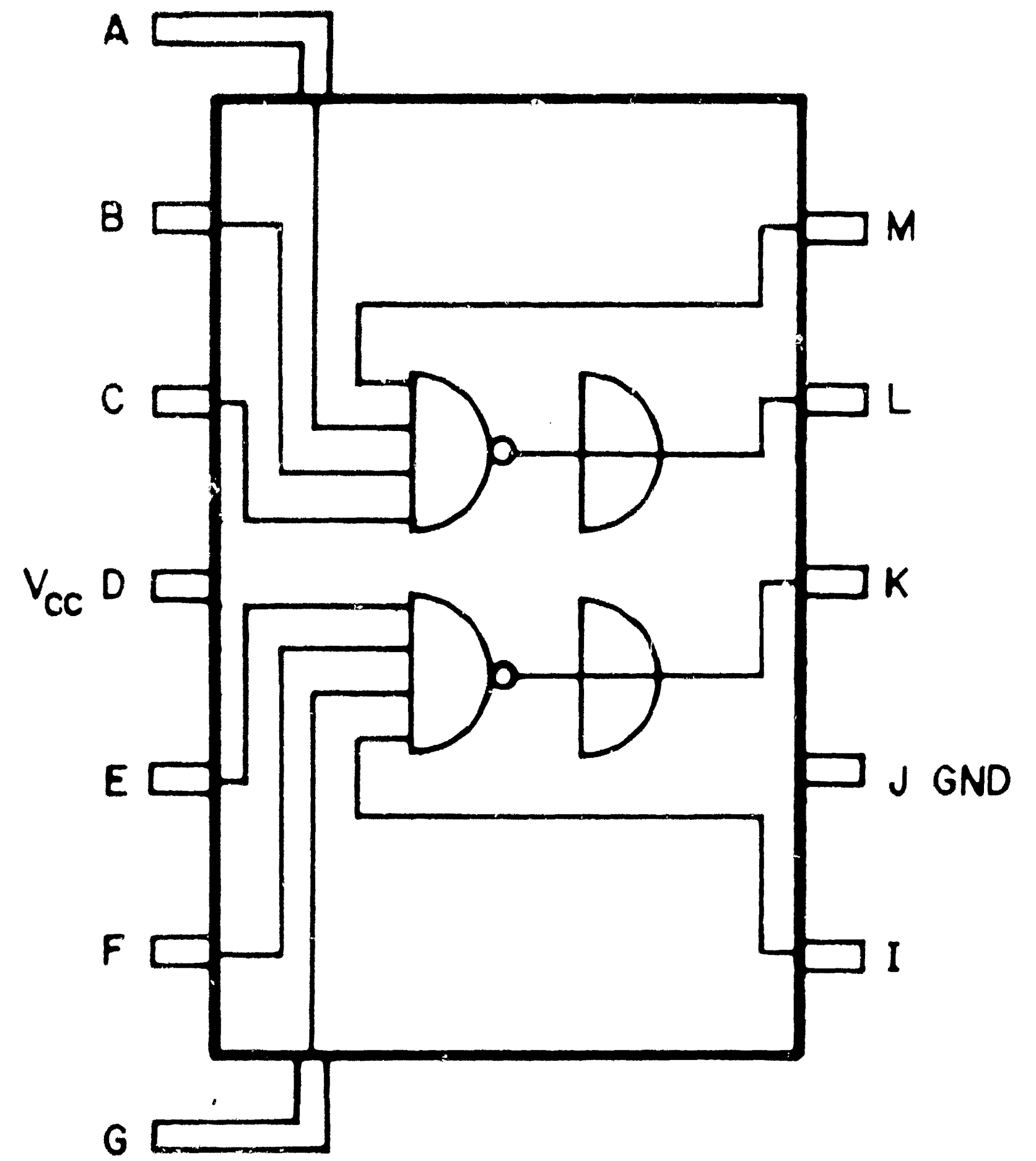
1. Variation of elements

a. Variation of V_{cc}

(1.) Variation of temperature



14-LEAD FLAT PACK



TOP VIEW

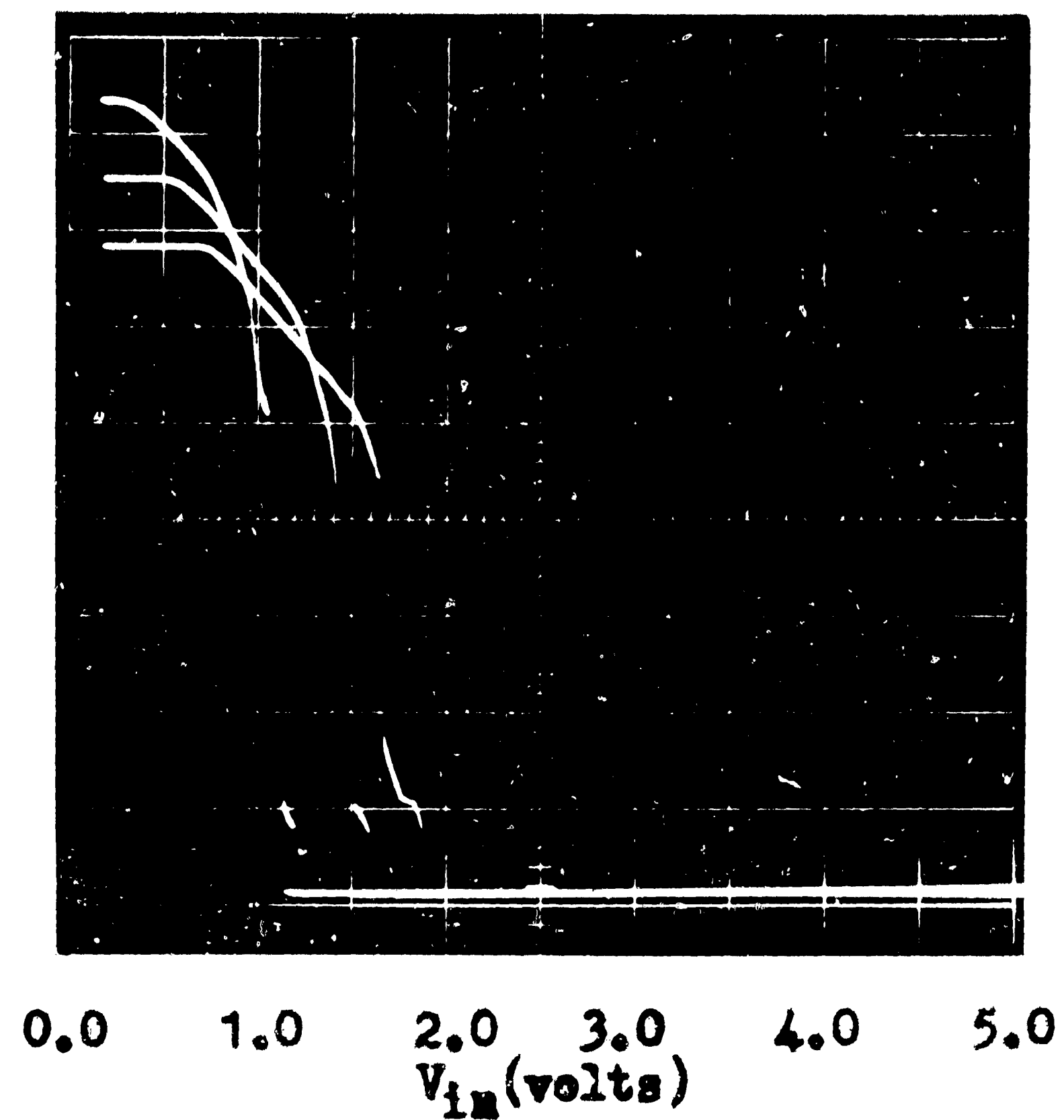
V_{in} vs. V_{out}

1.) $V_{CC} = 5 \text{ v.}$

+125°C
+25°C
-55°C

$V_{out}(\text{volts})$

4.0
3.0
2.0
1.0
0.0

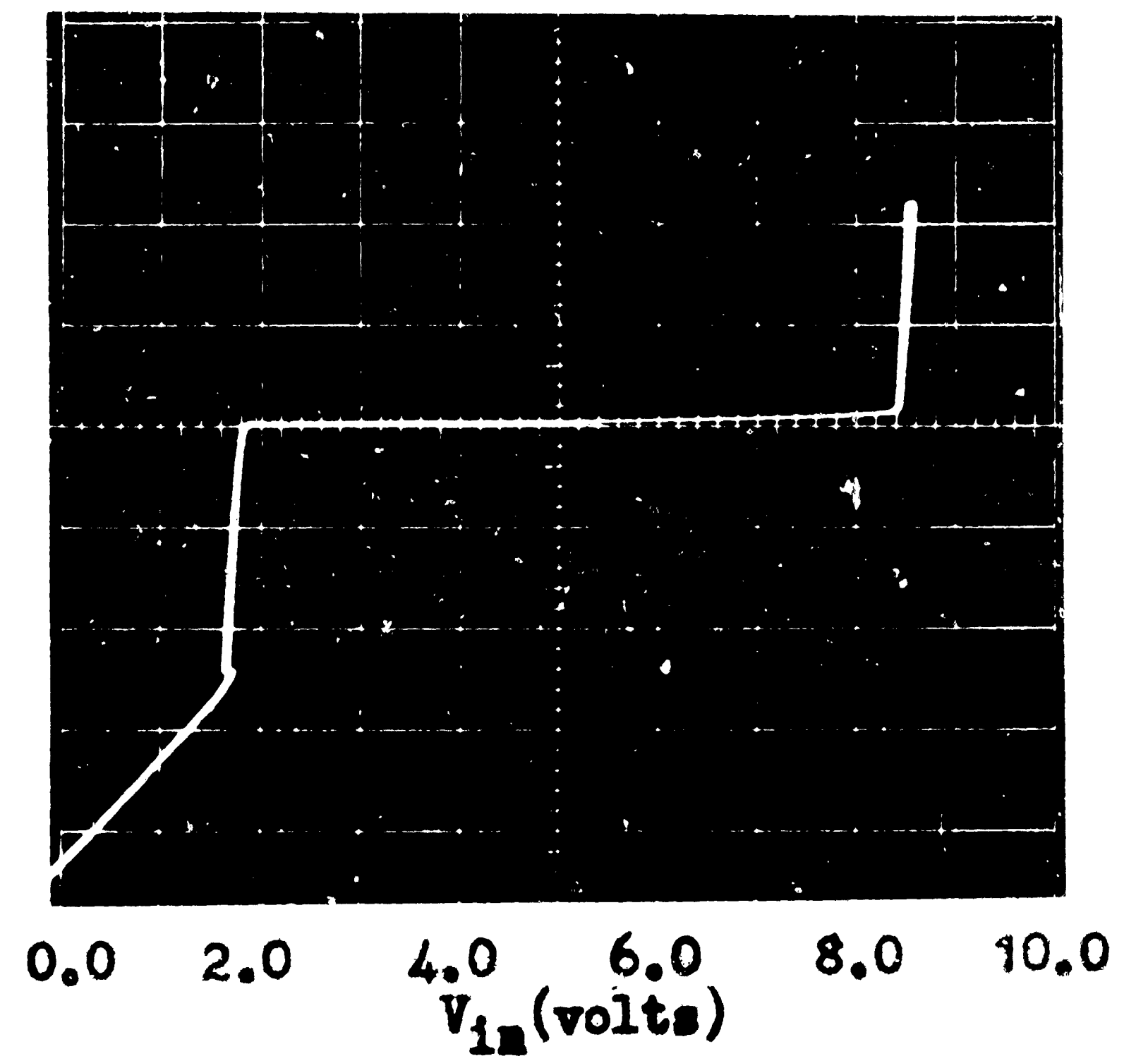


V_{in} vs. I_{in}

1.) $V_{CC} = 5 \text{ v.}$

2.) $T = 25^\circ\text{C}$

0.8
0.4
0.0
-0.4
-0.8
 $I_{in}(\text{Ma.})$



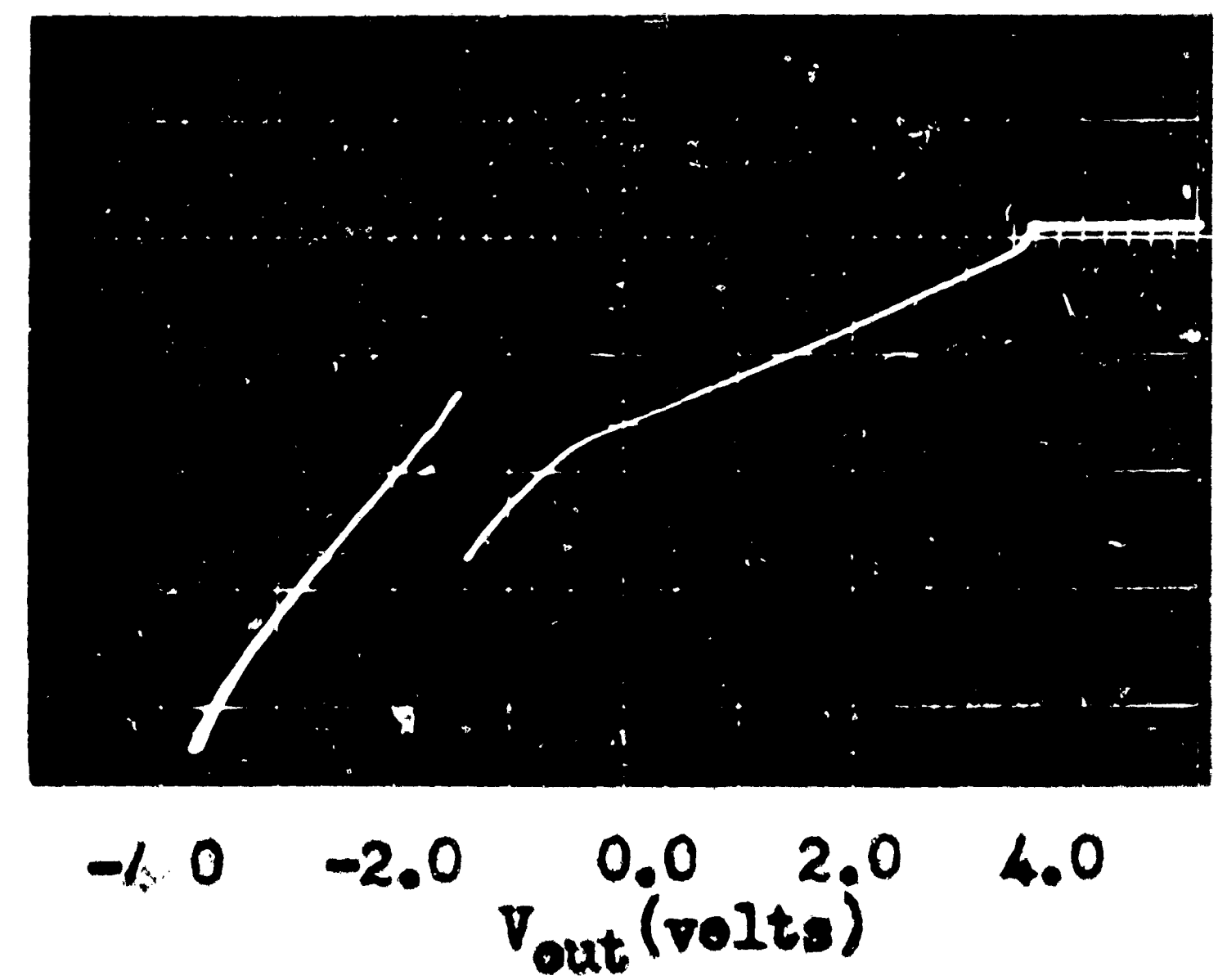
V_{out} vs. I_{out}

1.) $V_{CC} = 5 \text{ v.}$

2.) $T = 25^\circ\text{C}$

3.) Pin #3 & #10 @
ground.

40.0
0.0
-40.0
-80.0
 $I_{out}(\text{Ma.})$



V_{out} vs. I_{out}

1.) $T = 25^{\circ}\text{C}$

2.) $V_{cc} = 5.0 \text{ v.}$

3.) All inputs high

$I_{out} (\text{Ma.})$

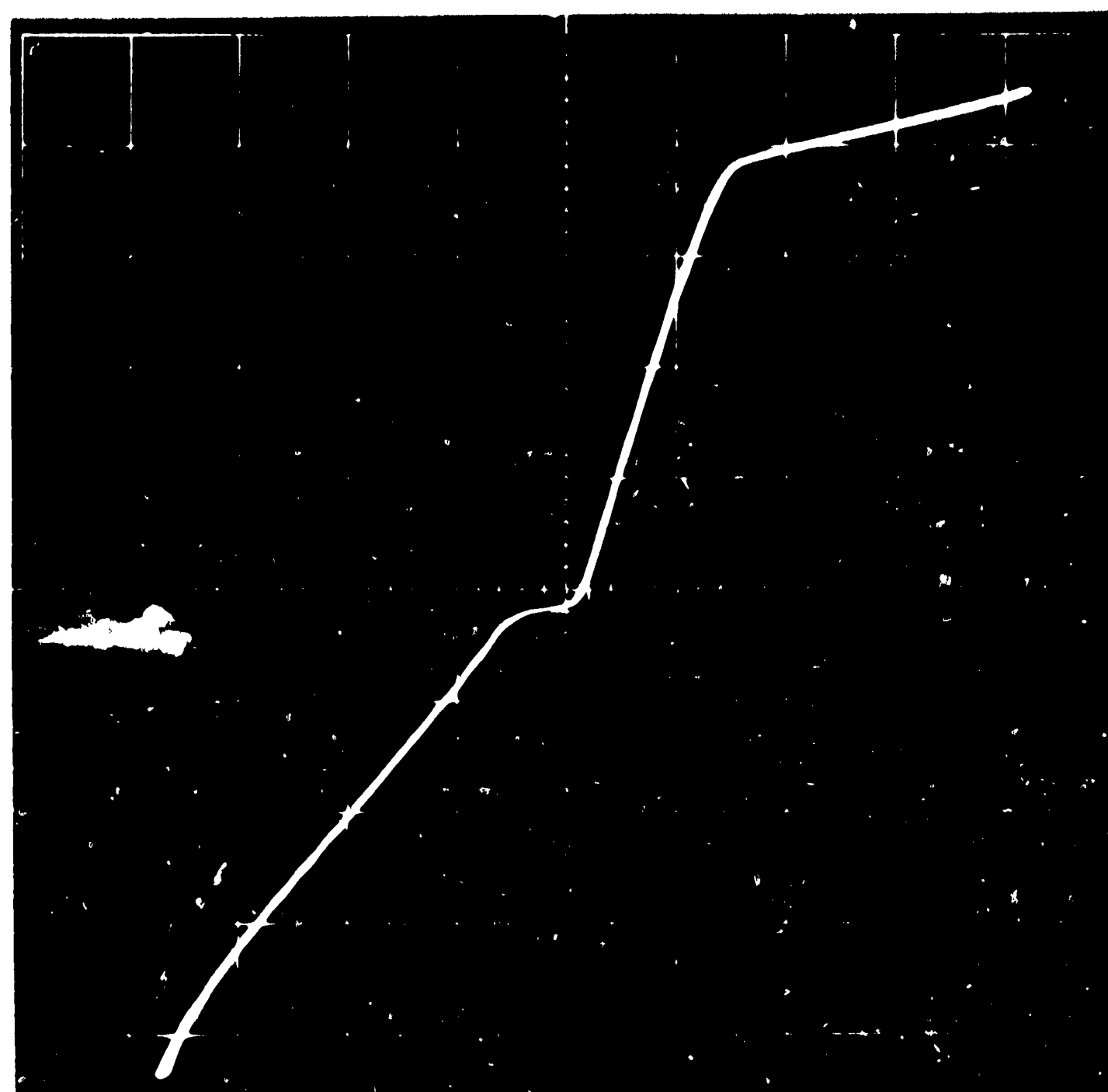
80.0

40.0

0.0

-40.0

-80.0



-4 -2 0.0 +2 +4
 $V_{out} (\text{volts})$

V_{cc} vs. I_{cc}

1.) $T = 25^{\circ}\text{C}$

2.) 50% duty cycle obtained with high output pin #7 connected to pin #3, with pin #10 grounded.

$I_{cc} (\text{Ma.})$

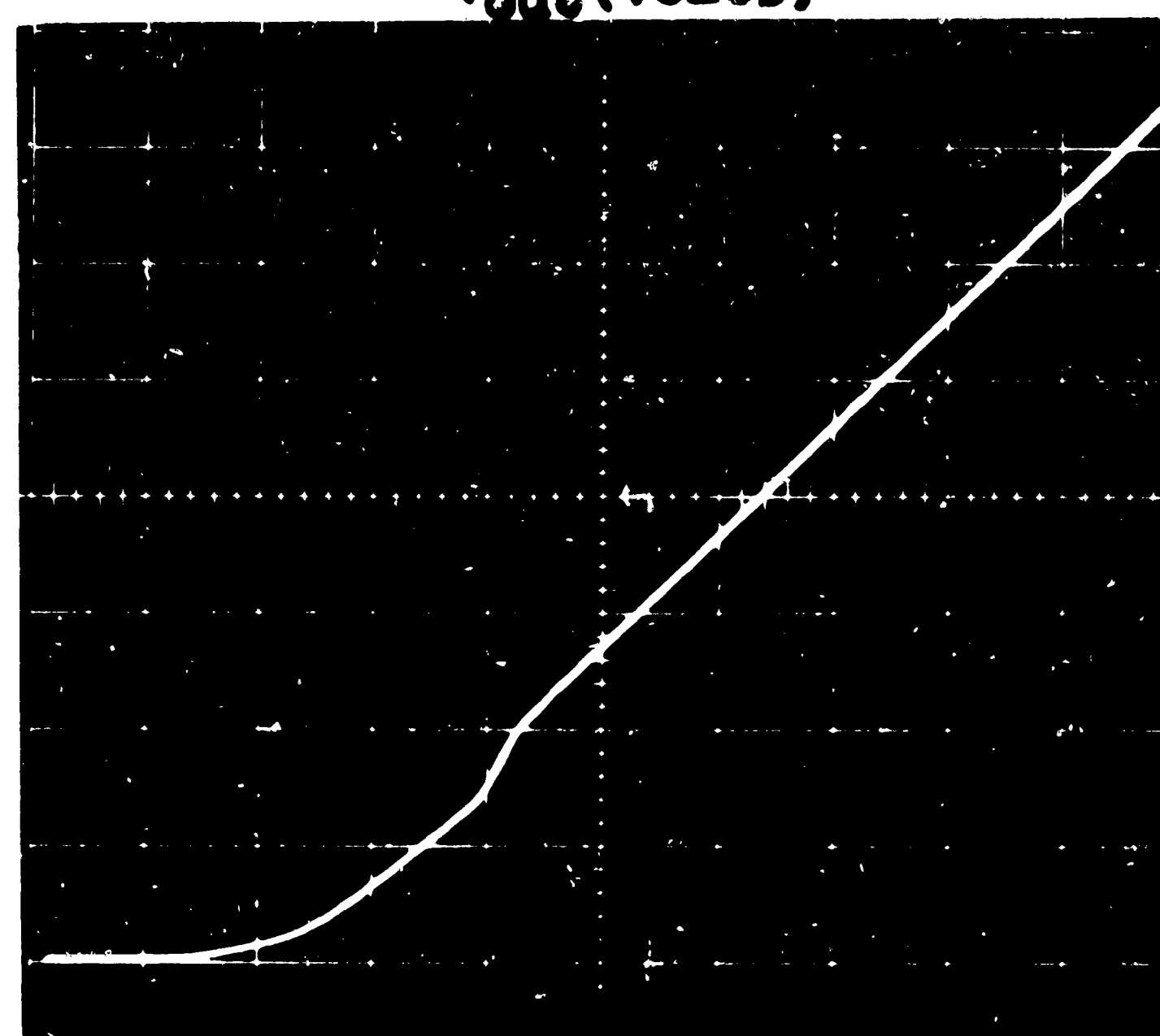
4.0

3.0

2.0

1.0

0.0



0 1 2 3 4 5
 $V_{cc} (\text{volts})$

V_{cc} vs. V_{out}

1.) $T = 25^{\circ}\text{C}$

2.) Top trace = "0" in

3.) Bottom trace = "1" in

$V_{out} (\text{volts})$

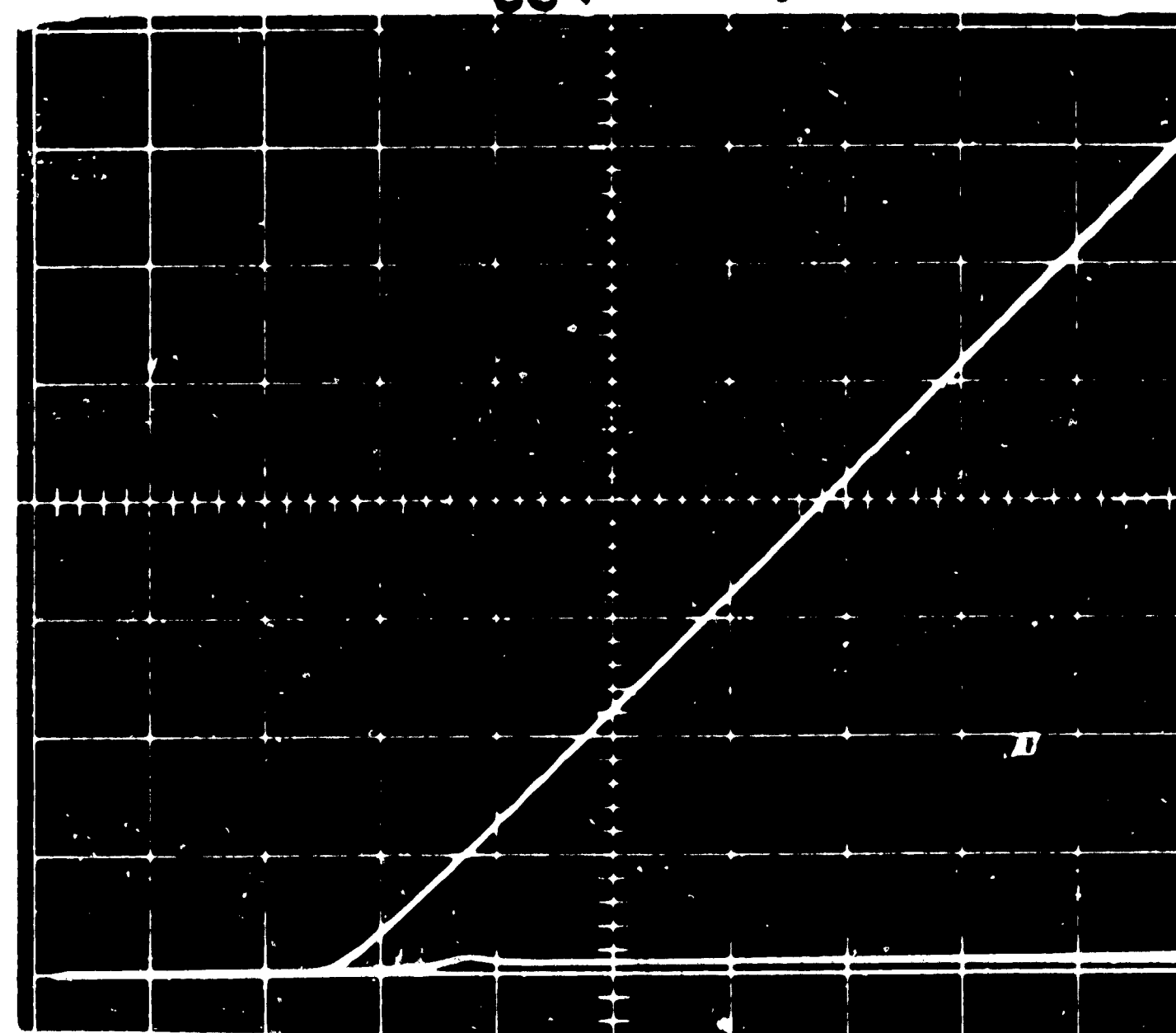
4.0

3.0

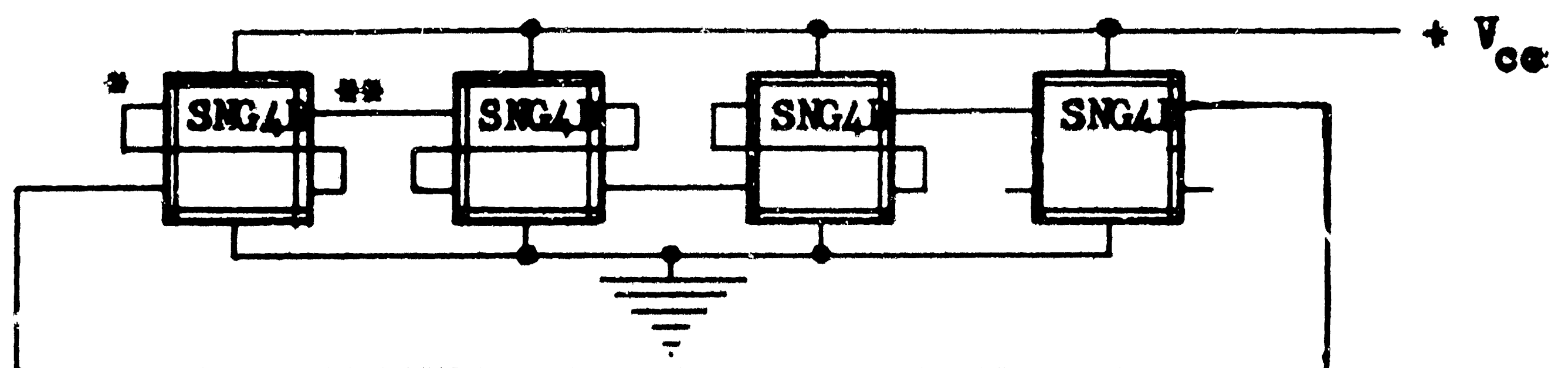
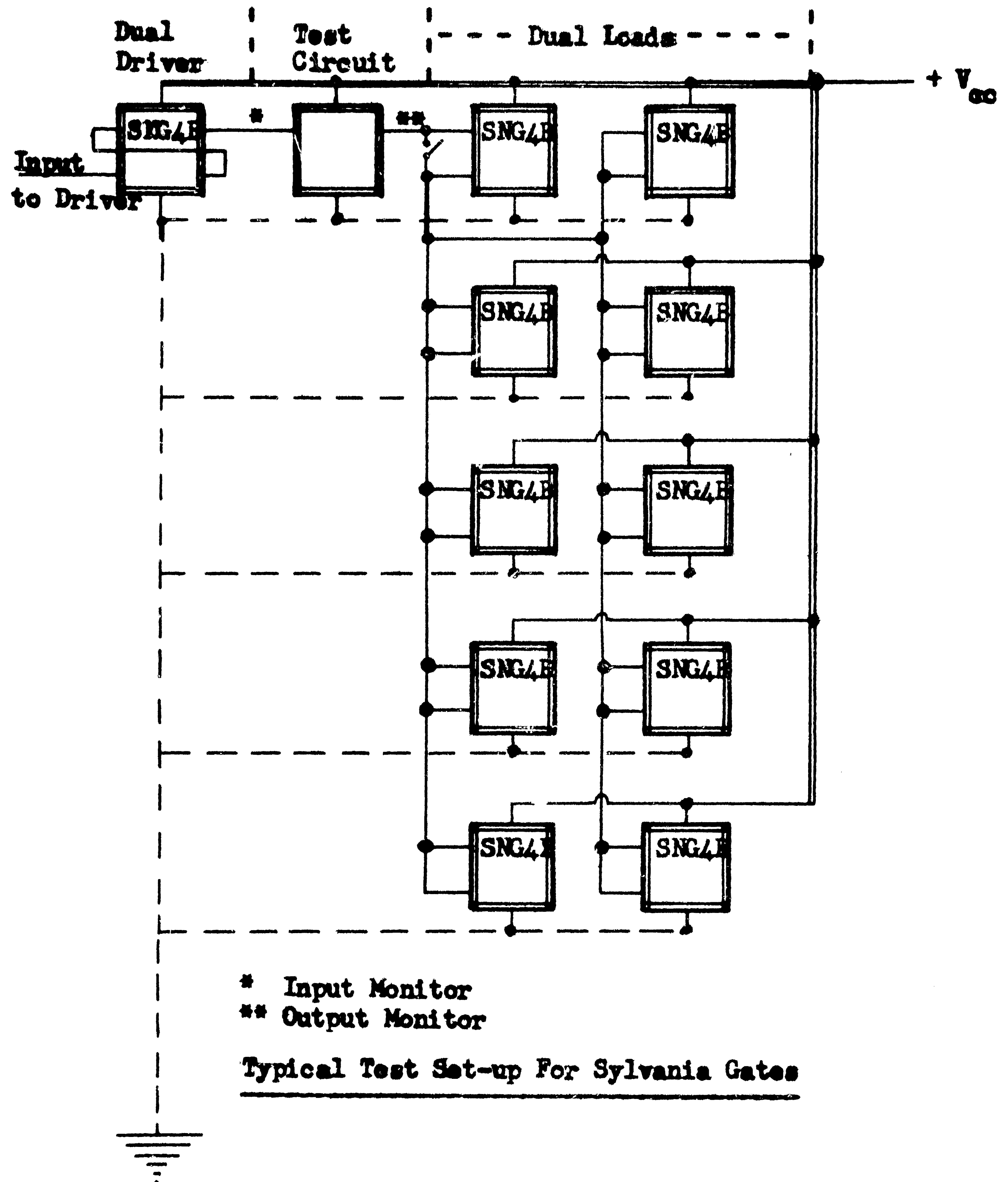
2.0

1.0

0.0



0 1 2 3 4 5
 $V_{cc} (\text{volts})$



SNG 4B 7 Element Ring Counter

Circuit SW1 4B		Supply Voltage 4.5				Frequency = 1 mc.				Fan-in 1			
Temperature:		-55°C				-40°C				+25°C			
Load		1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V _{pp})		2.7	2.6	2.9	2.3	2.8	2.7	3.0	2.4	2.9	2.9	3.4	2.6
Pulse Width (ns.)		200	183	200	179	200	190	200	185	200	195	200	196
T _r (ns.)		6.0	4.5	7.0	11	6.0	5.0	8.0	11	9.0	8.0	12	15
T _f (ns.)		8.5	10	9.0	31	8.0	10	8.0	27	6.0	6.0	5.4	14
T _d (ns.)			17		19		15		16		11		12
T _g (ns.)			8.0		8.0		8.0		8.0		7.0		7.0
T _{pd} (ns.)			13		19		12		16		9.5		12
Temperature:		+85°C				+125°C							
Load		1	1	20	20	1	1	20	20				
Test Circuit		input	output	input	output	input	output	input	output				
Pulse Amplitude (V _{pp})		3.2	3.1	3.7	2.8	3.2	3.3	3.7	2.8				
Pulse Width (ns.)		200	201	200	205	200	206	200	211				
T _r (ns.)		13	12	19	21	18	16	41	27				
T _f (ns.)		5.0	5.0	5.0	13	5.5	5.5	6.0	12				
T _d (ns.)			11		11		10		10				
T _g (ns.)			7.5		8.5		8.0		9.0				
T _{pd} (ns.)			8.5		12		8.5		11				

Circuit <u>92A 4B</u> Supply Voltage <u>5.0</u> Frequency = <u>1 MC.</u> Fan-in <u>1</u>															
Temperature:		-55°C						-40°C				+25°C			
Load		1	1	20	20	1	1	20	20	1	1	20	20		
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output		
Pulse Amplitude (V _{pp})		3.2	3.1	3.5	2.8	3.3	3.1	3.6	2.8	3.4	3.3	3.9	3.0		
Pulse Width (ns.)		200	192	200	192	200	193	200	194	200	198	200	200		
T _r (ns.)		6.6	5.5	9.0	12	6.8	5.5	10	12	9.8	8.5	14	16		
T _f (ns.)		6.8	8.5	7.0	26	6.0	7.5	6.0	19	5.0	5.5	5.0	13		
T _d (ns.)			12.7		14		11.8		13		9.8		11		
T _s (ns.)			7.4		8.0		7.0		7.0		7.0		7.0		
T _{pd} (ns.)			10		15		9.0		13		8.0		11		
Temperature:		+85°C						+125°C							
Load		1	1	20	20	1	1	20	20	1	1	20	20		
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output		
Pulse Amplitude (V _{pp})		3.7	3.7	4.2	3.3	3.7	3.8	4.3	3.5						
Pulse Width (ns.)		200	205	200	207	200	209	200	215						
T _r (ns.)		15	13	38	23	20	17	39	27						
T _f (ns.)		5.0	5.0	5.0	11	5.0	5.0	5.0	8.5						
T _d (ns.)			9.4		9.5		9.0		9.0						
T _s (ns.)			7.5		8.5		8.0		10						
T _{pd} (ns.)			8.0		11		8.0		11						

Circuit SMG 4B		Supply Voltage 5.5				Frequency = 1 mc.				Fan-in 1			
Temperature:		-55°C				-40°C				+25°C			
Load		1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})		3.7	3.5	4.1	3.2	3.7	3.6	4.2	3.3	3.9	3.8	4.5	3.5
Pulse Width (ns.)		200	196	200	196	200	196	200	197	200	199	200	204
T_r (ns.)		7.0	6.0	10	15	8.0	6.0	11	15	10	9.0	16	20
T_f (ns.)		6.0	7.0	5.0	18	5.0	6.0	5.0	15	4.5	5.0	5.0	12
T_d (ns.)			10		12		10		11		8.8		9.0
T_s (ns.)			7.0		7.0		7.0		7.0		6.5		7.0
T_{pd} (ns.)			9.5		13		8.5		13		7.0		10
Temperature:		+85°C				+125°C							
Load		1	1	20	20	1	1	20	20				
Test Circuit		input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})		4.1	4.1	4.9	3.8	4.2	4.2	4.8	3.9				
Pulse Width (ns.)		200	206	200	211	200	212	200	218				
T_r (ns.)		16	14	37	24	21	18	38	26				
T_f (ns.)		4.5	4.5	5.0	11	4.8	4.6	5.0	8.0				
T_d (ns.)			8.5		9.0		8.0		8.0				
T_s (ns.)			7.0		8.0		8.0		10				
T_{pd} (ns.)			7.5		11		11		11				

Circuit <u>SMU 4B</u>				Supply Voltage <u>5.0</u>				Frequency = <u>6 ms.</u>				Fan-in <u>1</u>				
Temperature:				-55°C				-40°C				+25°C				
Load	1	1	20	20	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.2	3.1	3.7	2.9	3.2	3.2	3.8	3.0	3.4	3.4	4.1	3.2	3.4	3.4	4.1	3.2
Pulse Width (ns.)	50	46	50	46	50	47	50	48	50	49	50	51	50	49	50	51
T_r (ns.)	6.5	6.0	10	14	7.0	6.0	11	15	10	9.0	35	18	9.0	9.0	35	18
T_f (ns.)	5.0	7.0	5.0	26	5.0	6.0	5.0	17	4.0	5.0	5.0	13	4.0	5.0	5.0	13
T_d (ns.)		10		11		9.0		10		8.0		9.0		8.0		9.0
T_s (ns.)		7.0		6.5		6.0		7.0		6.0		8.0		6.0		8.0
T_{pd} (ns.)		8.5		12		8.0		11		7.5		10		7.5		10
Temperature:				+85°C				+125°C								
Load	1	1	20	20	1	1	20	20	1	1	20	20				
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})	3.6	3.6	4.3	3.4	3.8	3.8	4.3	3.5								
Pulse Width (ns.)	50	55	50	59	50	60	50	66								
T_r (ns.)	15	13	38	23	20	17	39	27								
T_f (ns.)	4.0	5.0	5.0	13	4.5	5.0	5.0	12								
T_d (ns.)		8.0		9.0		8.0		8.0								
T_s (ns.)		7.0		8.0		8.0		9.0								
T_{pd} (ns.)		7.5		10		7.0		11								

SNG 4B $V_{cc}=5.0$ v. Frequency = 1 mc. Input Pulse Width = 200 nsec.

Load Ckts.	20	18	16	14	12	10	8	6	4	2
T_{pd}	11.0	10.6	10.6	10.6	10.5	10.1	10.0	9.5	9.5	9.2
T_r Output	16.8	15.2	14.7	14.2	13.5	12.7	12.0	11.0	10.5	10.2
T_f Output	12.5	12.0	11.5	11.0	10.4	9.8	9.0	8.5	7.4	6.5
Pulse Amp. (Input)	4.0	3.8	3.8	3.7	3.7	3.6	3.6	3.5	3.4	3.3
Pulse Amp. (Output)	2.98	3.02	3.06	3.06	3.08	3.12	3.20	3.22	3.24	3.26

Temperature = 25°C.

SNQ 4 B Ring Counter (7 elements)

Temperature °C	-55		-40		+25		+85		+125	
Frequency no.	7.4 ---		8.0 ---		9.0 ---		8.5 ---		8.1 ---	
V _{cc} volts	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5
Test Circuit	in	out	in	out	in	out	in	out	in	out
Pulse Amp. volts pp.	2.9	2.9	3.0	2.8	3.1	2.9	3.3	3.2	3.5	3.2
Pulse Width nsec.	71	66	65	61	57	56	57	61	58	67
T _r nsec.	6.0	4.4	6.6	4.3	9.4	6.3	14	10	18	13
T _f nsec.	8.5	6.3	7.6	5.5	5.7	4.3	5.4	4.0	5.4	4.0
T _d nsec.	—	11	—	10	—	8.3	—	7.7	—	7.6
T _s nsec.	—	8.6	—	8.3	—	7.7	—	8.4	—	9.0
T _{pd} nsec.	—	9.1	—	8.6	—	7.4	—	7.2	—	7.4

SNQ 4B Ring Counter (7 elements)

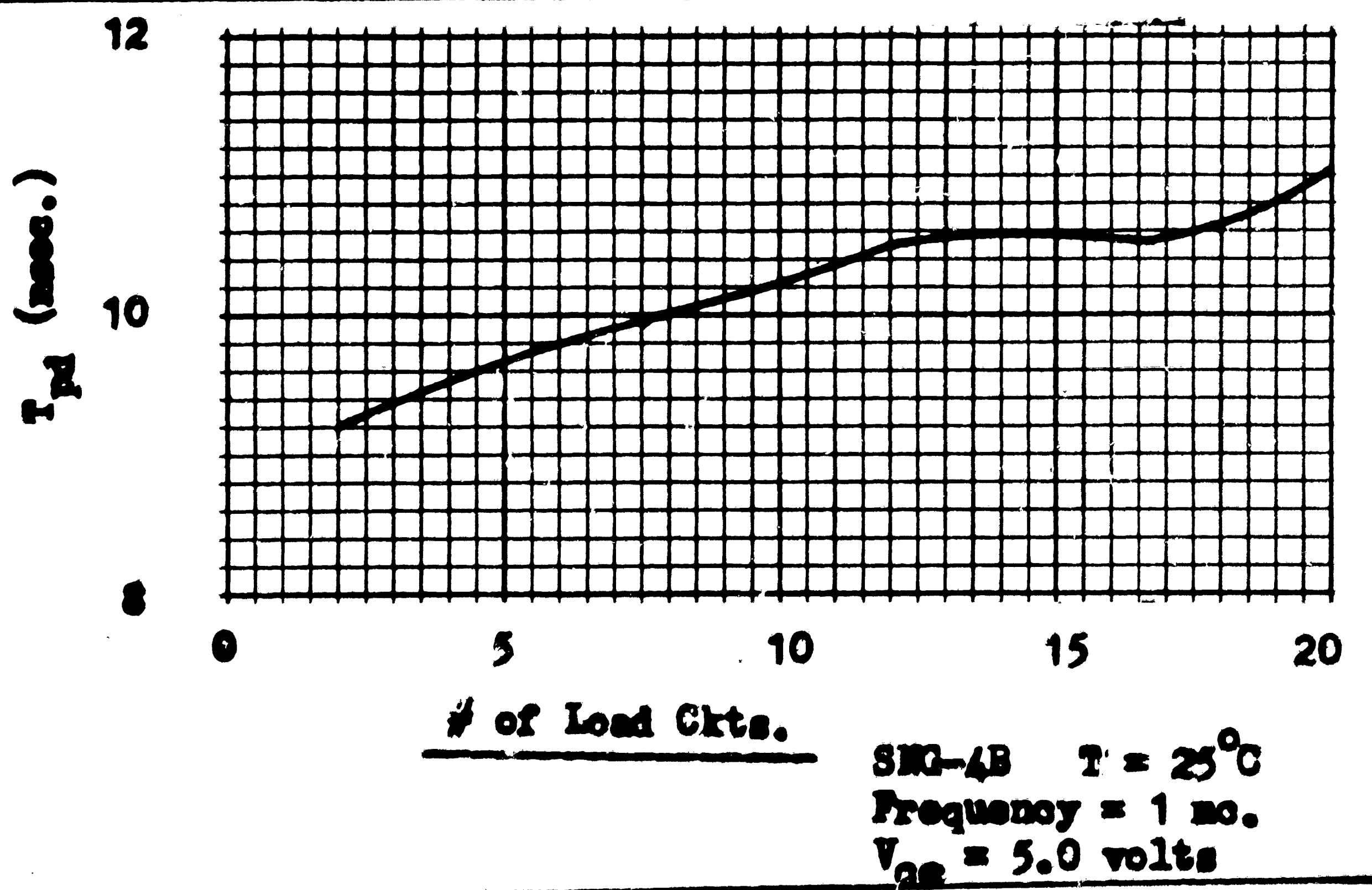
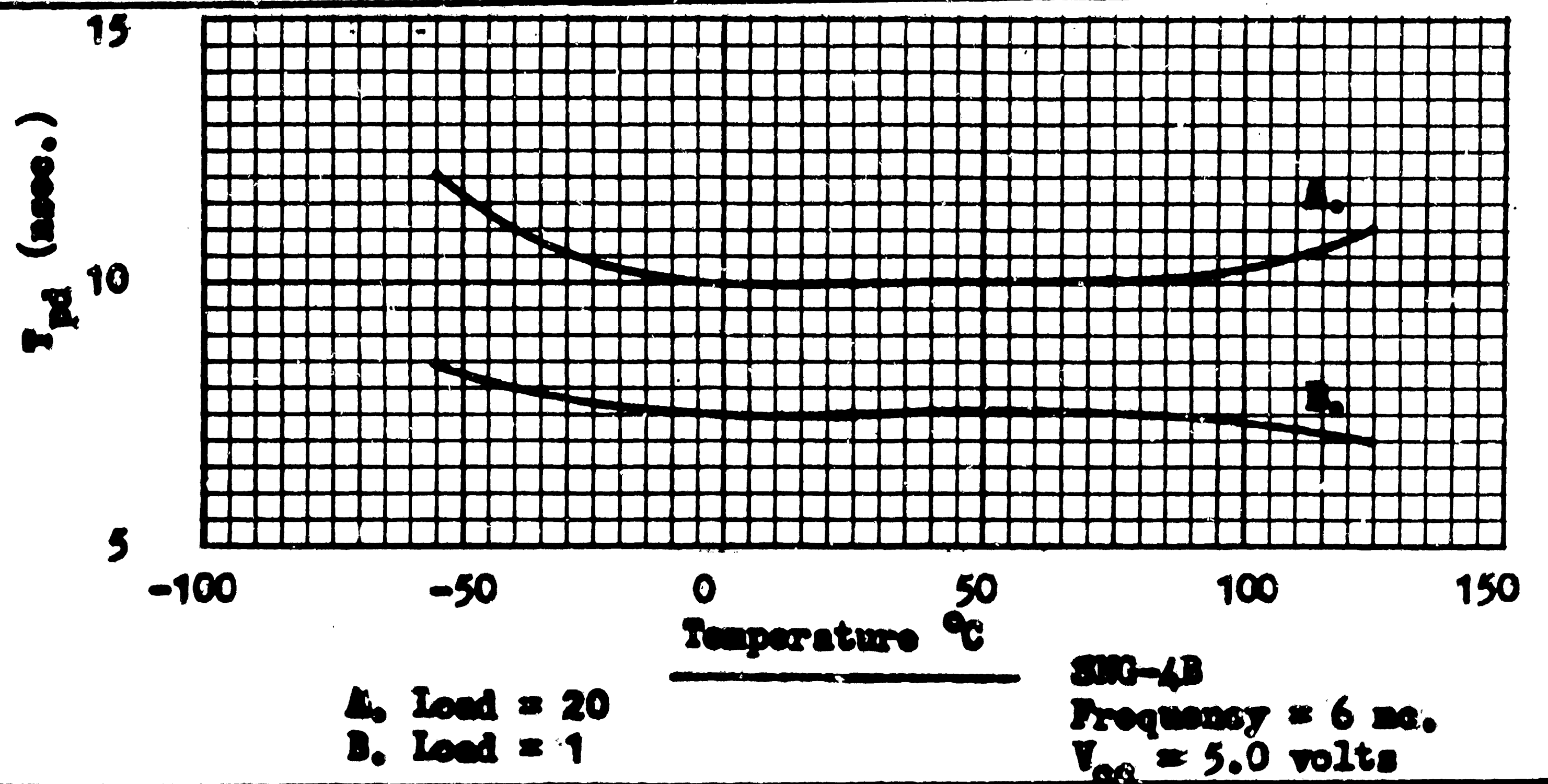
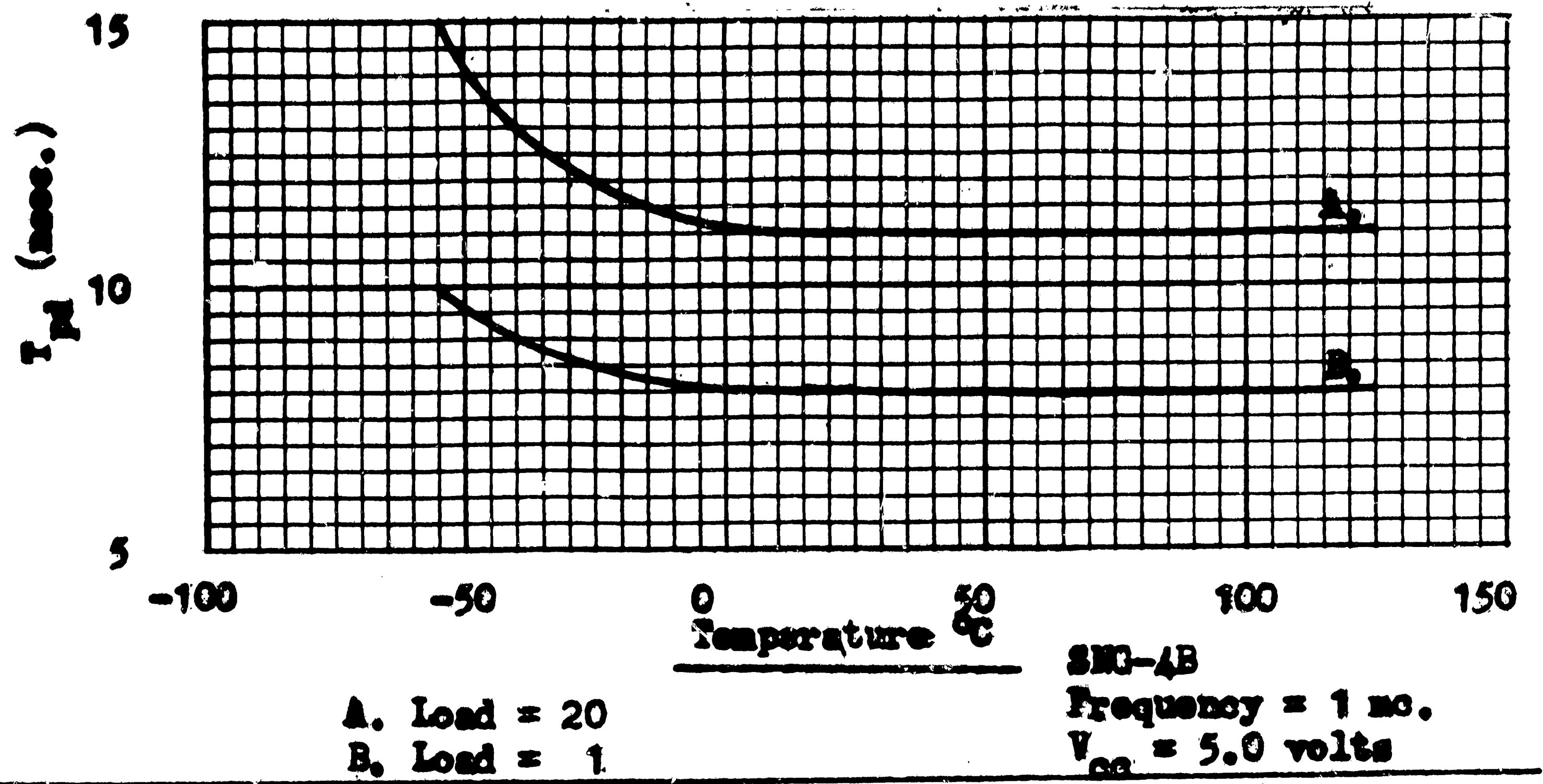
Temperature °C	-55		-40		+25		+85		+125	
Frequency no.	8.4 ---		8.8 ---		9.6 ---		8.9 ---		8.3 ---	
V _{cc} volts	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0
Test Circuit	in	out	in	out	in	out	in	out	in	out
Pulse Amp. volts pp.	3.4	3.3	3.4	3.9	3.6	3.5	3.8	3.6	3.9	3.7
Pulse Width nsec.	62	60	58	56	52	54	53	60	55	67
T _r nsec.	7.2	4.7	7.5	4.9	10	7.6	15	12	20	15
T _f nsec.	7.4	5.5	6.6	5.0	5.0	4.0	4.9	4.0	5.0	4.2
T _d nsec.	—	9.6	—	8.8	—	7.3	—	7.0	—	7.0
T _s nsec.	—	8.5	—	8.1	—	7.7	—	8.0	—	9.0
T _{pd} nsec.	—	8.5	—	7.9	—	7.0	—	6.9	—	7.0

SNG 4 B Ring Counter (7 element)

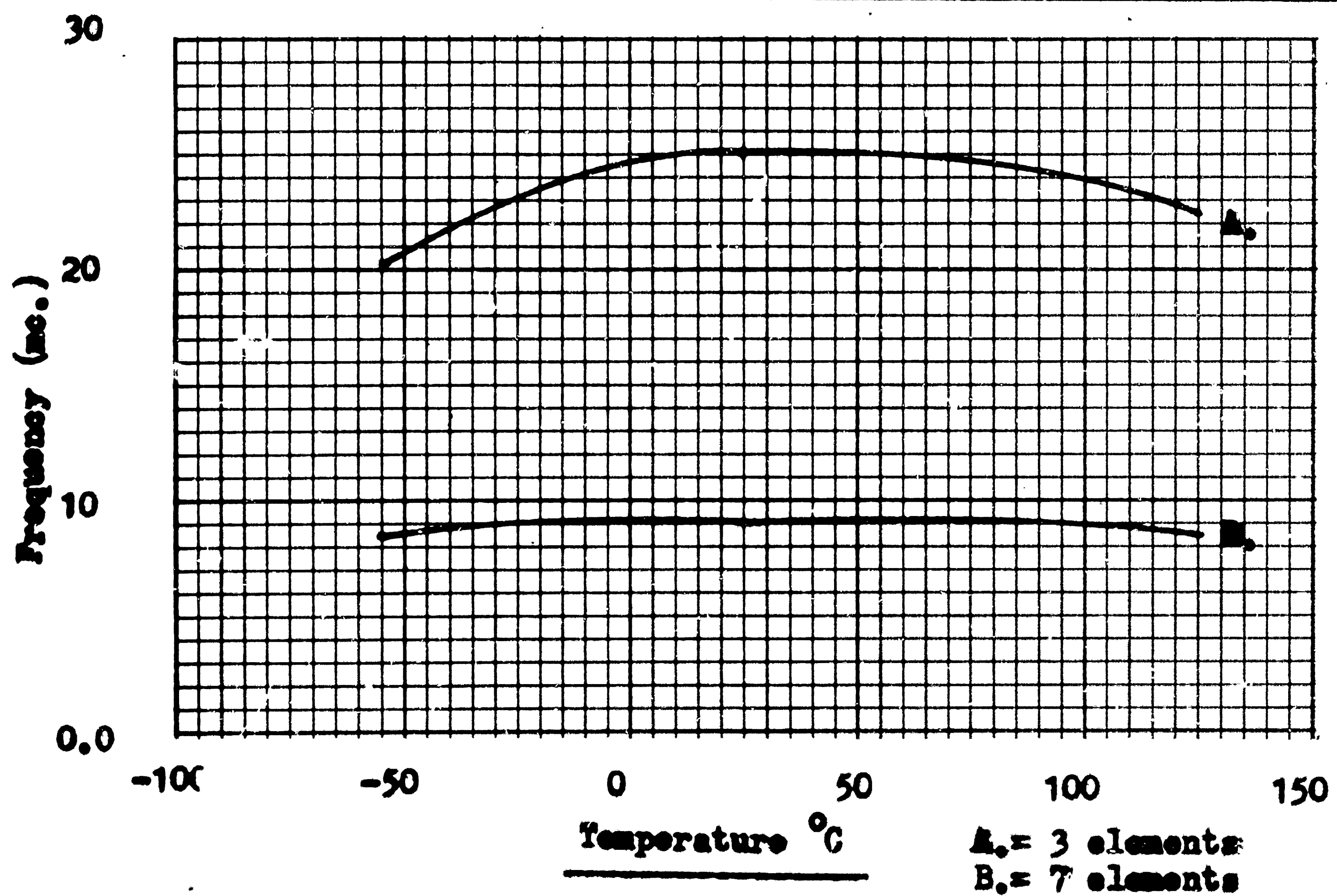
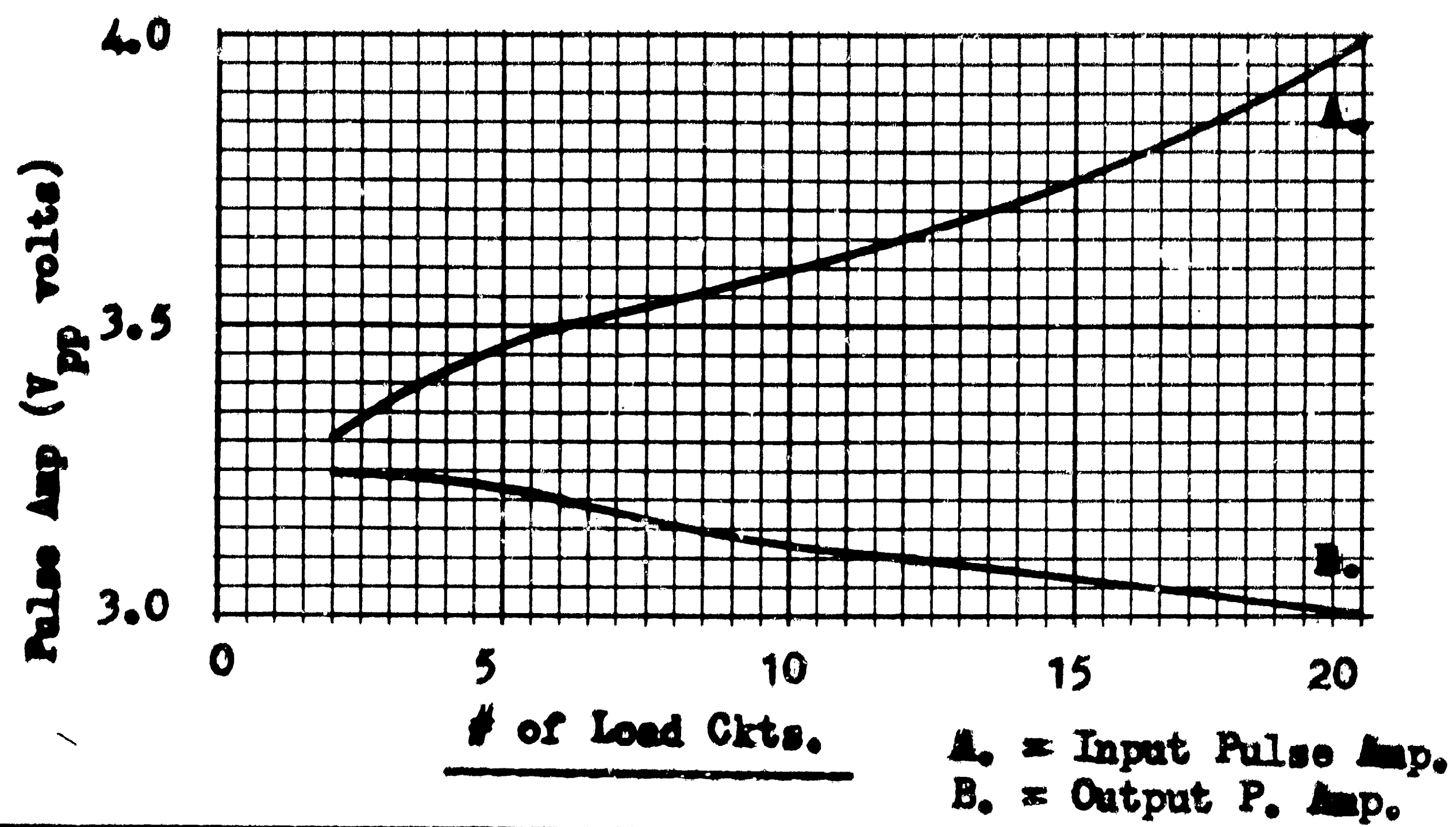
Temperature °C	-55		-40		+25		+85		+125	
Frequency mc.	8.8 —		9.4 —		10 —		9.2 —		8.3 —	
V _{cc} volts	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Test Circuit	in	out	in	out	in	out	in	out	in	out
Pulse Amp. volts pp.	3.9	3.7	4.0	3.8	4.1	3.9	4.4	4.2	4.5	4.3
Pulse Width nsec.	56	56	53	53	49	52	50	60	53	68
T _r nsec.	8.3	5.2	9.0	5.6	12	8.7	17	13	21	16
T _f nsec.	6.5	5.0	5.8	4.5	4.6	3.9	4.5	4.0	4.8	4.1
T _d nsec.	—	8.4	—	7.7	—	6.6	—	6.4	—	6.6
T _s nsec.	—	8.4	—	8.0	—	7.7	—	8.3	—	9.0
T _{pd} nsec.	—	7.9	—	7.4	—	6.6	—	6.5	—	7.5

SNG 4 B Ring Counter (3 element)

Temperature °C	-55 —		-40 —		+25 —		+85 —		+125 —	
Frequency mc.	20.1 —		21.8 —		25.0 —		24.8 —		22.8 —	
V _{cc} volts	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0
Test Circuit	in	out	in	out	in	out	in	out	in	out
Pulse Amp. volts pp.	3.6	3.4	3.6	3.5	3.8	3.3	3.8	3.7	3.5	3.5
Pulse Width nsec.	27	25	25	23	19	22	18	23	17	27
T _r nsec.	5.0	5.0	5.0	5.0	11	9.0	11	10	13	13
T _f nsec.	6.7	6.0	6.0	5.0	4.0	4.0	5.0	4.0	5.0	4.0
T _d nsec.	—	9.0	—	8.0	—	7.0	—	7.0	—	7.0
T _s nsec.	—	8.0	—	8.0	—	8.0	—	8.0	—	8.0
T _{pd} nsec.	—	8.2	—	7.7	—	6.5	—	6.0	—	6.0



SMG-4B
 Freq. = 1 mc.
 $V_{cc} = 5.0$ v.
 $T = 25^{\circ}\text{C}$



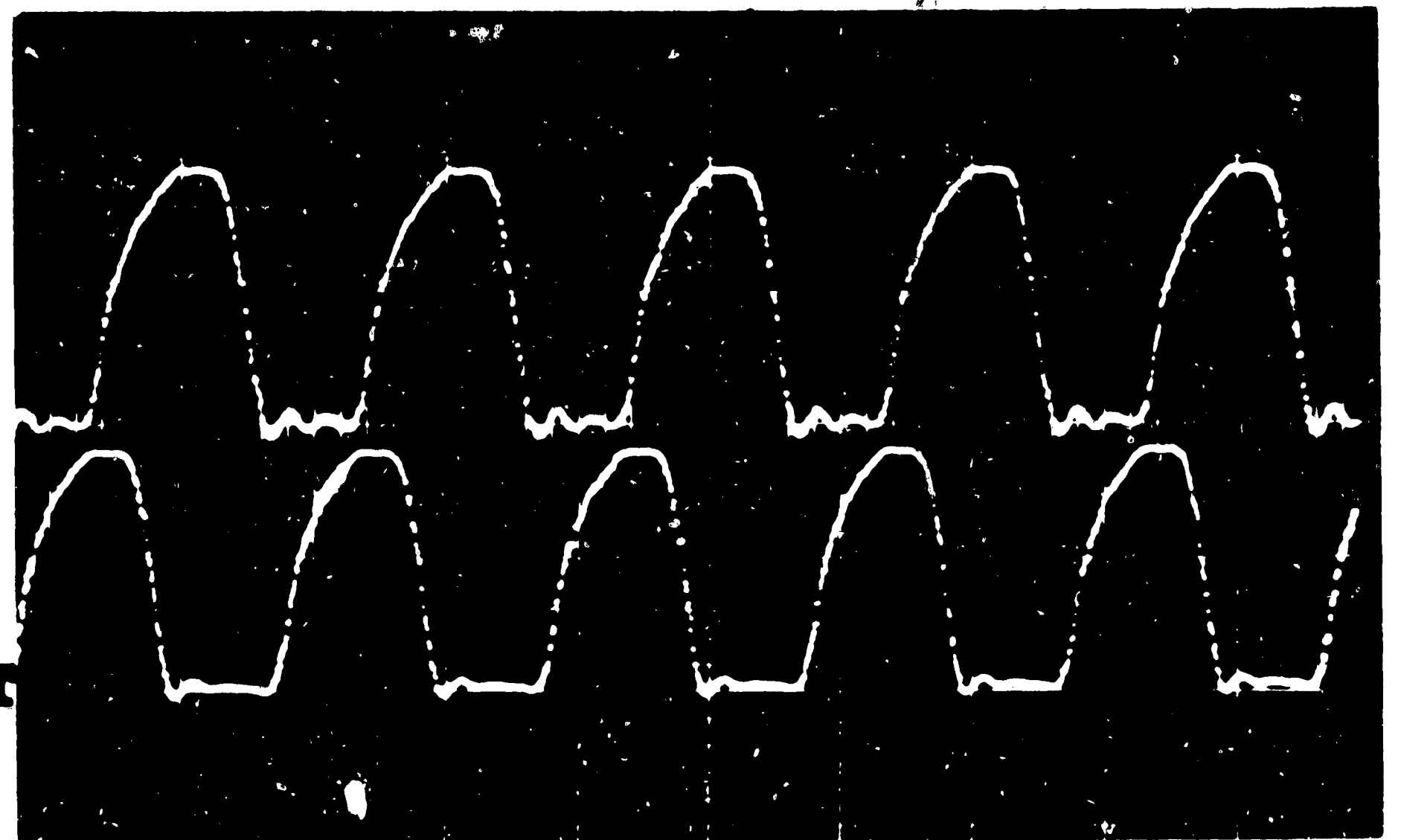
SMG-4B Ring Counter
 $V_{cc} = 5.0$ volts

Ring Counter
 SNG-4B
 Frequency = 24.2 mc.
 (3 elements)
 Load = 1 ckt.
 $V_{cc} = 5.0$ v.
 Temperature = 25°C.

2 v./div.

IN

OUT



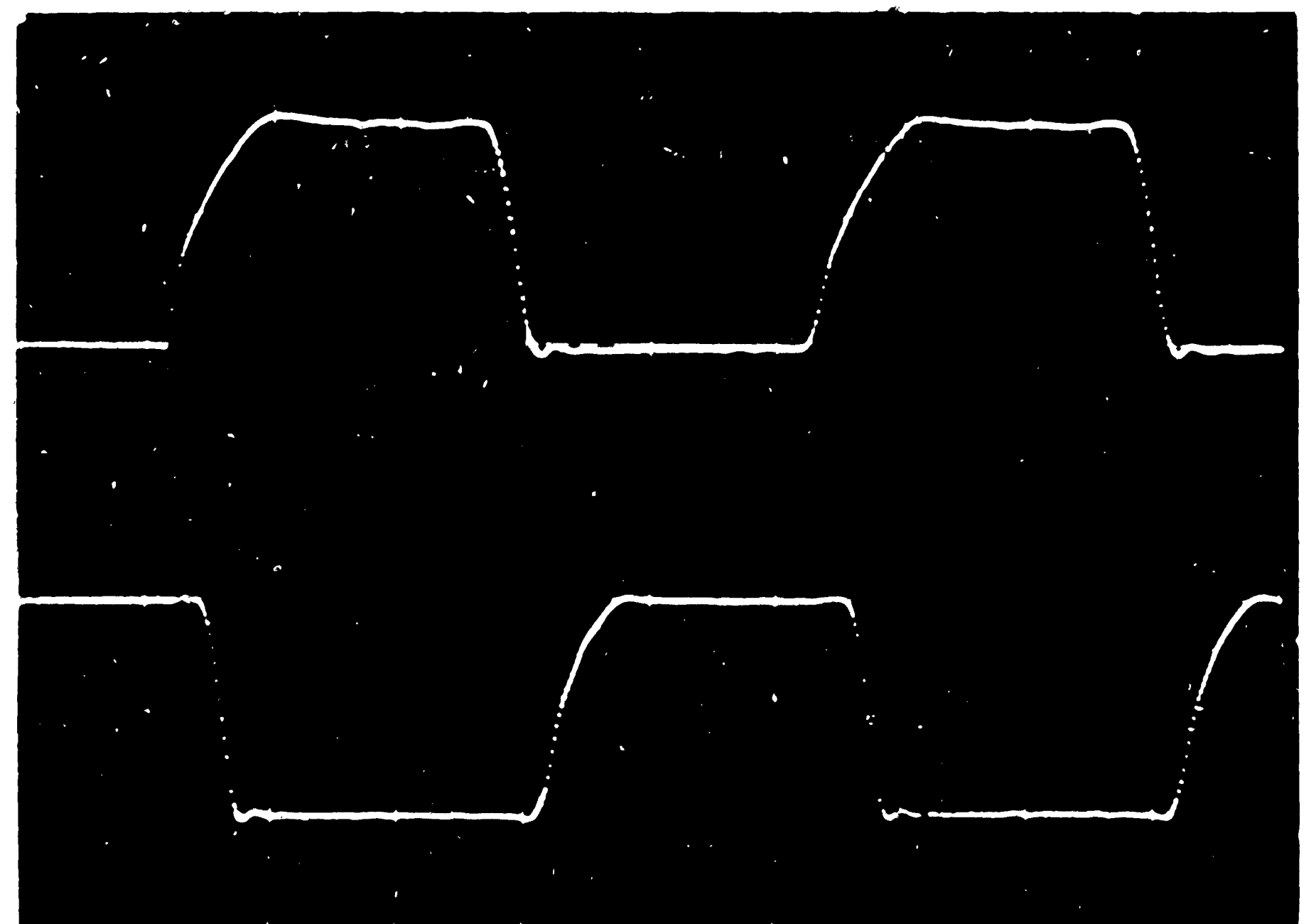
20 nsec./div.

Ring Counter
 SNG-4B (7 elements)
 Frequency = 9.58 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C

2 v./div.

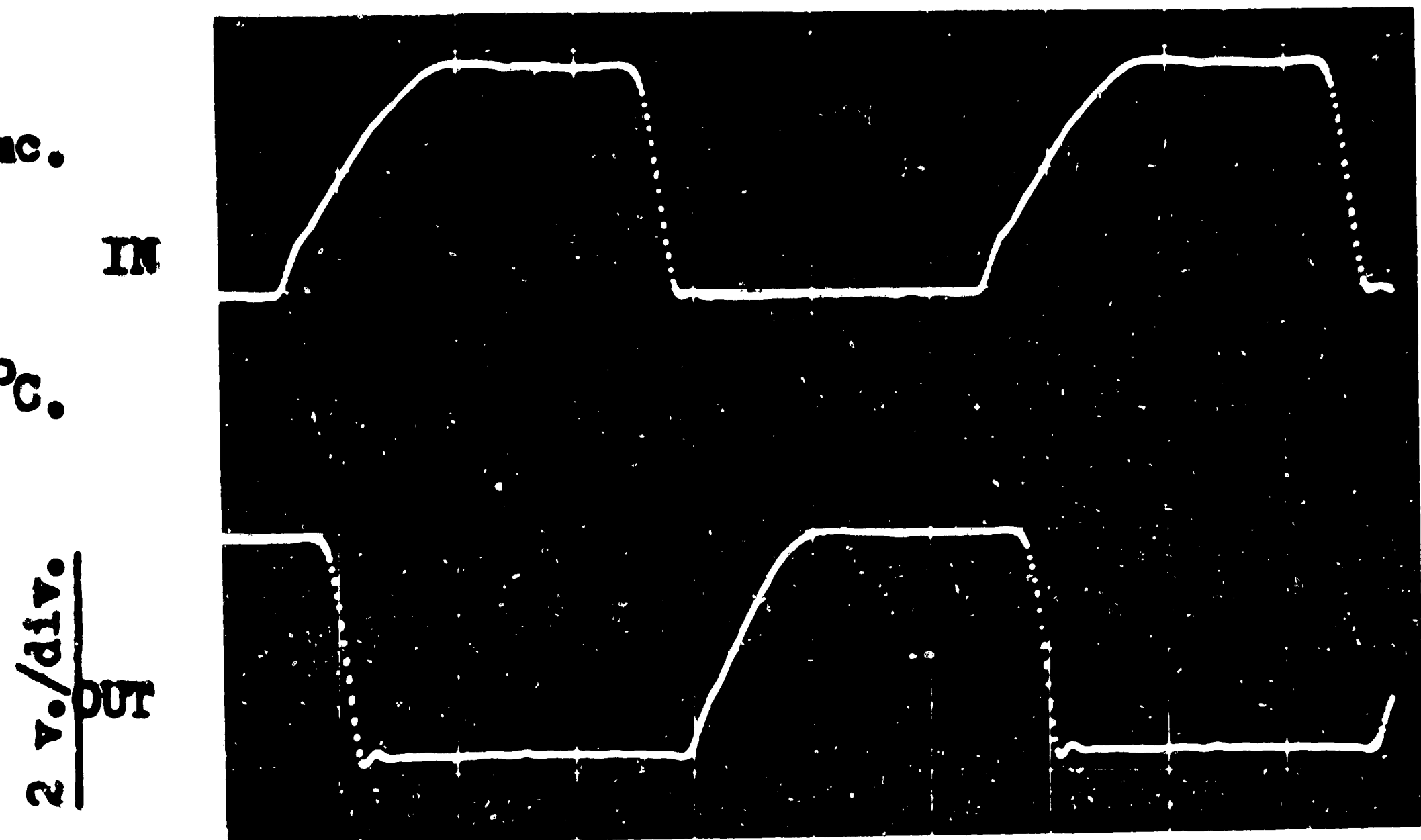
IN

OUT



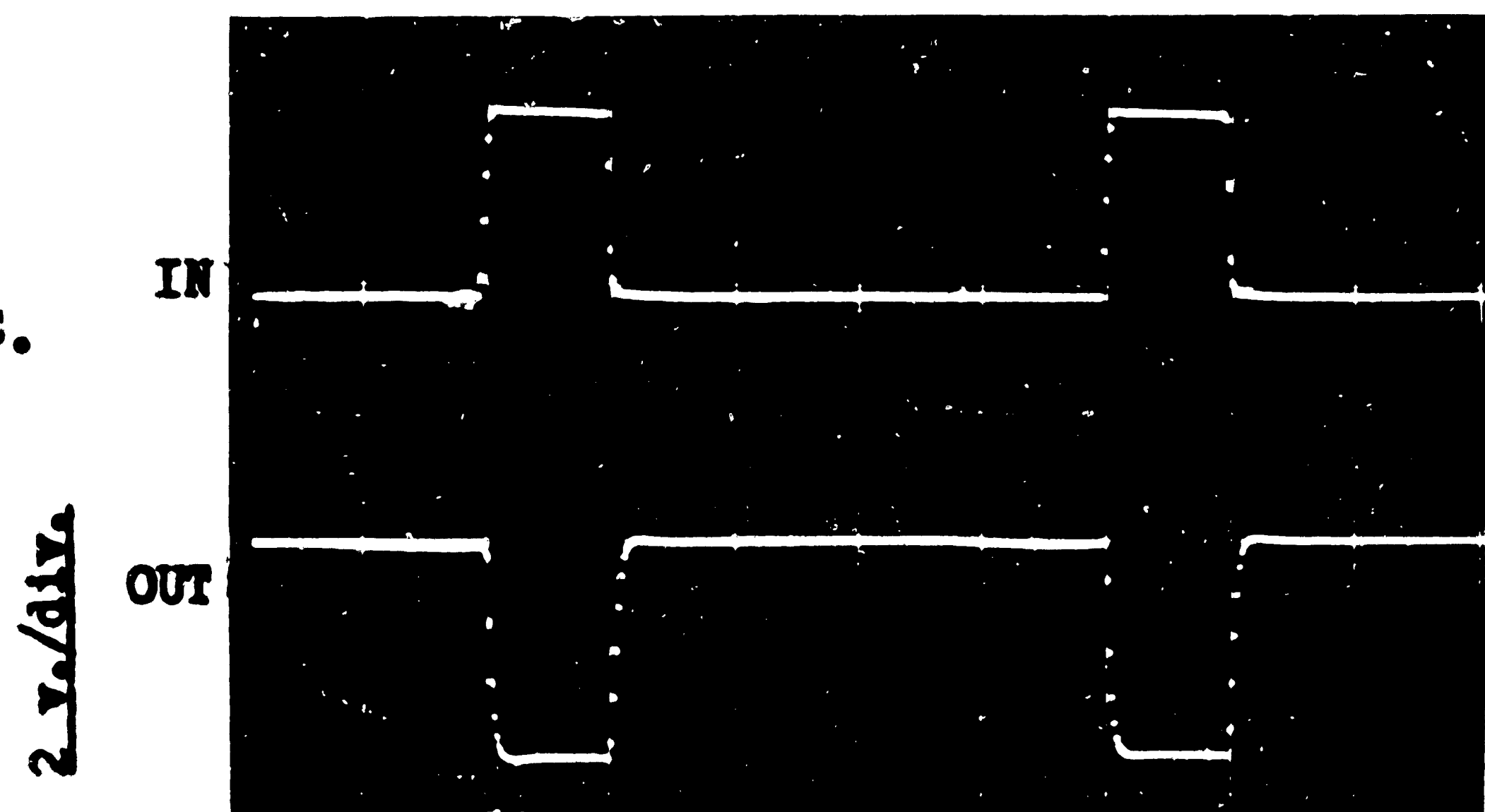
20 nsec./div.

Ring Counter
 SNG-4B
 Frequency = 8.26 mc.
 (7 elements)
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 125°C.

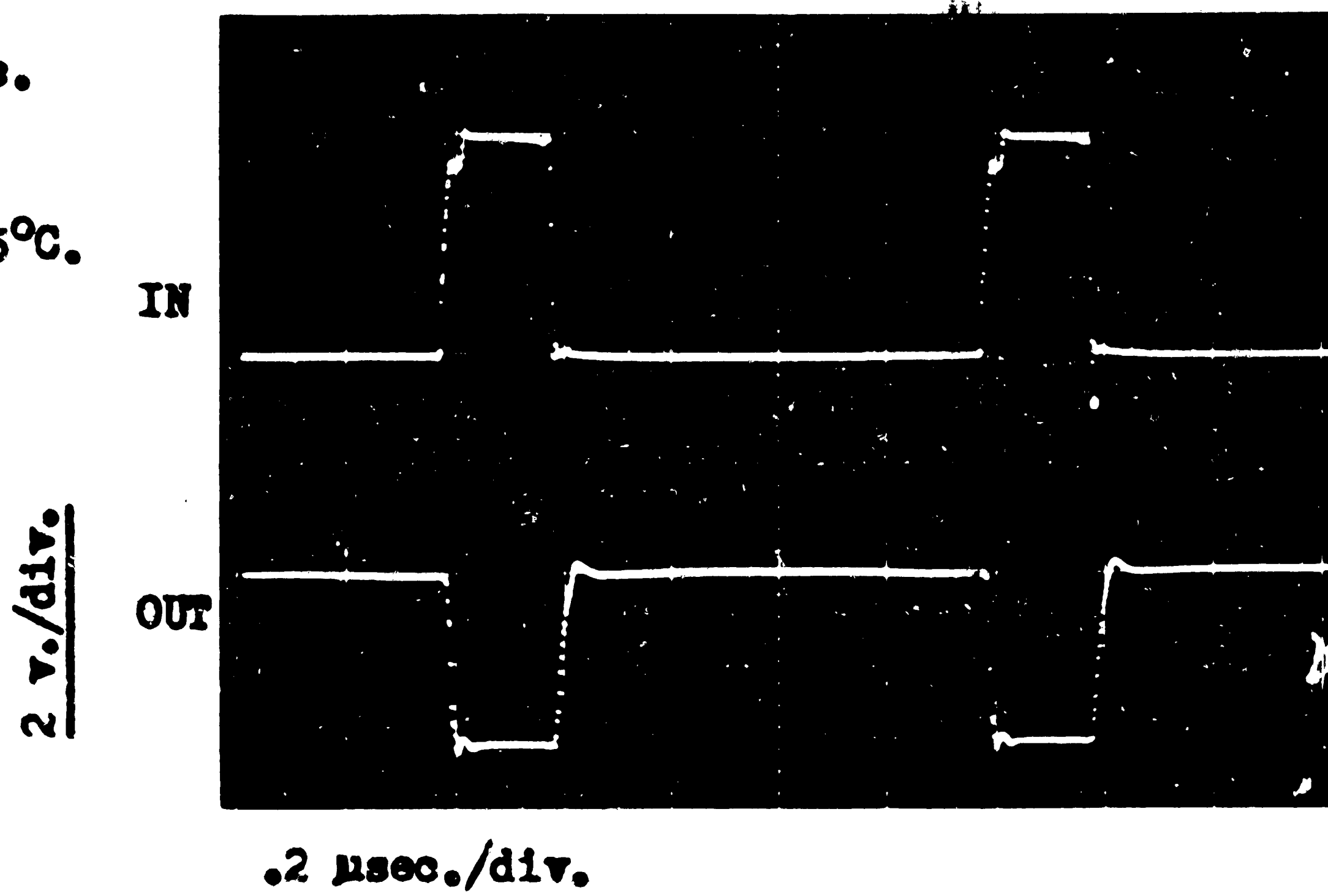


End of ring counter traces.

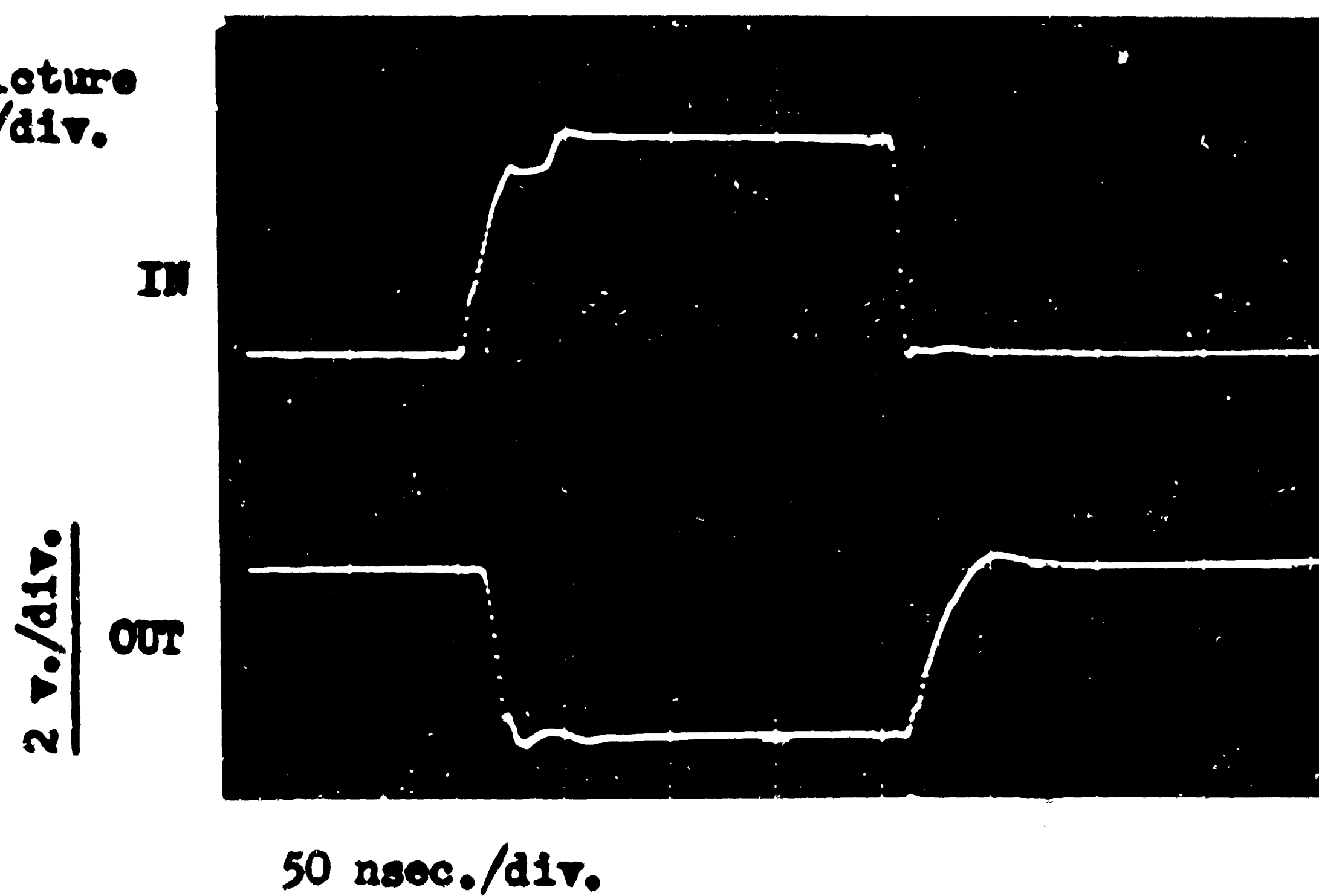
SNG-4B
 Frequency = 1 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C.



SNG-4B
 Frequency = 1 mc.
 Load = 20 ckts.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C.



SNG-4B
 Same as above picture
 except 50 nsec./div.



SNG-4B
 Frequency = 1 mc.
 Load = 20 ckts.
 $V_{cc} = 5.0$ volts
 Temperature = -55°C . IN

2 v./div.
 OUT



50 nsec./div.

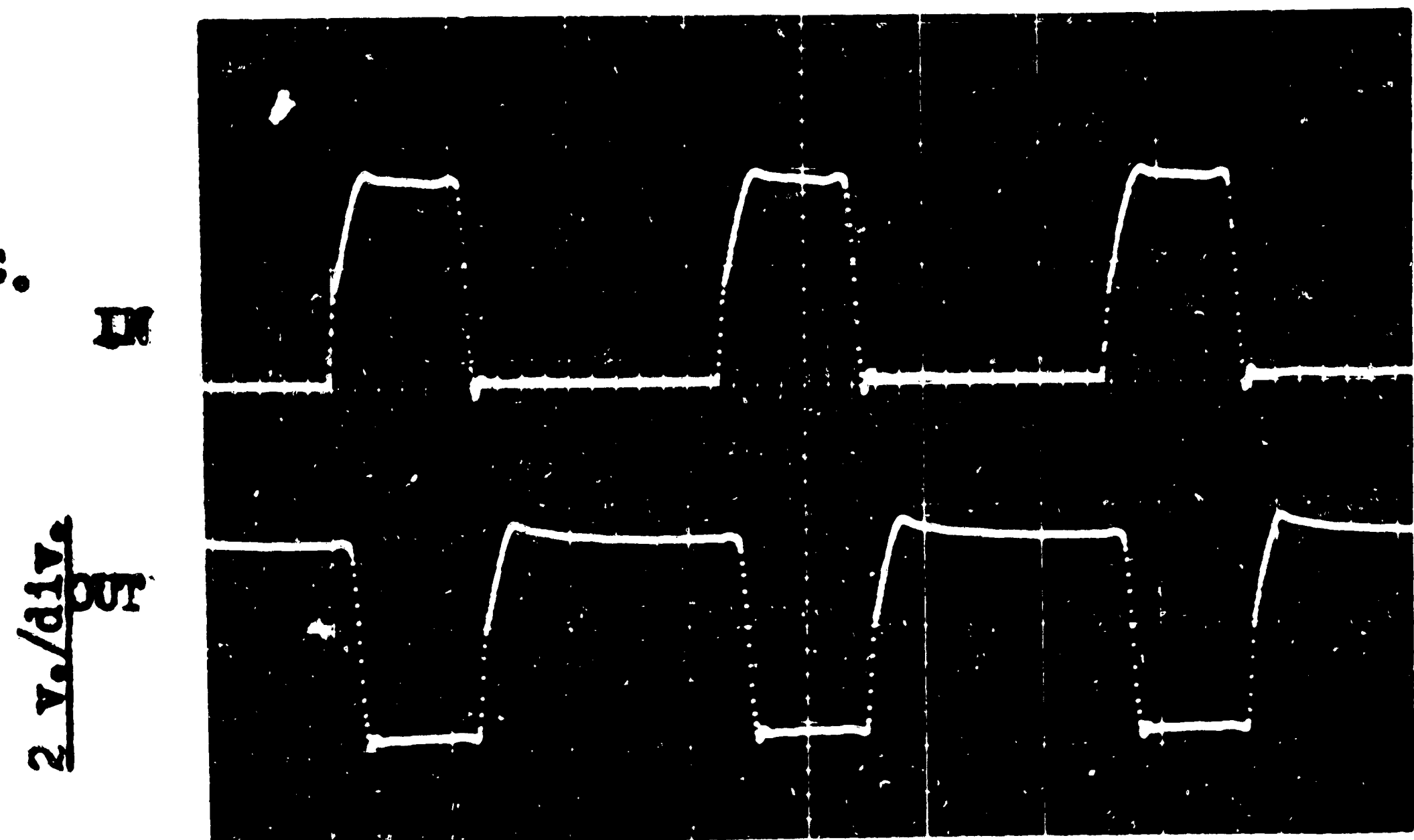
SNG-4B
 Frequency = 1 mc.
 Load = 20 ckts.
 $V_{cc} = 5.0$ volts
 Temperature = 125°C . IN

2 v./div.
 OUT



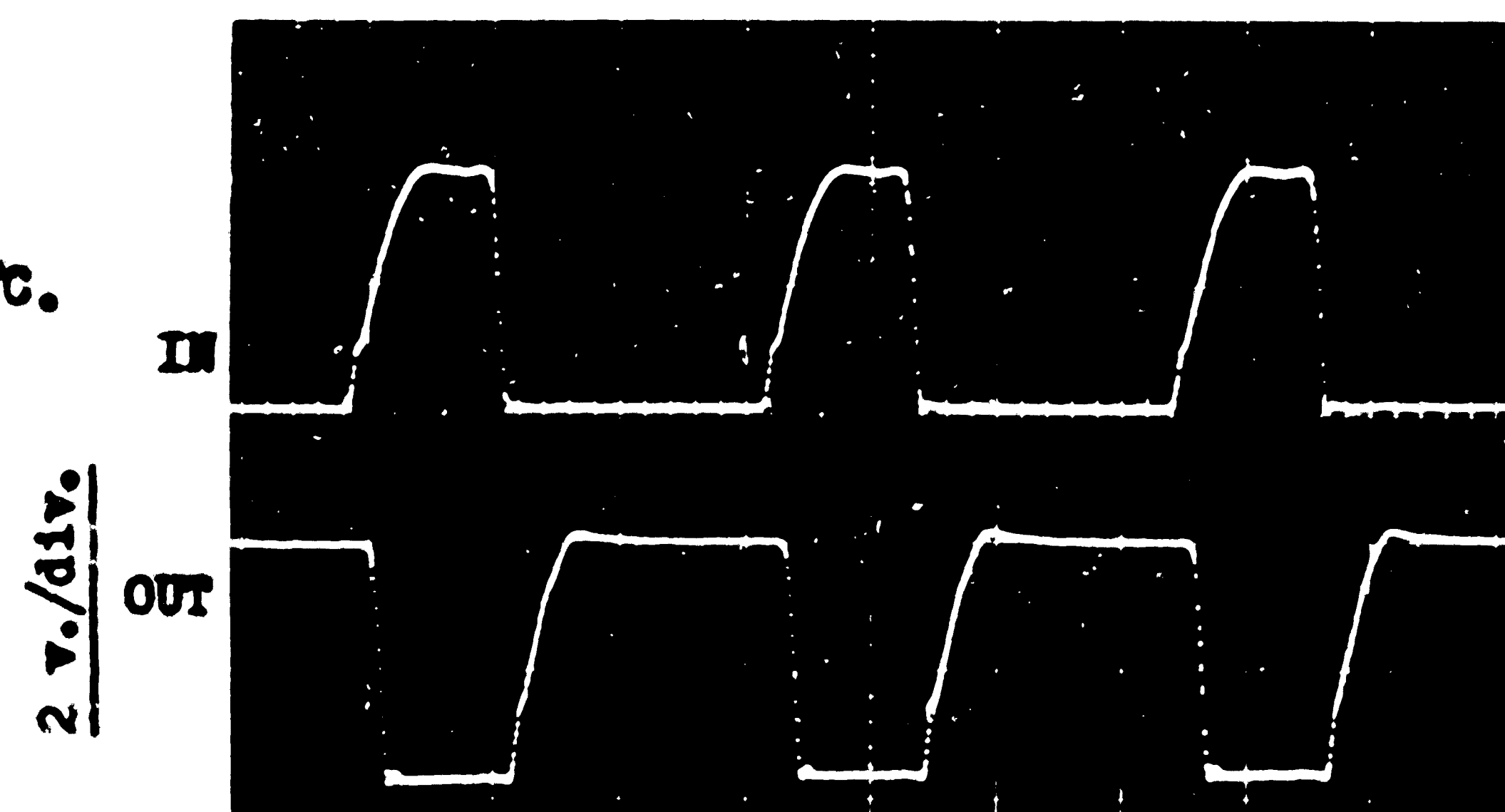
50 nsec./div.

SNG-4B
 Frequency = 6 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C.



50 nsec./div.

SNG-4B
 Frequency = 6 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 125°C.

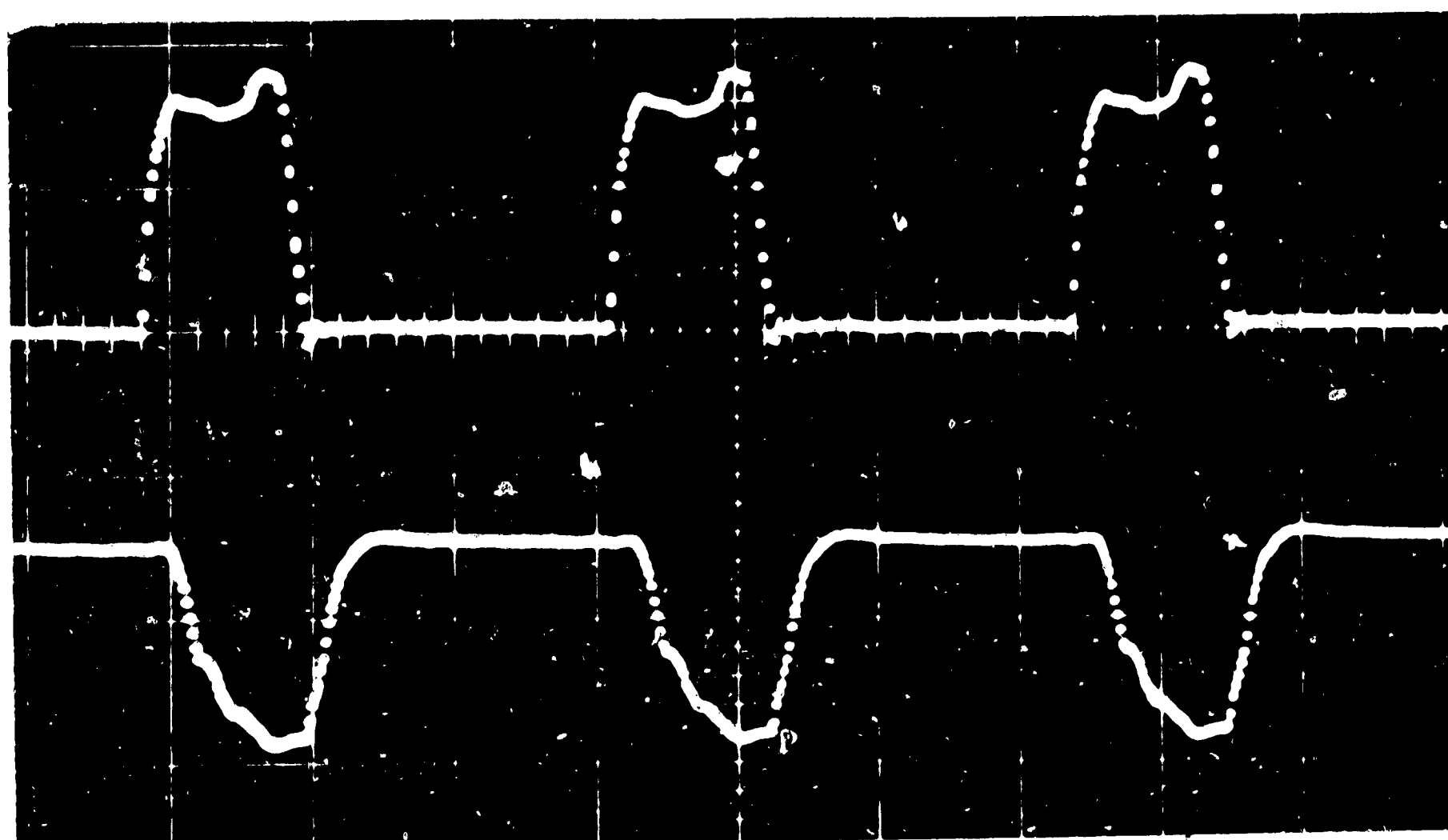


50 nsec./div.

SNG-4B
 Frequency = 6 mc.
 Load = 20 ckts.
 $V_{cc} = 5.0$ volts
 Temperature = -55°C . IN

2 v./div.

OUT

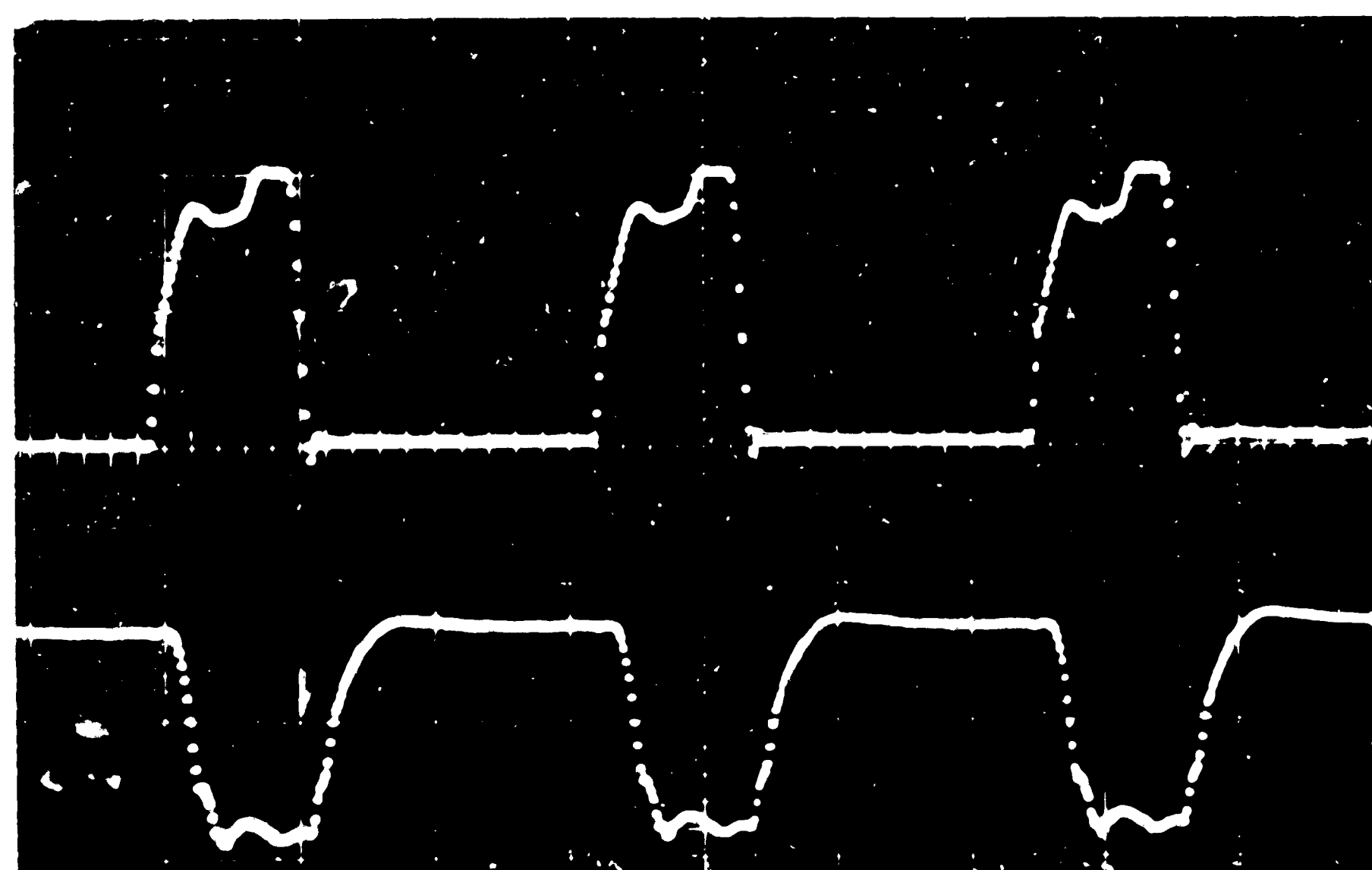


50 nsec./div.

SNG-4B
 Frequency = 6 mc.
 Load = 20 ckts.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C . IN

2 v./div.

OUT

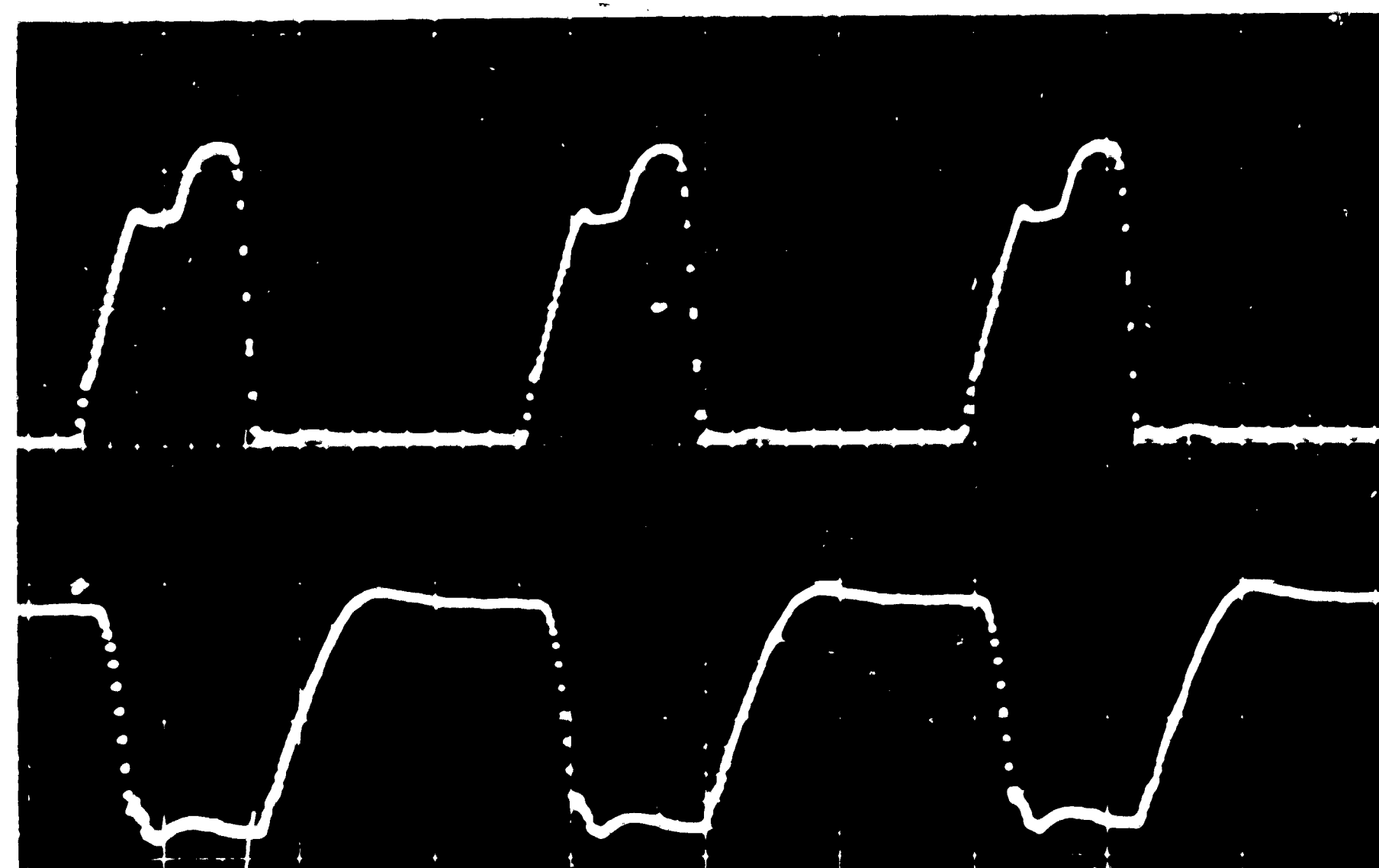


50 nsec./div.

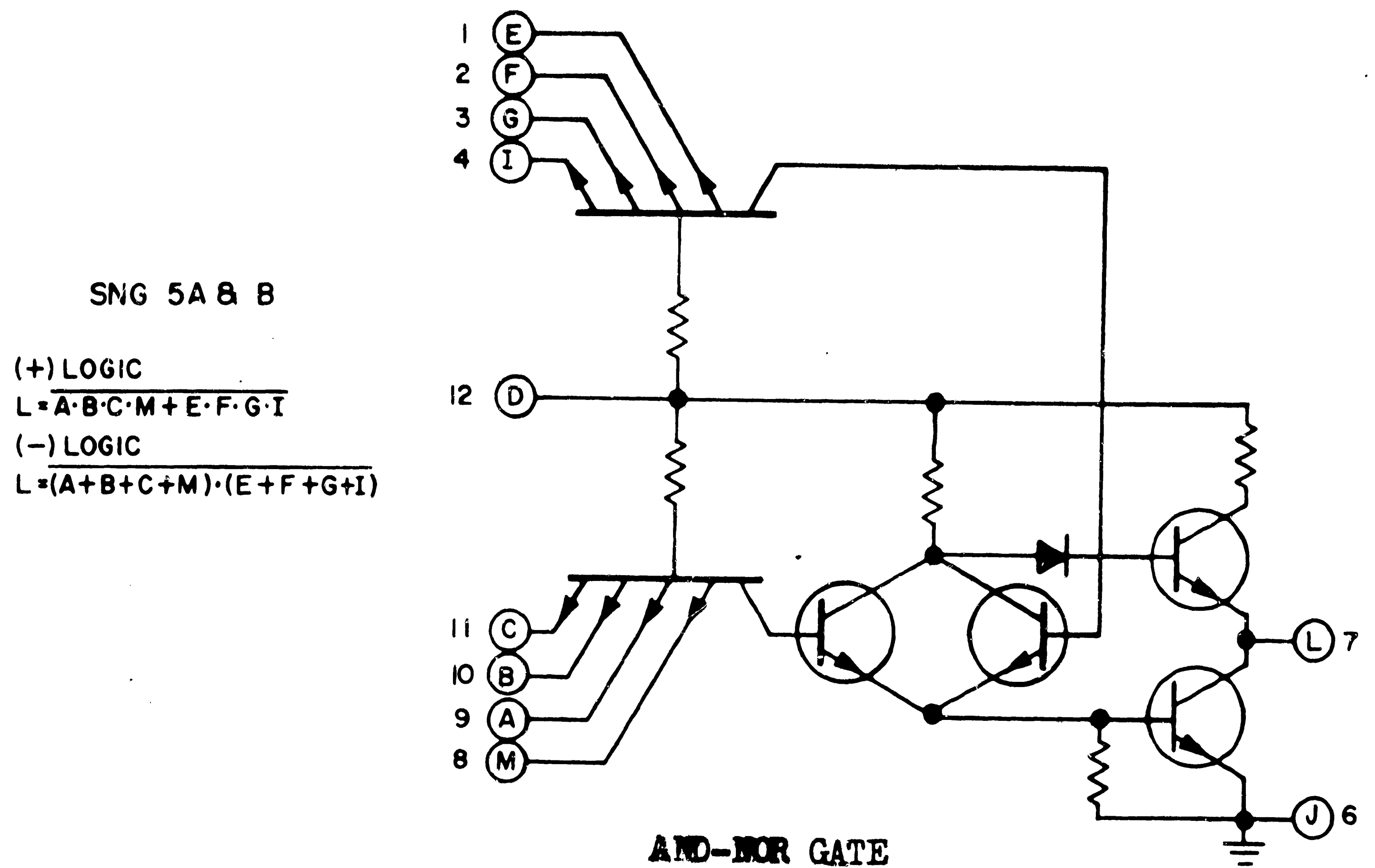
SNG-4B
 Frequency = 6 mc.
 Load = 20 ckts.
 $V_{cc} = 5.0$ volts
 Temperature = 125°C . IN

2 v./div.

OUT

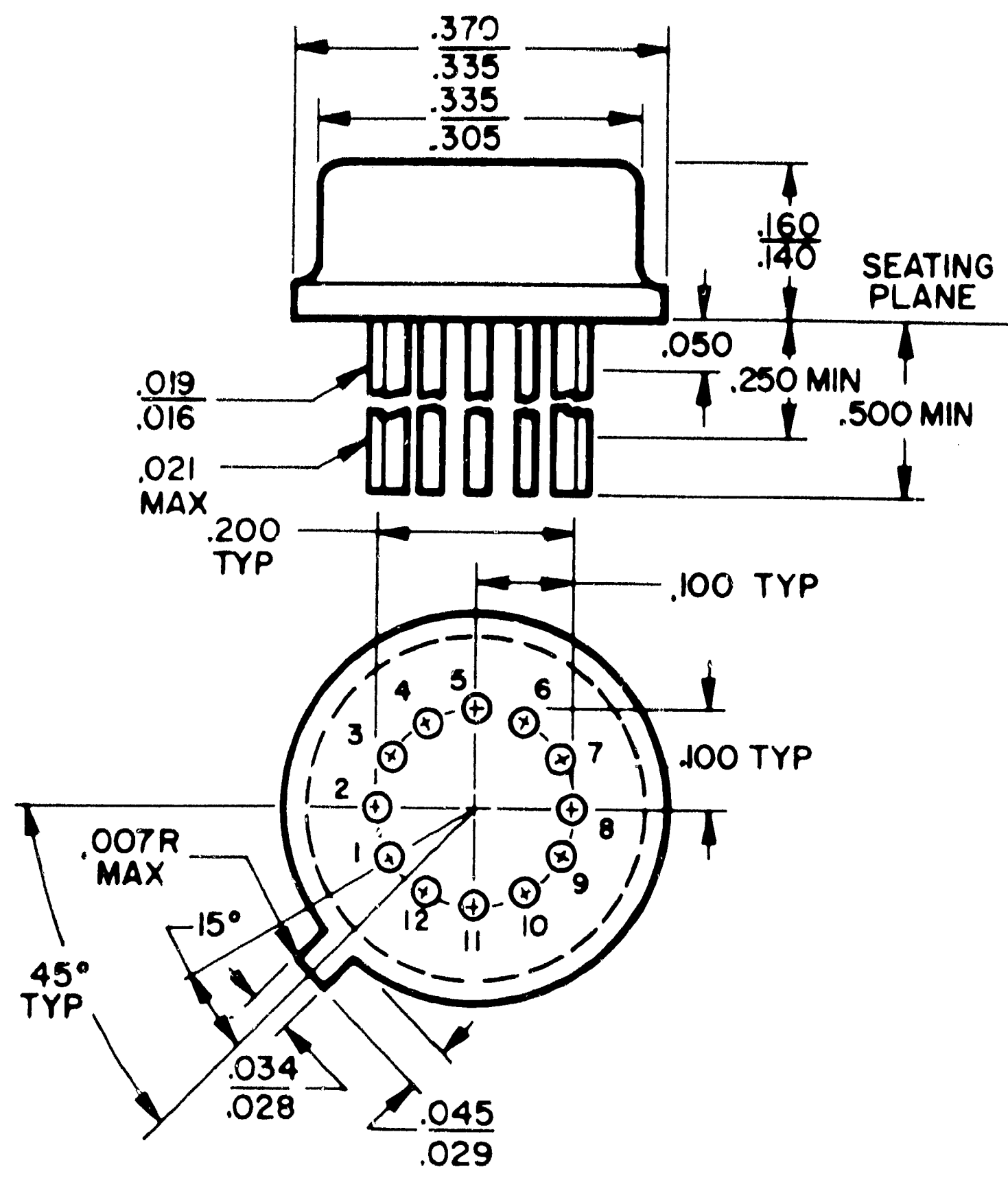


50 nsec./div.

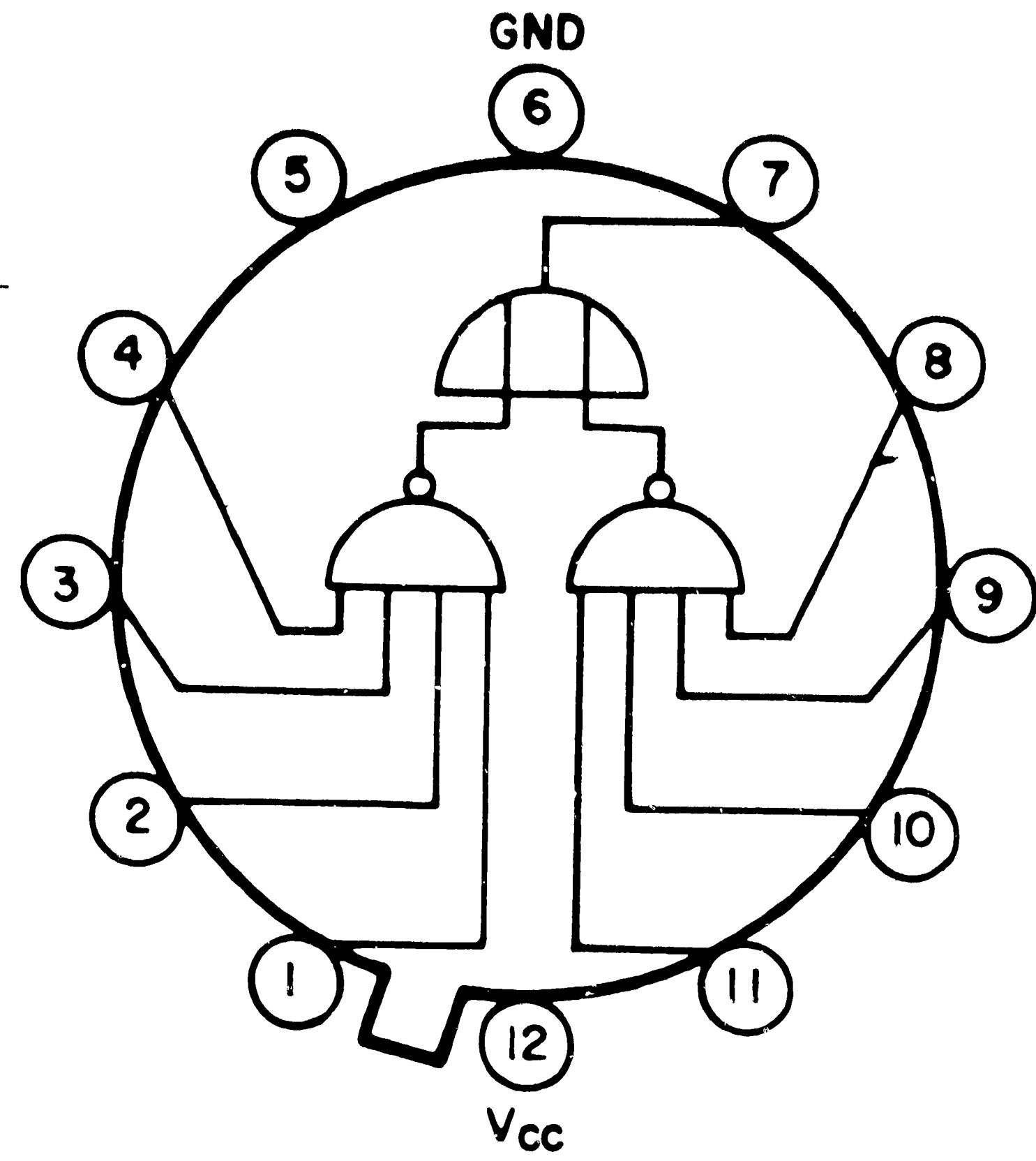


The SNG-5 AND-NOR gate functions as a **AND-NOR** element or as an **EXCLUSIVE-OR** element or one-half of a set-reset-trigger flip-flop. It is a monolithic, epitaxial, planar type and requires a single power supply.

The "A" version has three input points per input transistor, while the "B" version has four input points per input transistor. Both circuits have dual input transistors.



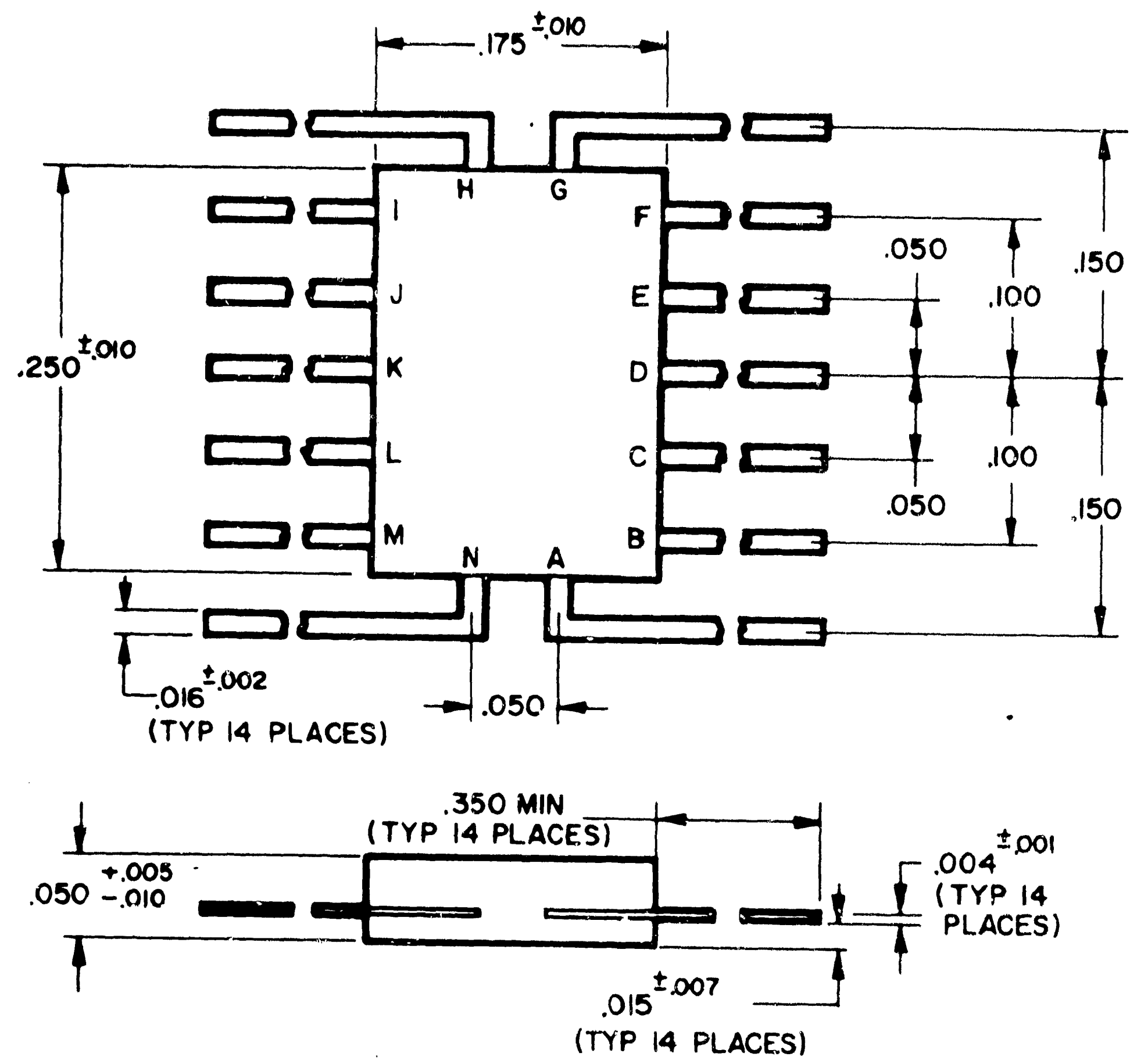
12 LEAD TO-5



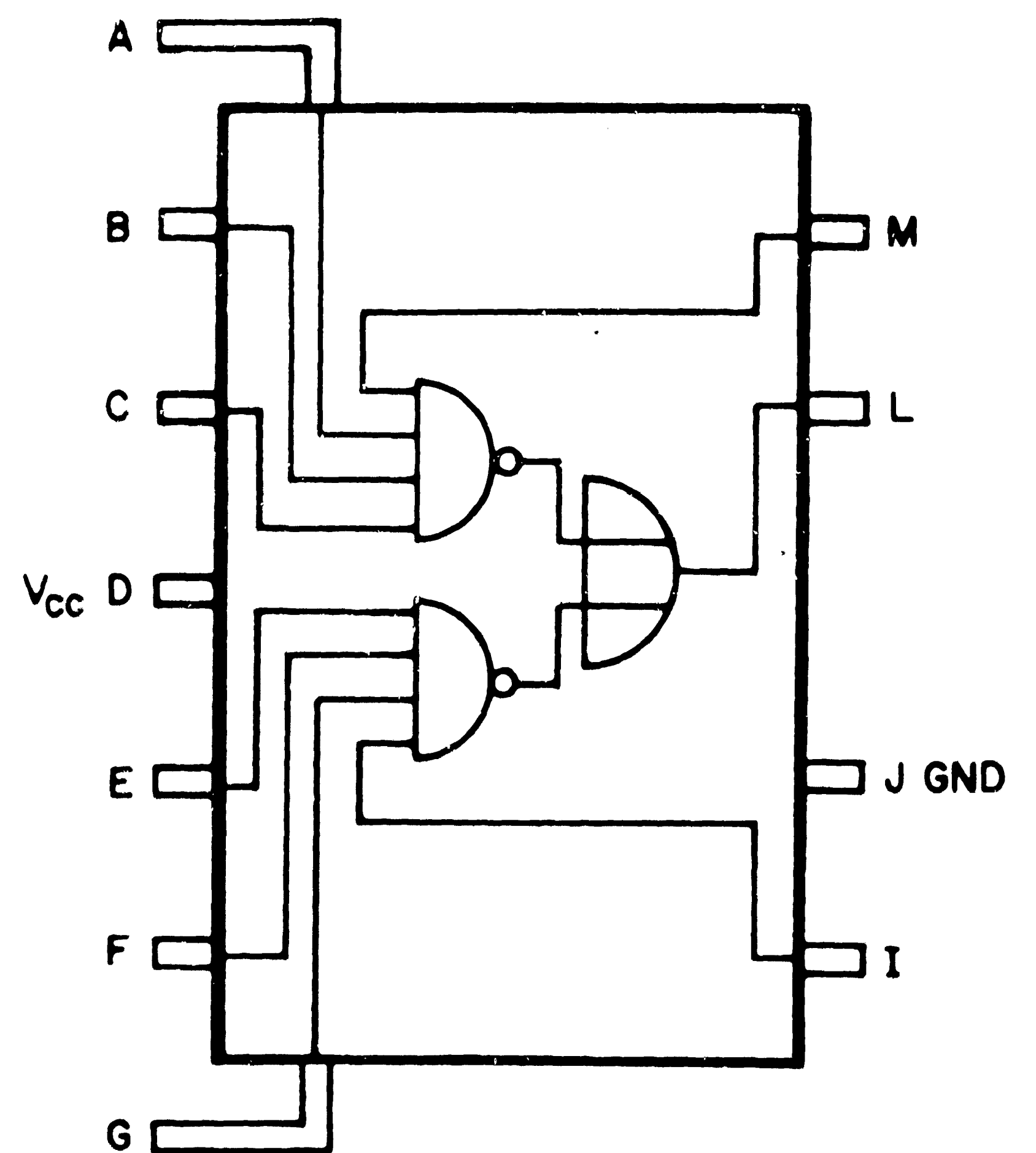
BOTTOM VIEW

SNG-5B

FOR SNG-5A INPUTS 9-A AND 3-G ARE NOT PRESENT



14 LEAD FLAT PACK



TOP VIEW

V_{in} vs. V_{out}

1.) $V_{cc} = 5 \text{ v.}$

2.) Pin #3 @ ground

+125°C

+25 °C

-55 °C

$V_{out}(\text{Ma.})$

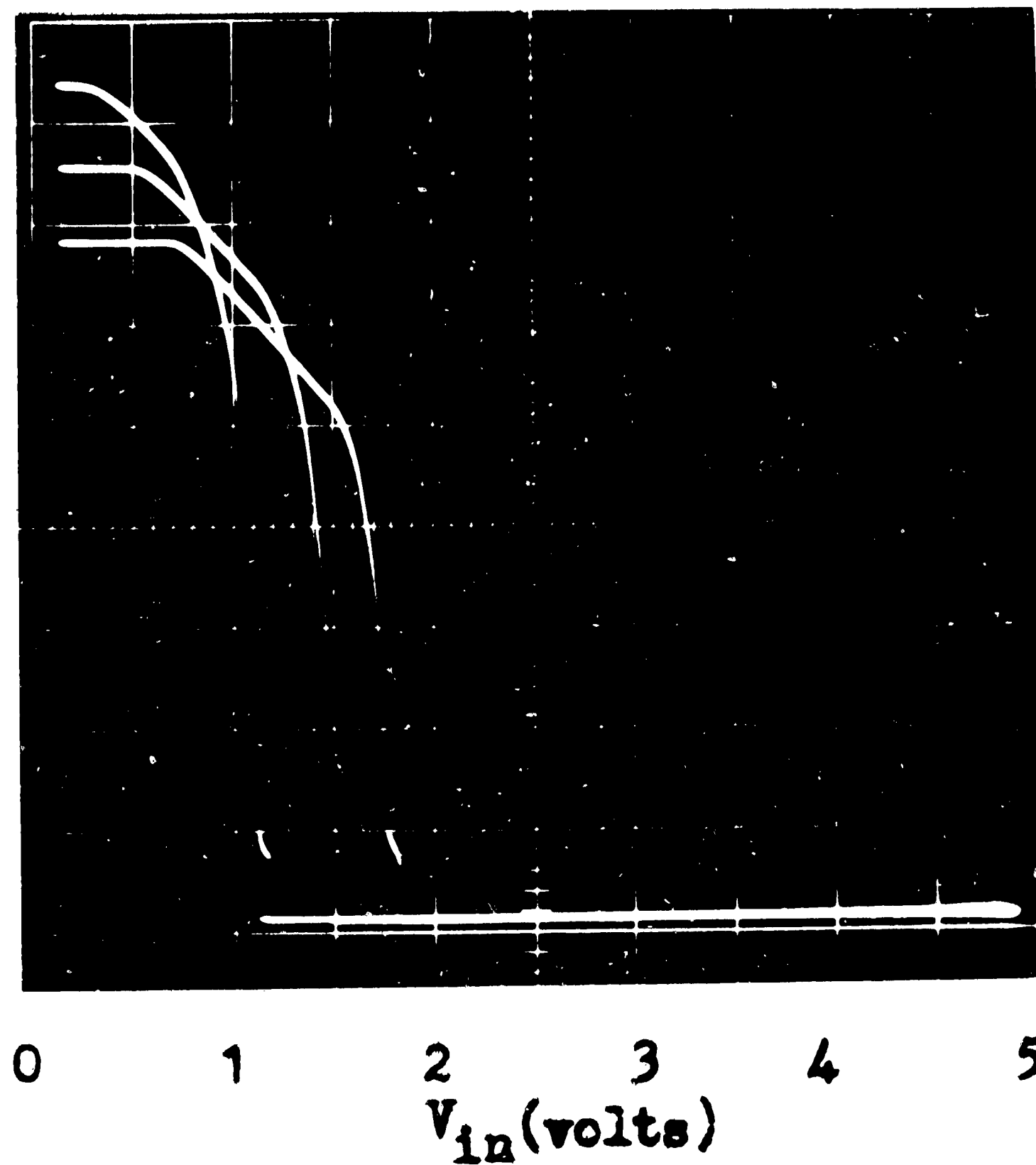
4

3

2

1

0



V_{in} vs. I_{in}

1.) $V_{cc} = 5 \text{ v.}$

2.) $T = 25^\circ\text{C}$

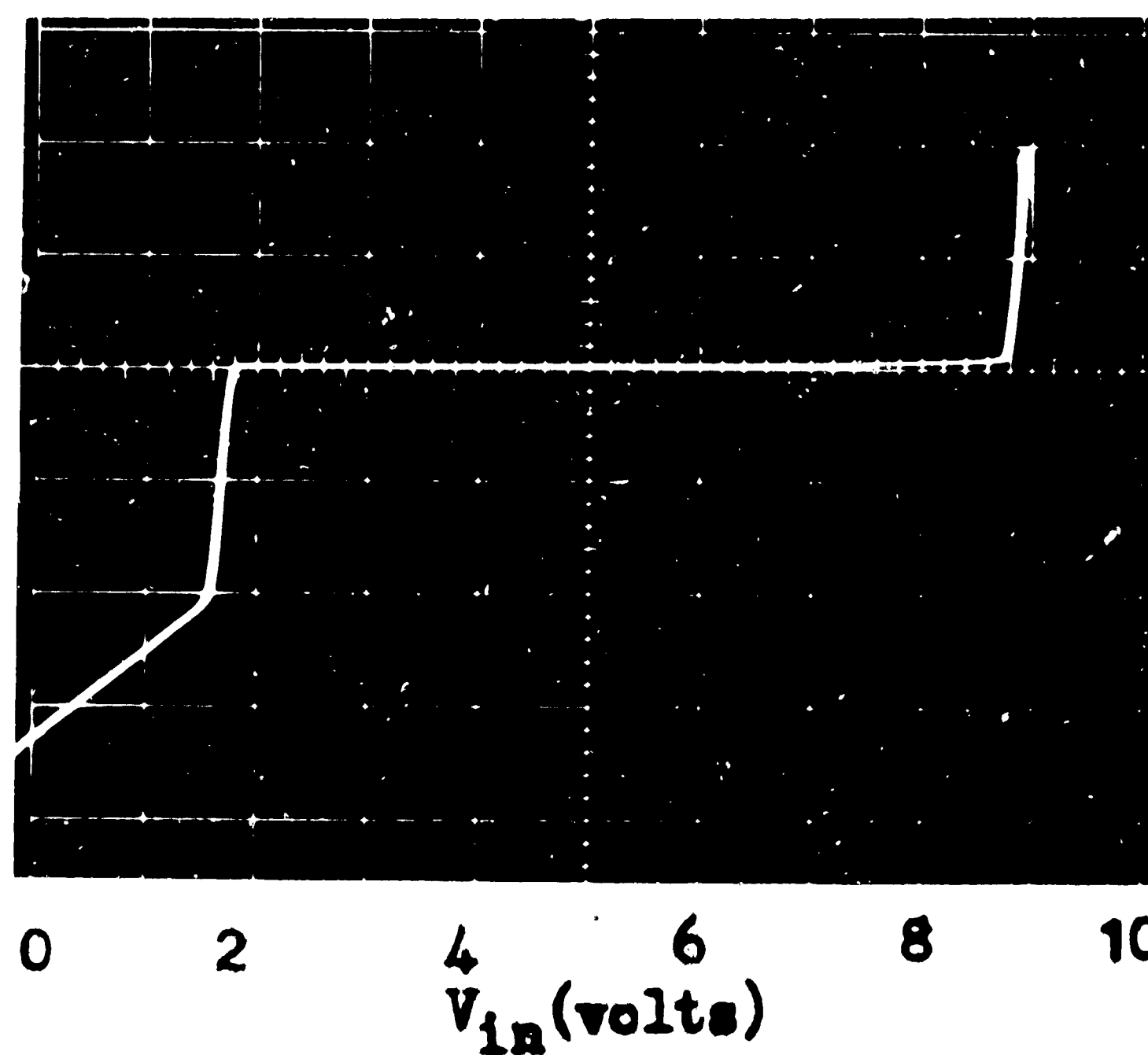
$I_{in}(\text{Ma.})$

0.4

0

-0.4

-0.8



V_{out} vs. I_{out}

1.) $V_{cc} = 5 \text{ v.}$

2.) $T = 25^\circ\text{C}$

3.) Pin #3 & #10
@ ground

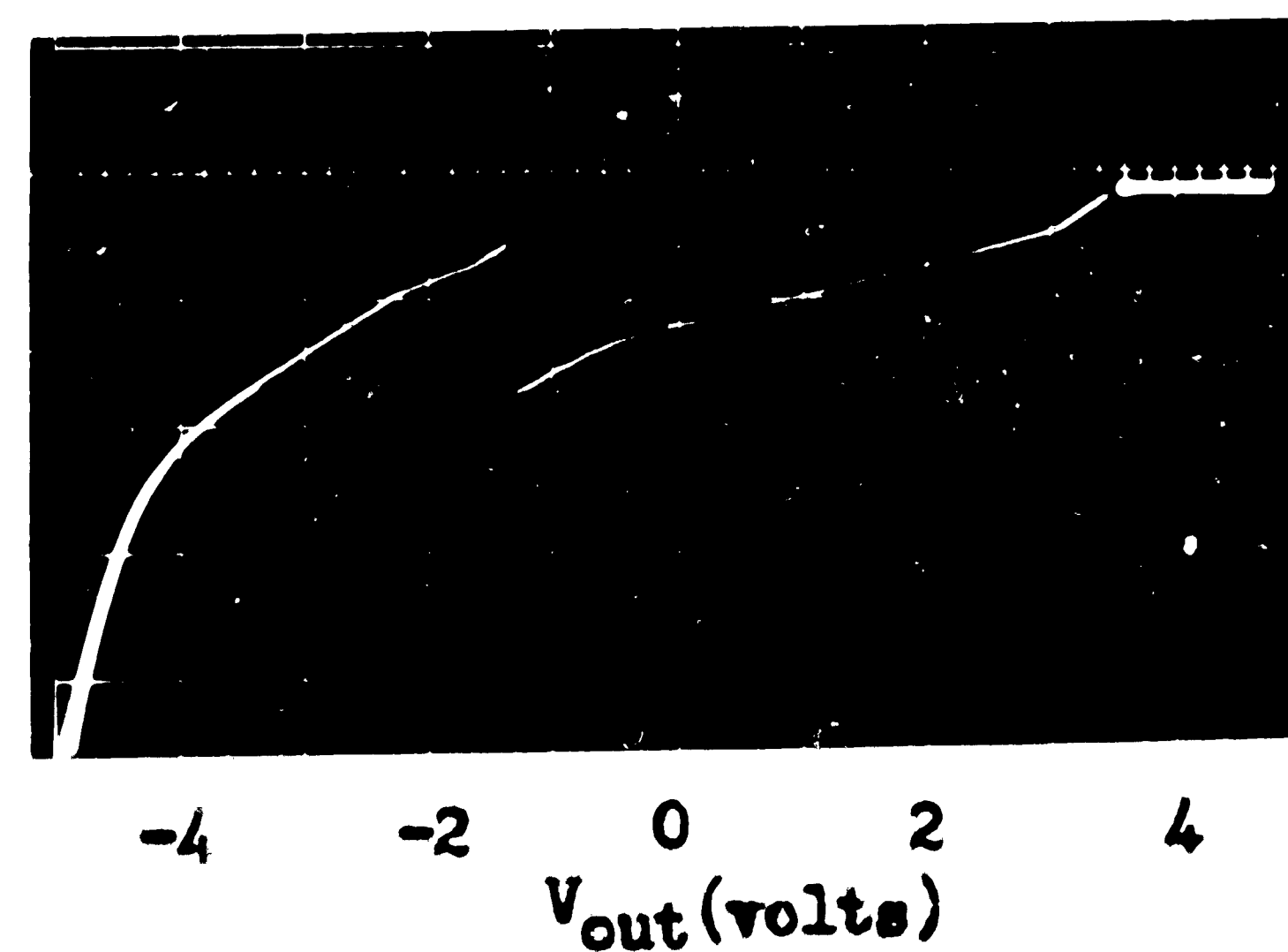
$I_{out}(\text{Ma.})$

+20

0.0

-40

-80

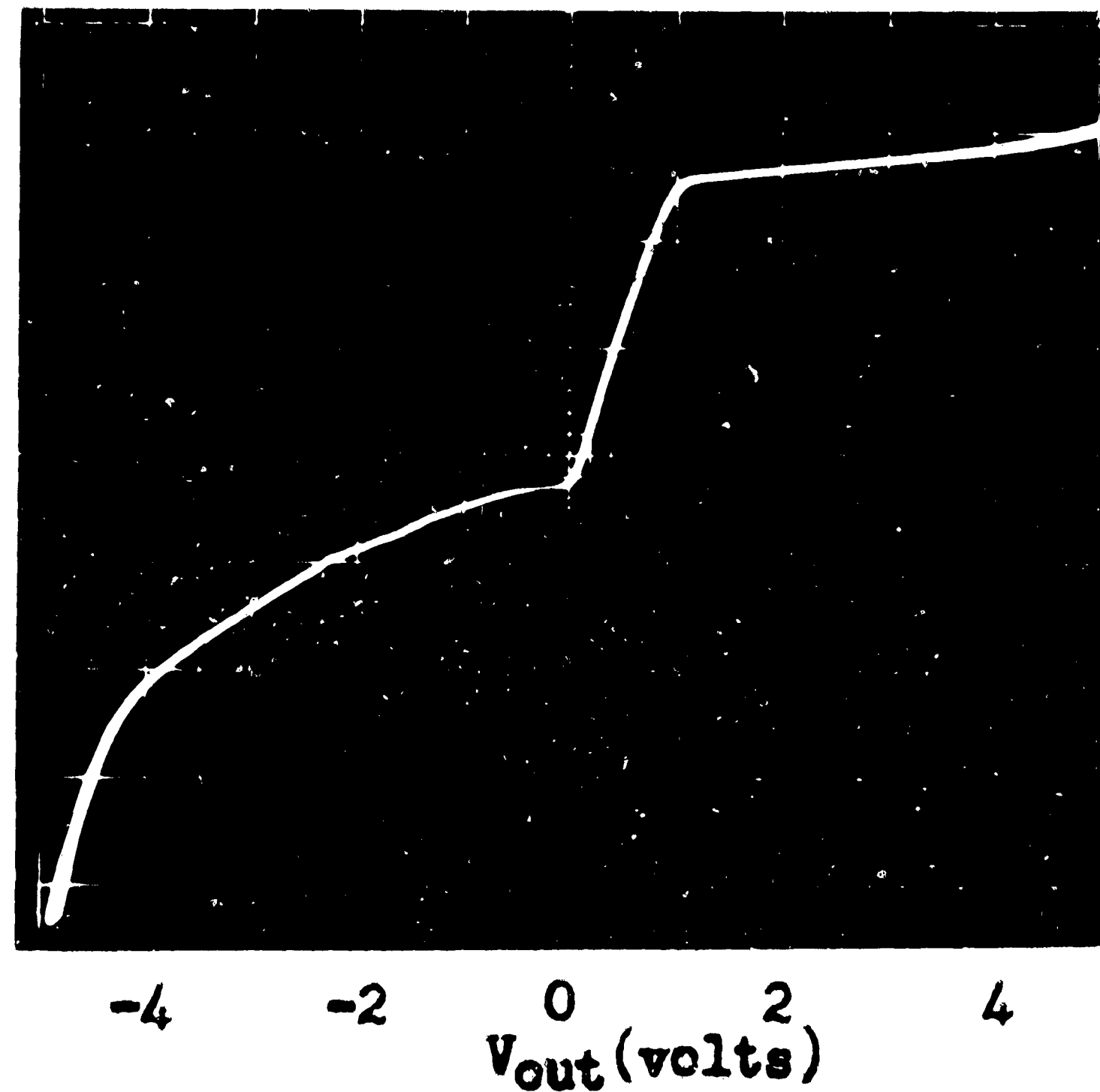


V_{out} vs. I_{out}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) $V_{cc} = 5 \text{ v.}$
- 3.) Pin #3 @ ground

$I_{out}(\text{Ma.})$

80
40
0
-40
-80

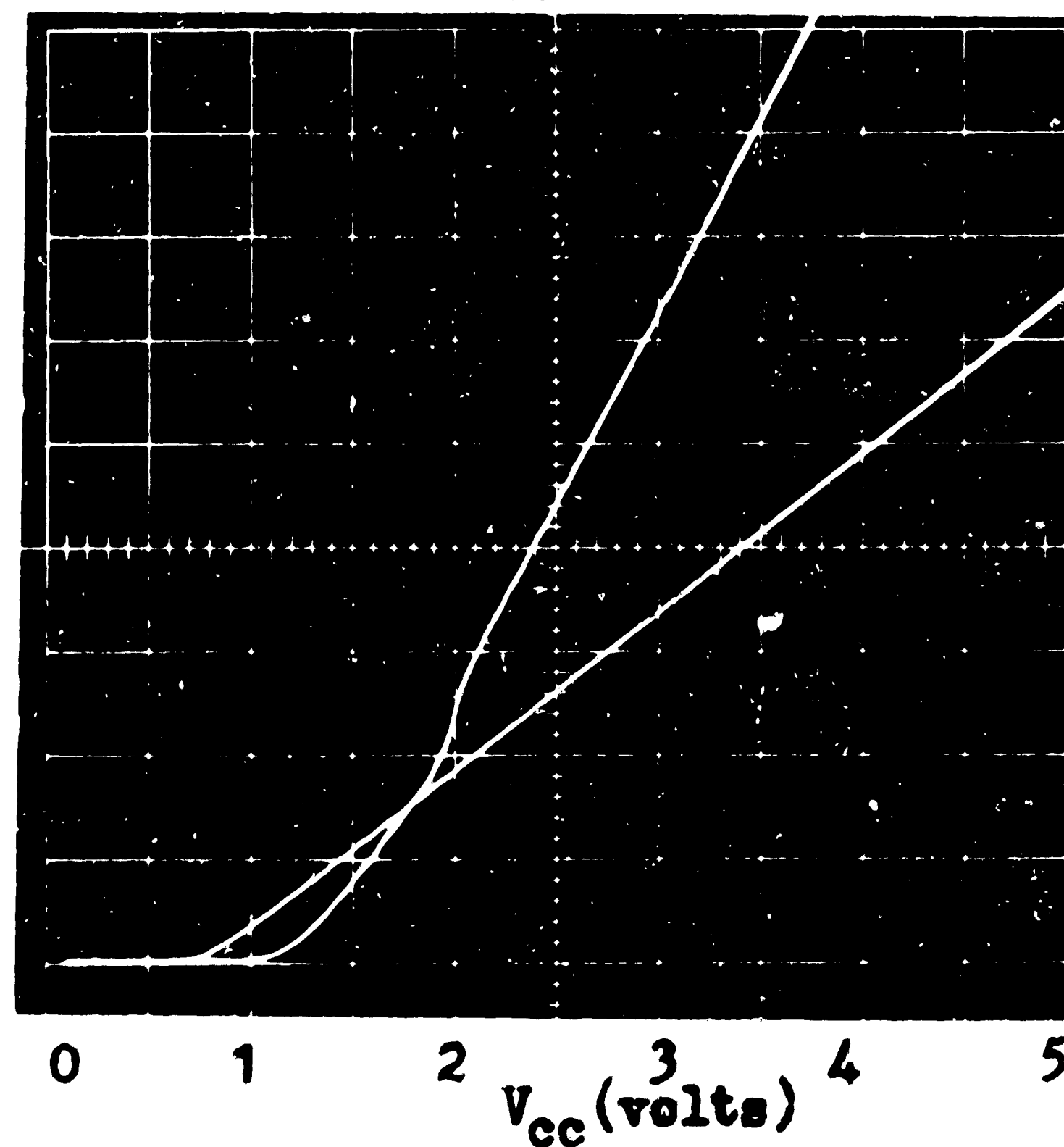


V_{cc} vs. I_{cc}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) Top trace with "1" in
- 3.) Bottom trace with "0" in.

$I_{cc}(\text{Ma.})$

1.6
1.2
.8
.4
0.0

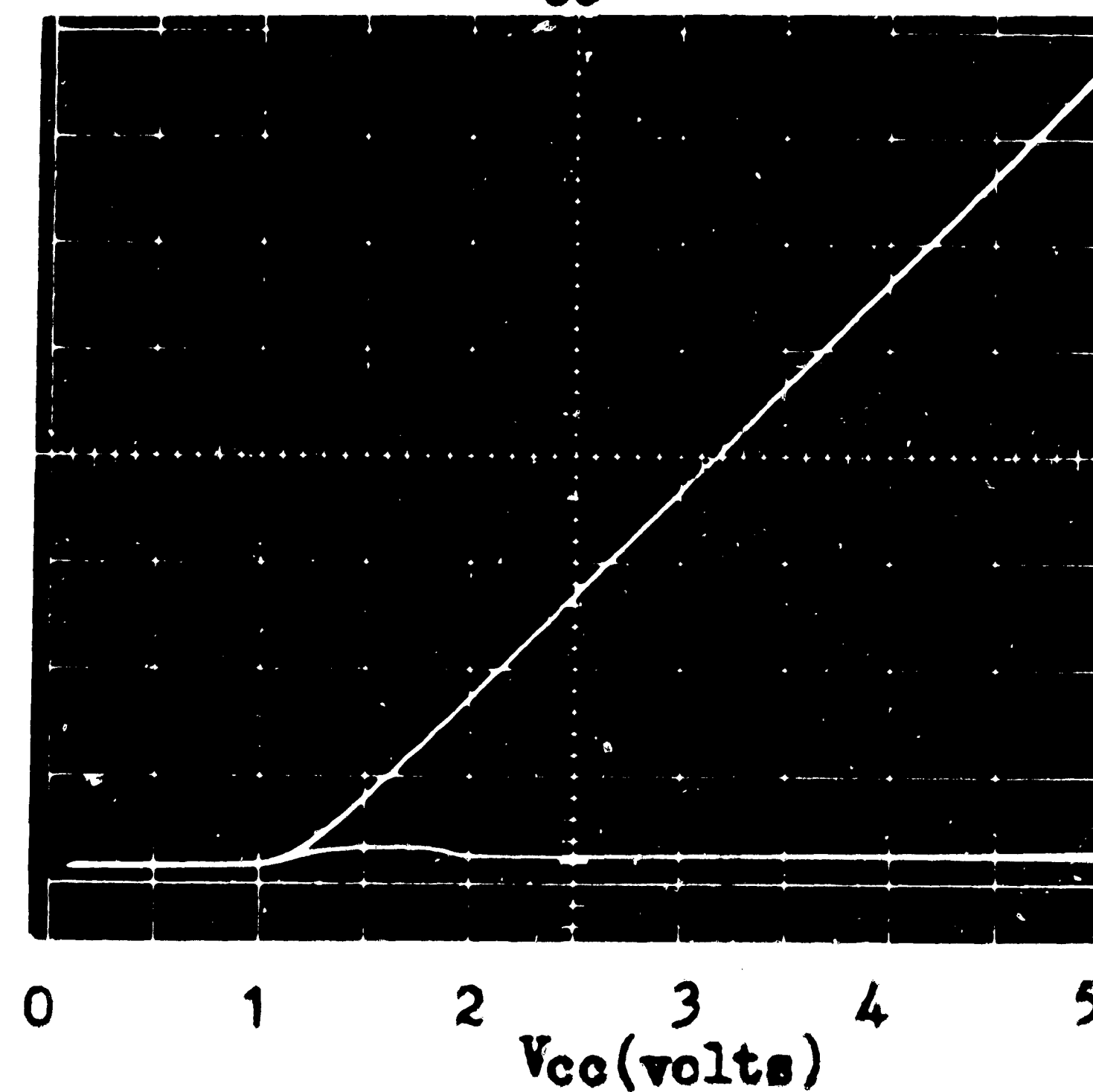


V_{cc} vs. V_{out}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) Top trace with "0" in
- 3.) Bottom trace with "1" in

$V_{out}(\text{volts})$

4
3
2
1
0



Circuit <u>510 5B</u>		Supply Voltage <u>4.5</u>				Frequency = <u>1 mc.</u>				Fan-in <u>1</u>			
Temperature:		-55°C				-40°C				+25°C			
Lead		1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})		2.8	2.8	2.9	2.5	2.8	2.8	2.9	2.6	2.9	3.0	3.4	2.9
Pulse Width (ns.)		200	192	200	186	200	195	200	191	200	200	200	200
T_r (ns.)		5.0	15	6.0	28	5.0	14	6.0	25	6.0	14	9.0	21
T_f (ns.)		8.0	11	8.0	34	7.0	10	7.0	31	5.0	9.0	5.0	16
T_d (ns.)			18		19		16		17		12		13
T_s (ns.)			10		9.0		10		9.0		10		9.0
T_{pd} (ns.)			16		21		15		19		13		16
Temperature:		+85°C				+125°C							
Lead		1	1	20	20	1	1	20	20				
Test Circuit		input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})		3.1	3.5	3.6	3.1	3.2	3.8	3.6	3.2				
Pulse Width (ns.)		200	206	200	207	200	212	200	212				
T_r (ns.)		10	17	13	21	13	20	17	25				
T_f (ns.)		4.5	8.0	5.0	13	5.0	8.0	6.0	13				
T_d (ns.)			11		11		10		11				
T_s (ns.)			11		11		12		14				
T_{pd} (ns.)			13		15		14		16				

Circuit <u>SMG 5B</u>		Supply Voltage <u>5.0</u>		Frequency = <u>1 mc.</u> Fan-in <u>1</u>												
Temperature:		-55°C					-40°C					+25°C				
Load		1	1	20	20	1	1	1	20	20	1	1	1	20	20	
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output	input	output	
Pulse Amplitude (V_{pp})		3.2	3.2	3.4	3.0	3.2	3.3	3.6	3.0	3.6	3.0	3.4	3.6	3.9	3.3	
Pulse Width (ns.)		200	197	200	195	200	199	200	198	200	198	200	203	200	204	
T_r (ns.)		5.0	14	7.0	28	5.0	13	7.0	26	7.5	13.5	11			21	
T_f (ns.)		7.0	10	7.0	33	6.0	9.0	6.0	29	4.5	7.0	4.0			14	
T_d (ns.)			13		15		12		14		10				11	
T_s (ns.)			10		10		10		9.0		9.5				9.0	
T_{pd} (ns.)			14		13		13		17		12				14.5	
Temperature:		+85°C					+125°C									
Load		1	1	20	20	1	1	1	20	20	1	1	1	20		
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output	input	output	
Pulse Amplitude (V_{pp})		3.6	4.1	4.2	3.6	3.7	4.3	4.2	3.7	4.2	3.7					
Pulse Width (ns.)		200	210	200	210	200	214	200	216	200	216					
T_r (ns.)		11	17	16	22	15	20	19	26							
T_f (ns.)		4.0	7.0	5.0	12	4.0	7.0	6.0	12							
T_d (ns)			10		10		9.0		10							
T_s (ns.)			11		12		13		15							
T_{pd} (ns.)			12.5		14		12.5		15							

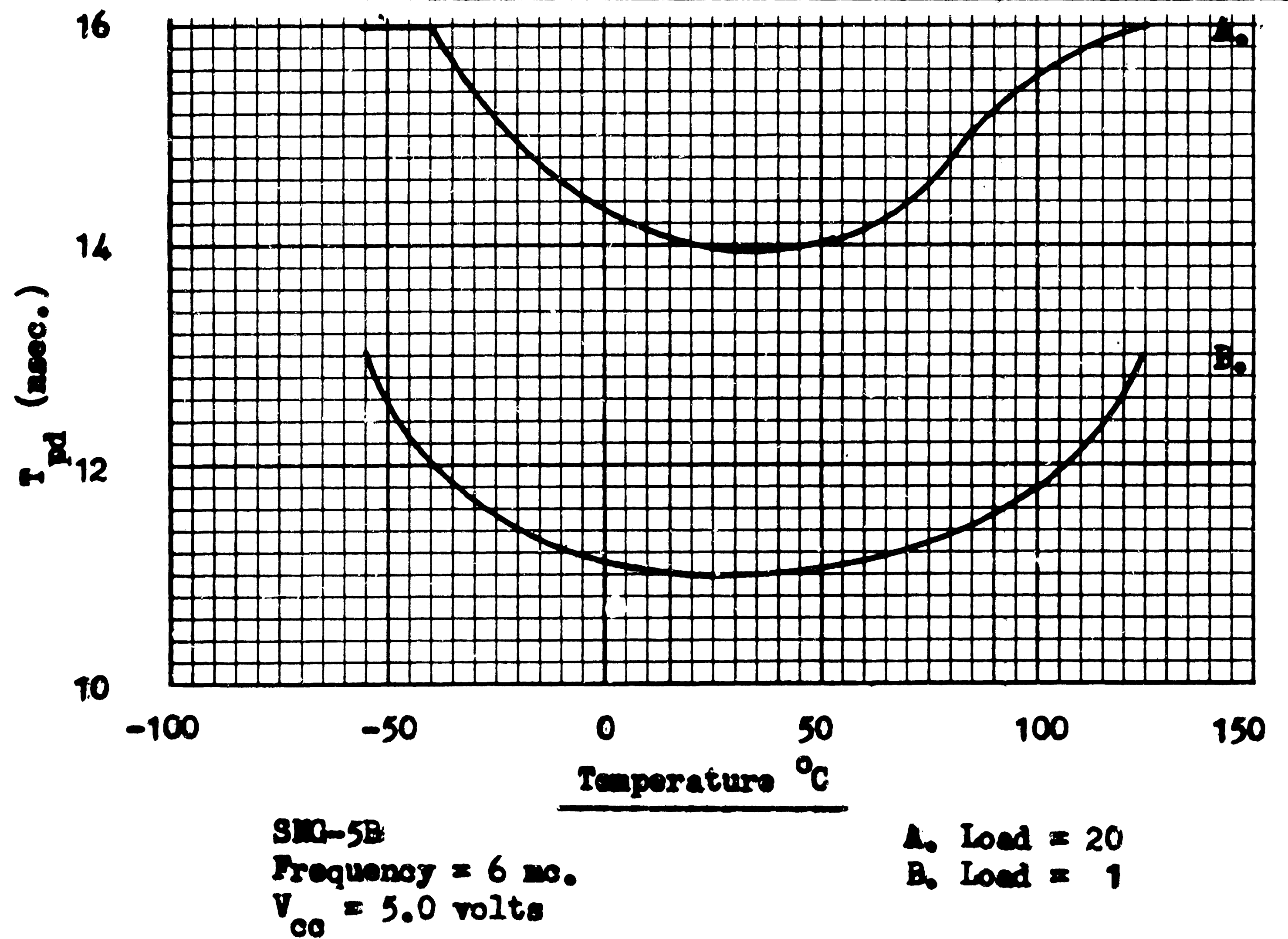
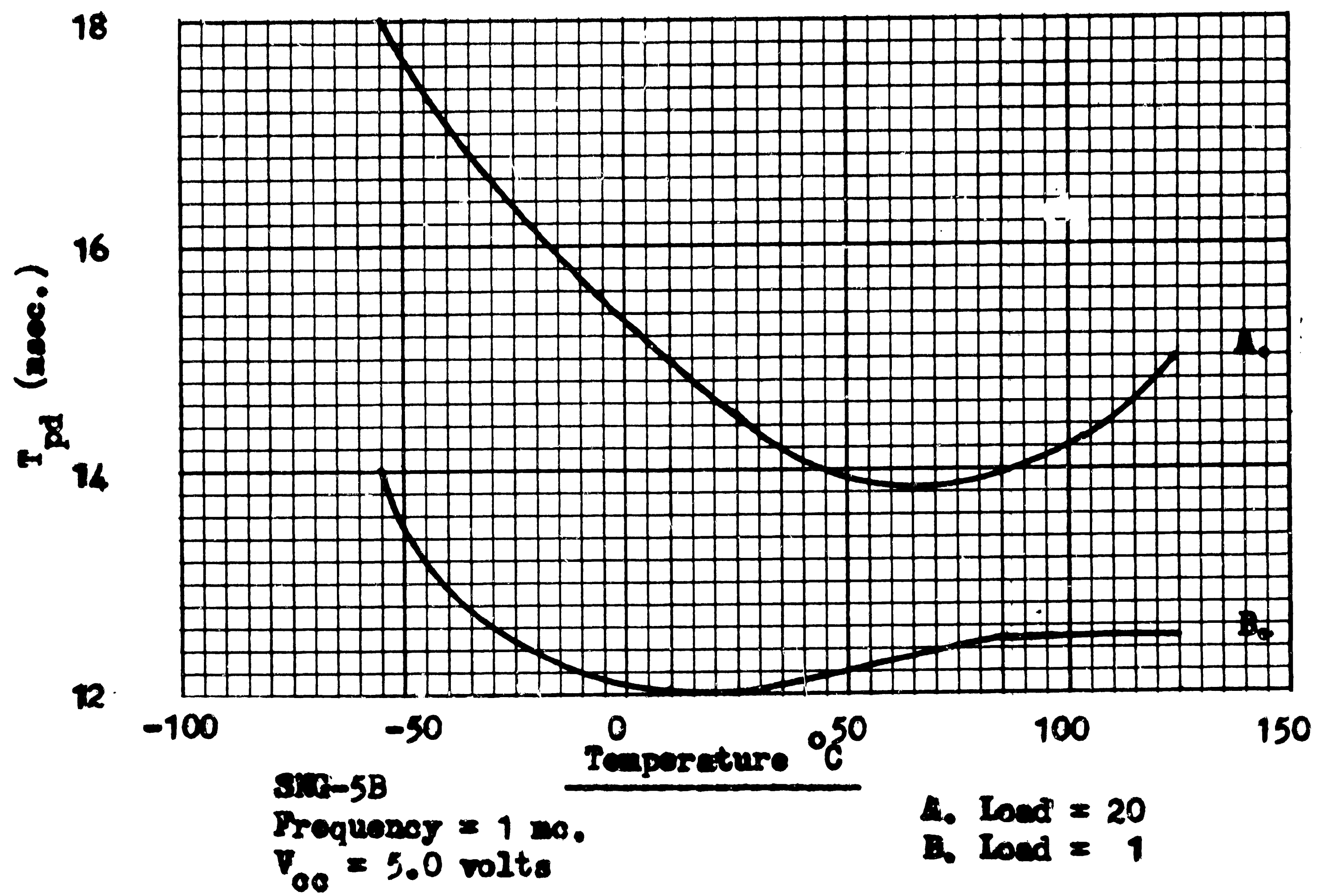
Circuit SMO 5B				Supply Voltage 5.5				Frequency = 1 Mc.				Fan-in 1			
Temperature:				-55°C				-40°C				+25°C			
Load		1	20	1	20	1	20	1	20	1	20	1	20		
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output	output	
Pulse Amplitude (V_{pp})		3.6	3.7	4.0	3.4	3.7	3.8	4.2	3.5	3.8	4.1	4.4	3.7		
Pulse Width (ns.)		200	201	200	199	200	204	200	201	200	205	200	206		
T_r (ns.)		6.0	14	7.0	27	6.0	13	9.0	25	8.0	14	12	21		
T_f (ns.)		6.0	9.0	6.0	32	5.0	8.0	5.0	27	4.0	7.0	5.0	13		
T_d (ns.)			12		13		10		12		9.0		10		
T_s (ns.)			10		9.0		10		8.0		10		9.0		
T_{pd} (ns.)			13		17		12		16		11		14		
Temperature:				+85°C				+125°C							
Load		1	20	1	20	1	20	1	20	1	20				
Test Circuit		input	output	input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})		4.1	4.6	4.7	4.0	4.2	4.8	4.6	4.1						
Pulse Width (ns.)		200	211	200	212	200	217	200	219						
T_r (ns.)		13	17	17	23	16	21	19	27						
T_f (ns.)		5.0	7.0	5.0	12	4.0	7.0	6.0	12						
T_d (ns.)			9.0		9.0		9.0		9.0						
T_s (ns.)			11		13		13		15						
T_{pd} (ns.)			12		14		13		15						

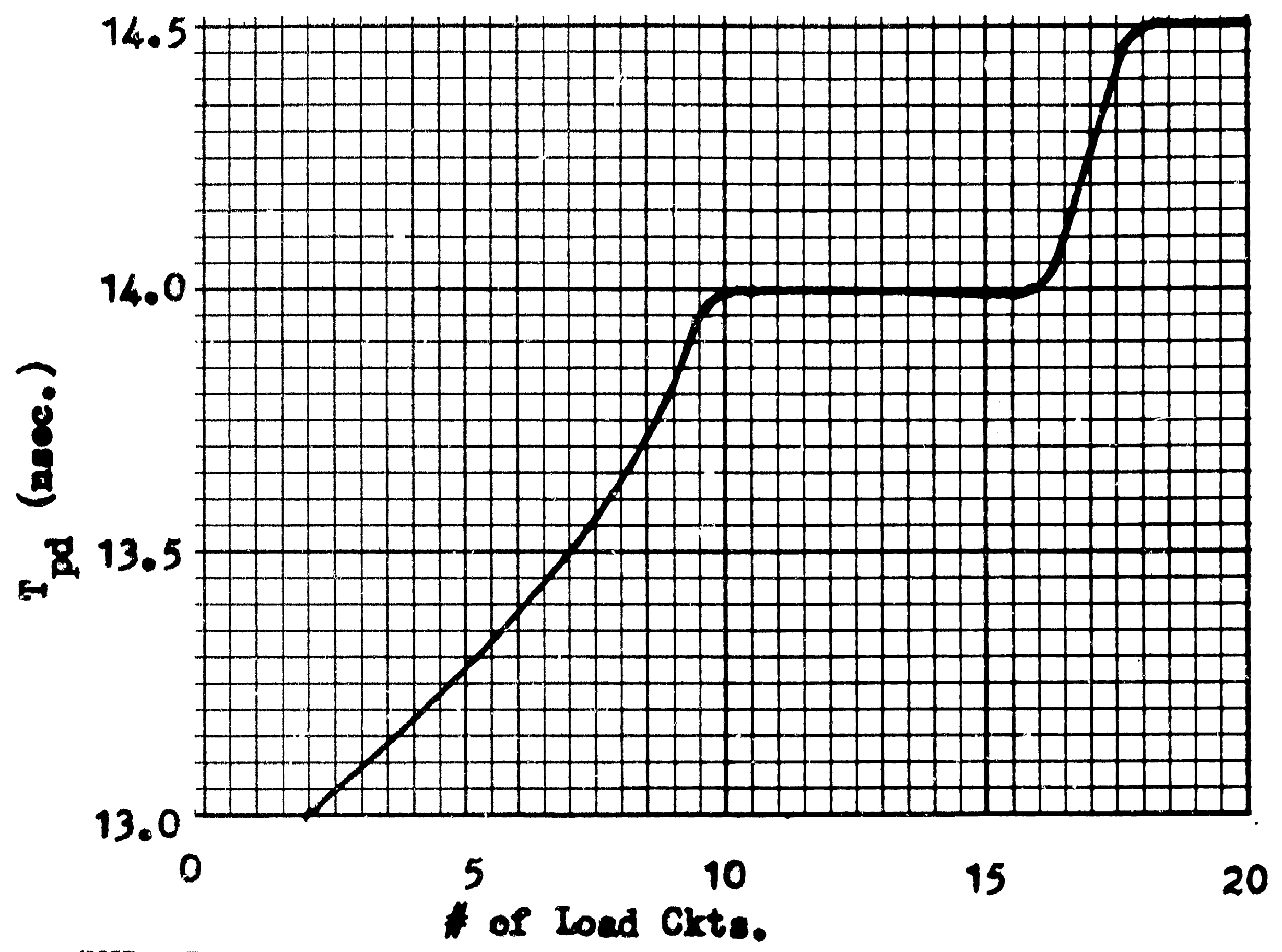
Circuit SNG 5 Supply Voltage 5.0 Frequency = 6 ms. Fan-in 1																
Temperature:		-55°C						-40°C						+25°C		
Load		1	1	20	20	20	1	1	20	20	20	1	1	20	20	20
Test Circuit		input	output	input	input	output	input	output	input	input	output	input	output	input	input	output
Pulse Amplitude (V _{pp})		3.3	3.3	3.6	3.1	3.1	3.3	3.4	3.8	3.1	3.1	3.5	3.8	4.2	3.4	3.4
Pulse Width (ns.)		50	49	50	47	47	50	50	50	49	49	50	54	50	55	55
T _r (ns.)		5.0	14	7.0	29	29	5.0	13	8.0	27	27	8.0	15	37	23	23
T _f (ns.)		5.0	9.0	6.0	34	34	5.0	8.0	5.0	30	30	4.0	7.0	5.0	13	13
T _d (ns.)			12		13	13		11		12	12		10		10	10
T _s (ns.)			9.0		8.0	8.0		9.0		47	47		9.0		10	10
T _{pd} (ns.)			13		16	16		12		16	16		11		14	14
Temperature:		+85°C						+125°C								
Load		1	1	20	20	20	1	1	20	20	20	1	1	20	20	20
Test Circuit		input	output	input	input	output	input	output	input	input	output	input	output	input	input	output
Pulse Amplitude (V _{pp})		3.7	4.4	4.5	4.0	4.0	3.7	4.6	4.5	4.1	4.1					
Pulse Width (ns.)		50	60	50	61	61	50	65	50	68	68					
T _r (ns.)		11	19	39	27	27	15	23	40	31	31					
T _f (ns.)		4.0	7.0	4.0	14	14	4.0	7.0	4.0	13	13					
T _d (ns)			9.0		10	10		9.0		9.0	9.0					
T _s (ns.)			11		11	11		13		13	13					
T _{pd} (ns.)			12		15	15		13		16	16					

SNG 5B $V_{cc} = 5.0$ v. Frequency = 1 mc. Input P.Width = 200 nsec.

Load ckt.s.	20	18	16	14	12	10	8	6	4	2
T_{pd}	14.5	14.5	14.0	14.0	14.0	14.0	13.5	13.5	13.1	13.0
T_r Output	21.0	20.5	19.8	18.5	17.6	17.3	16.4	15.9	15.2	15.0
T_f Output	14.0	13.4	12.5	11.8	11.4	10.5	10.0	9.6	8.8	8.5
Pulse Amp. (Input)	3.82	3.76	3.72	3.60	3.56	3.52	3.44	3.36	3.31	3.24
Pulse Amp. (Output)	3.28	3.32	3.32	3.34	3.36	3.40	3.41	3.44	3.50	3.54

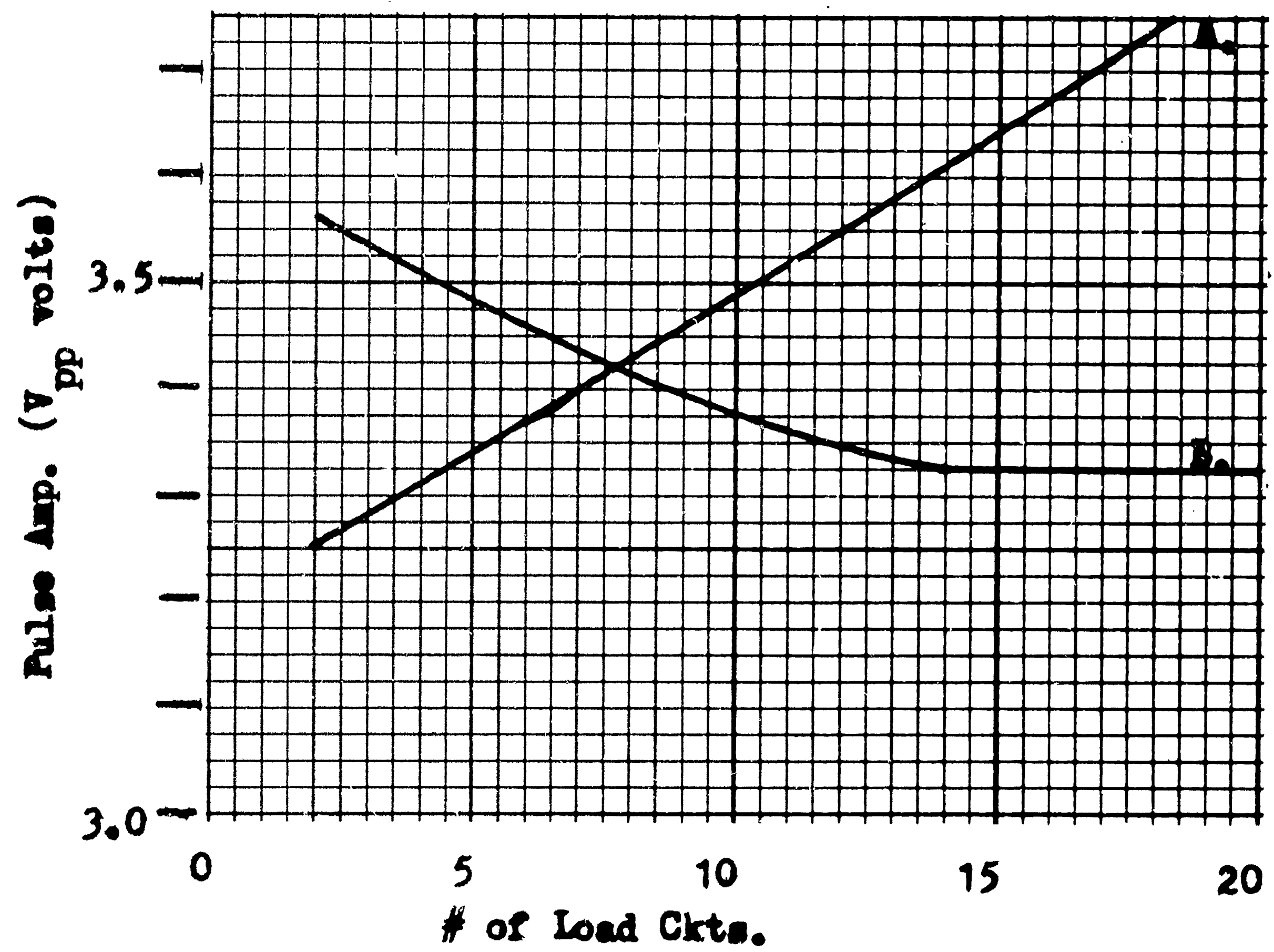
Temperature = 25°C.





SNG-5B
Frequency = 1 mc.

$V_{cc} = 5.0$ volts
 $T = 25^\circ \text{C.}$



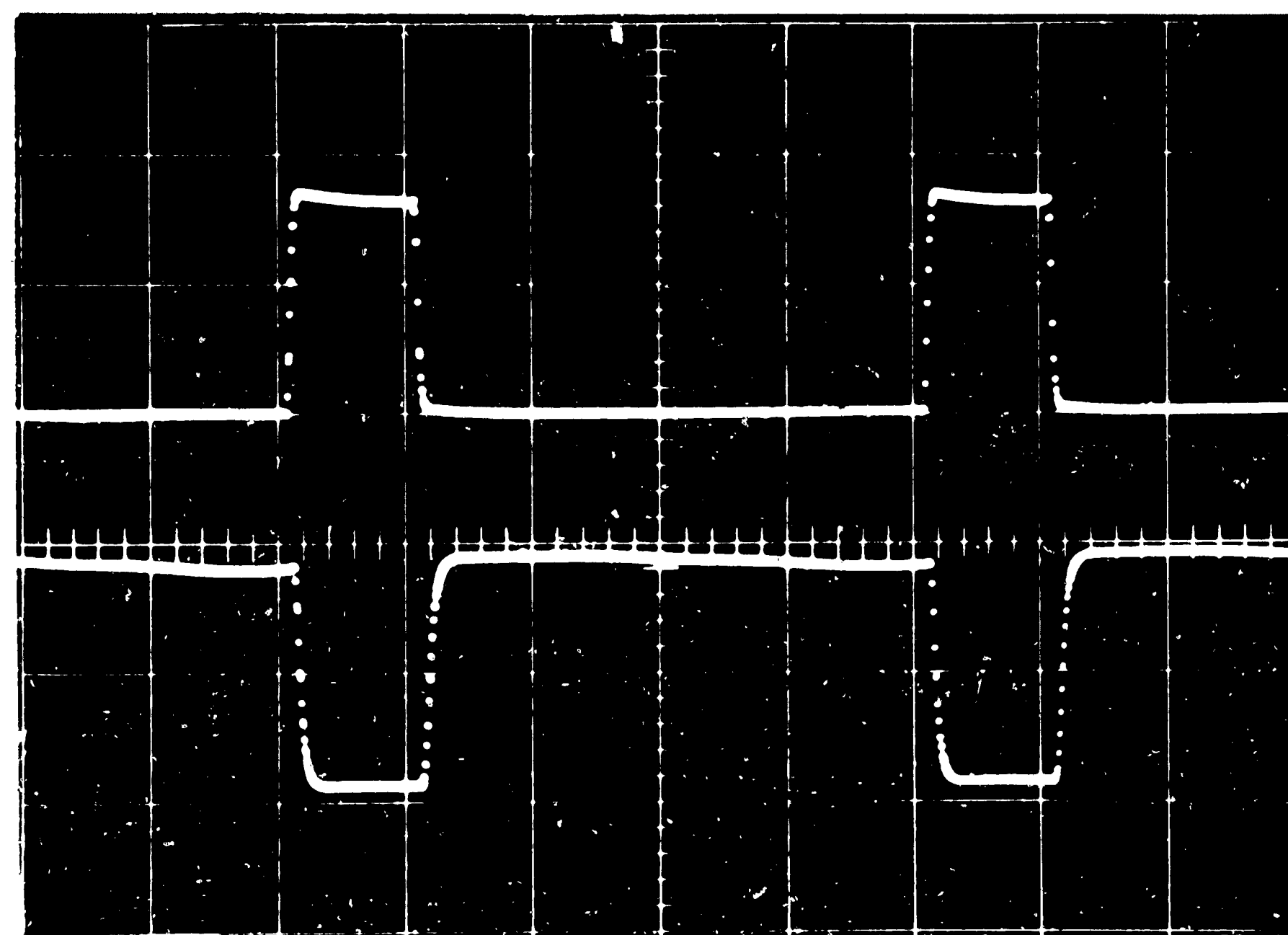
SNG-5B
Frequency = 1 mc.
 $V_{cc} = 5.0$ volts

A. Input Pulse Amp.
B. Output Pulse Amp.

SNG-5B
 Frequency = 1 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C.

2 v./div.

IN
 OUT

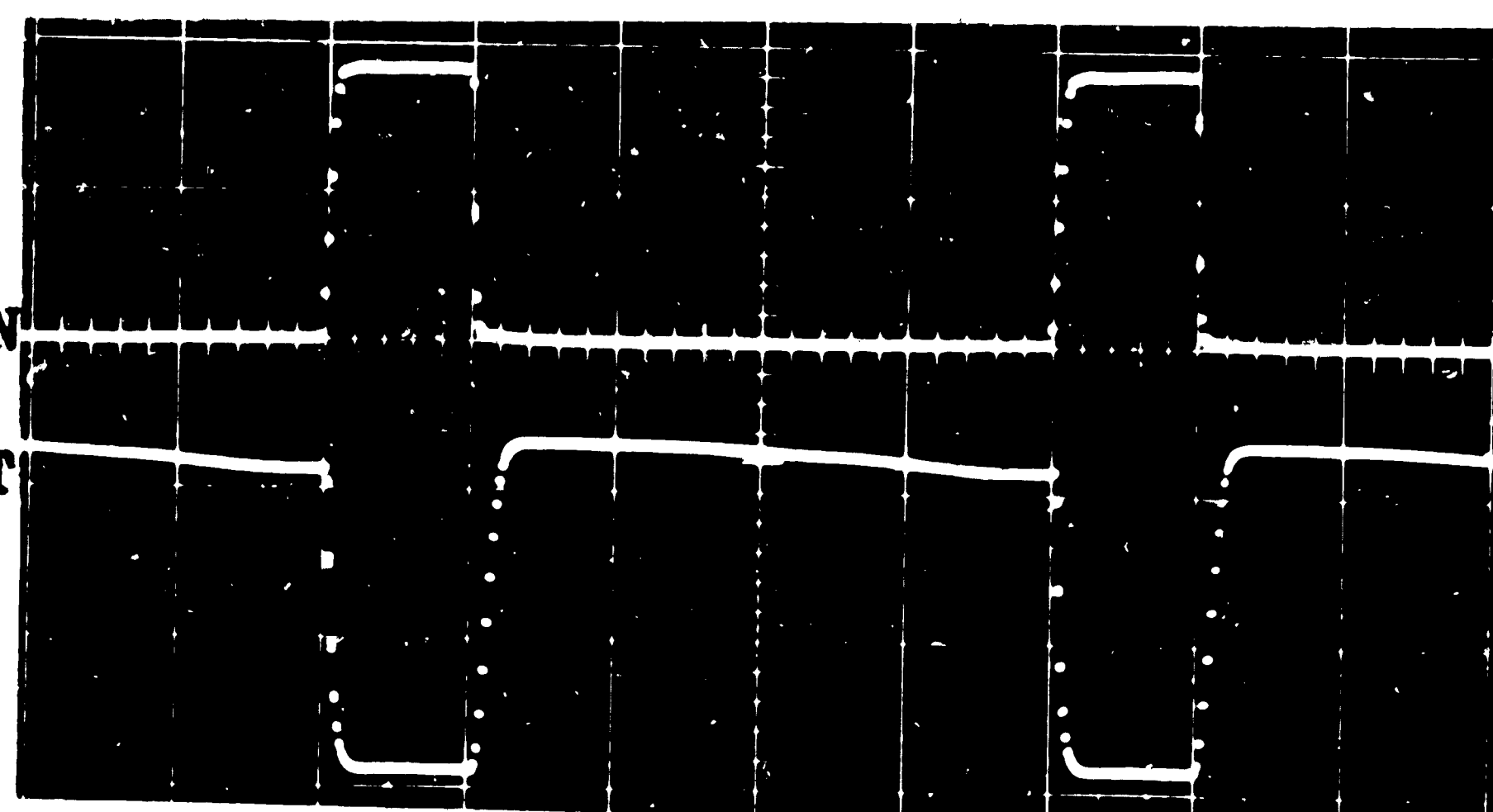


0.2 μsec./div.

SNG-5B
 Frequency = 1 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 125°C.

2 v./div.

IN
 OUT

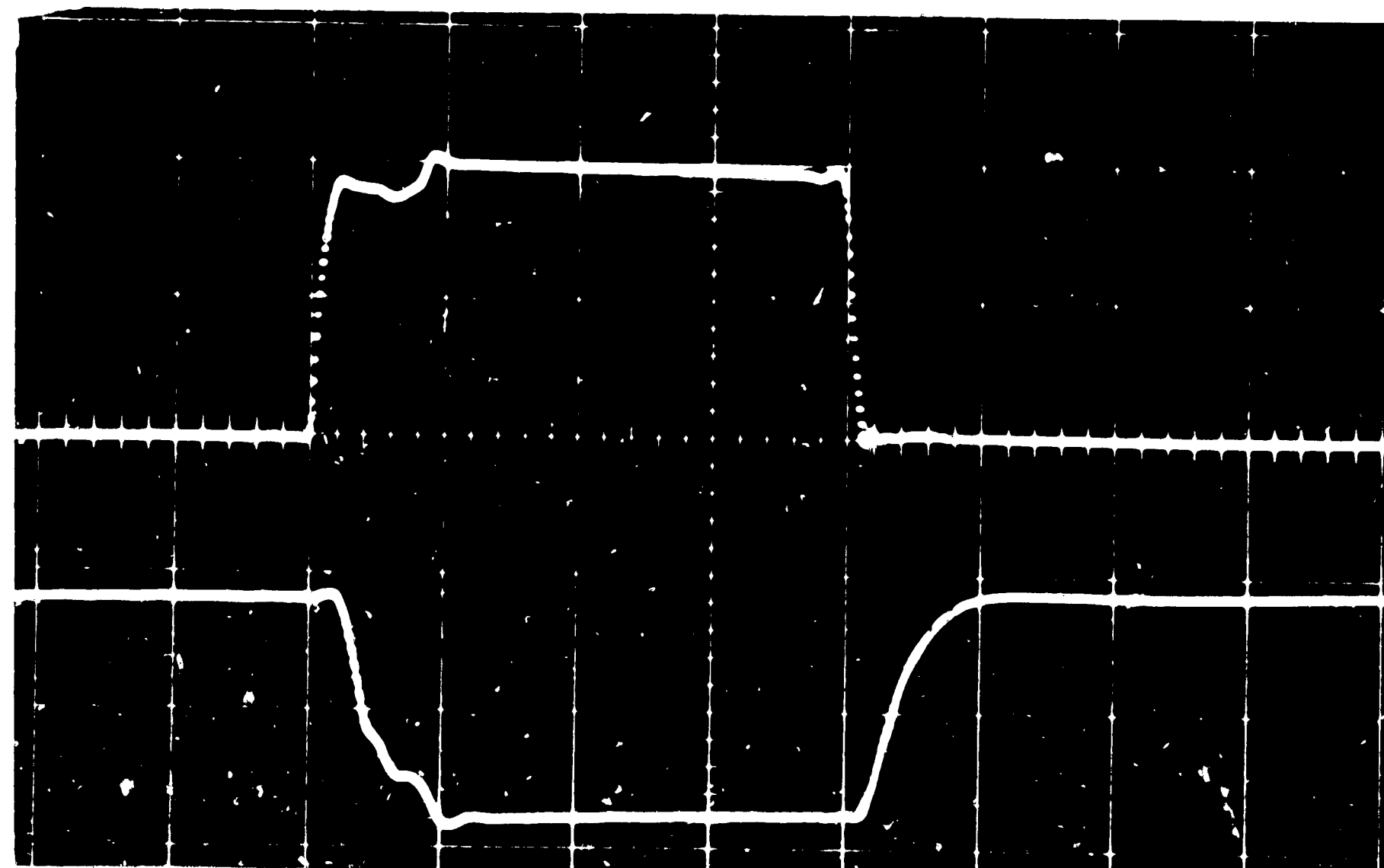


0.2 μsec./div.

SNG-5B
 Frequency = 1 mc.
 Load = 20 ckts.
 $V_{cc} = 5.0$ volts
 Temperature = -55°C.

2 v./div.

IN
 OUT

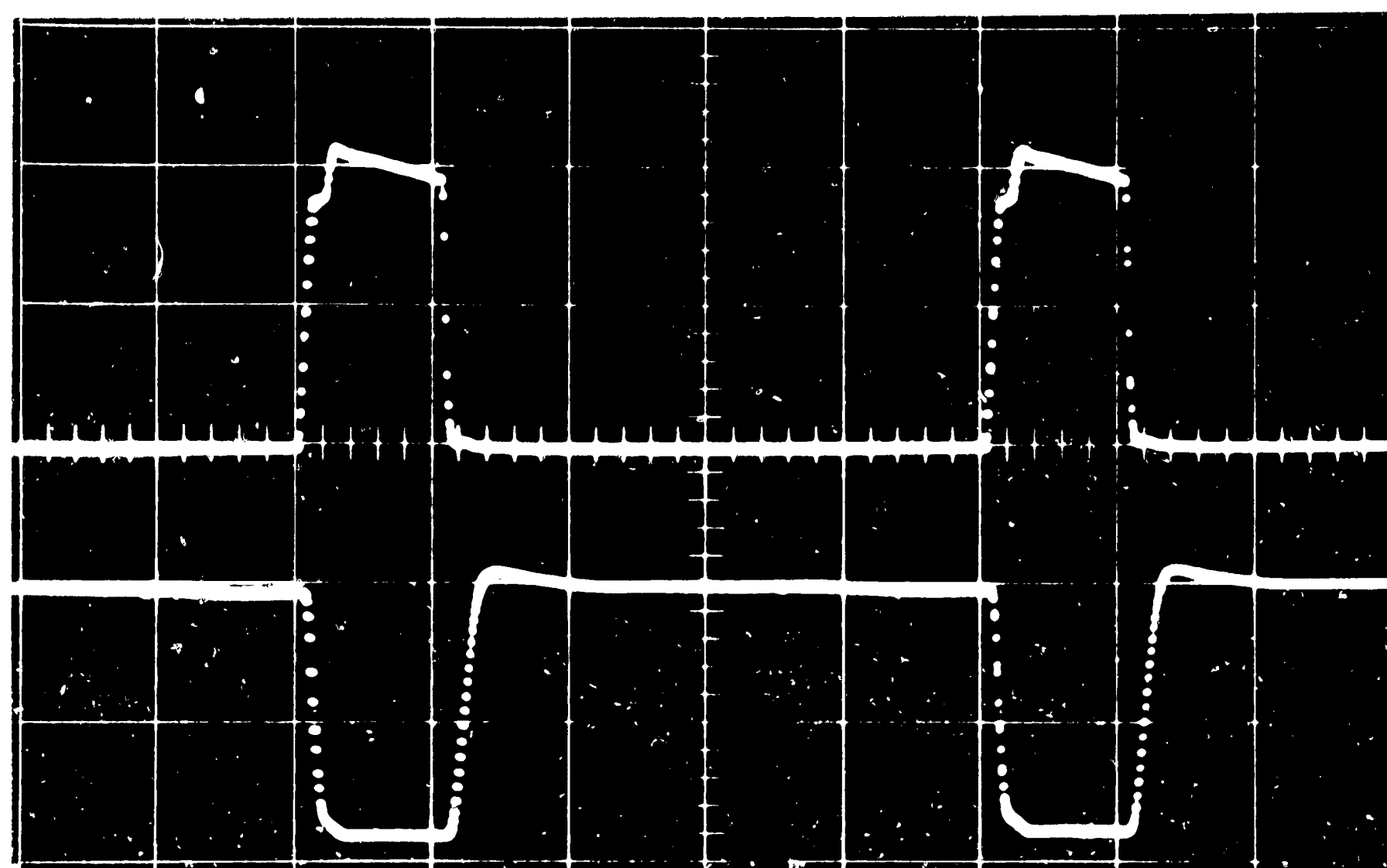


50 nsec./div.

SNG-5B
 Frequency = 1 mc.
 Load = 20 ckts.
 $V_{cc} = 5.0$ volts
 Temperature = 125°C

2 v./div.

IN
 OUT

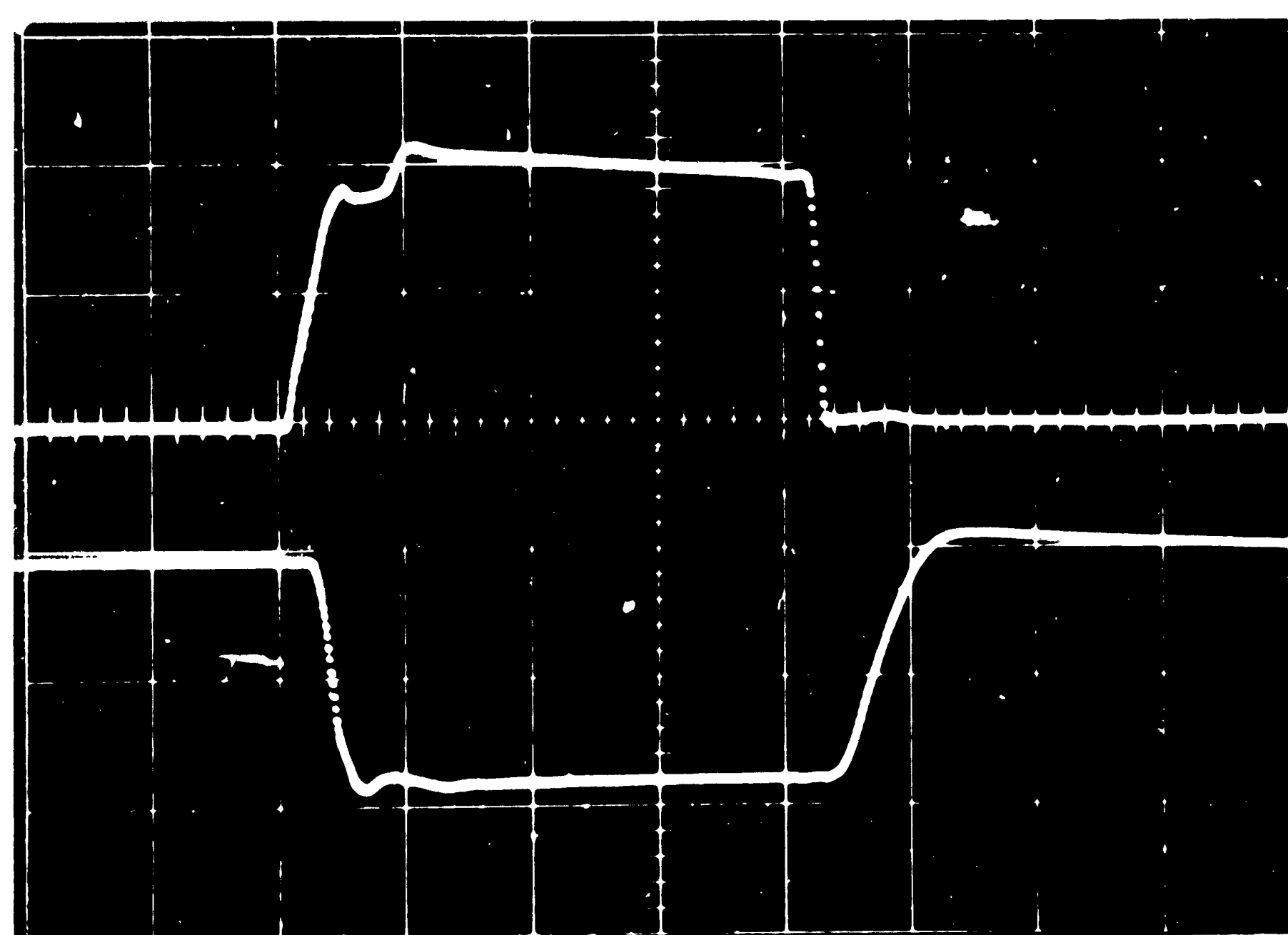


.2 μsec./div.

SNG-5B
 Same as above except
 50 nsec./div.

2 v./div.

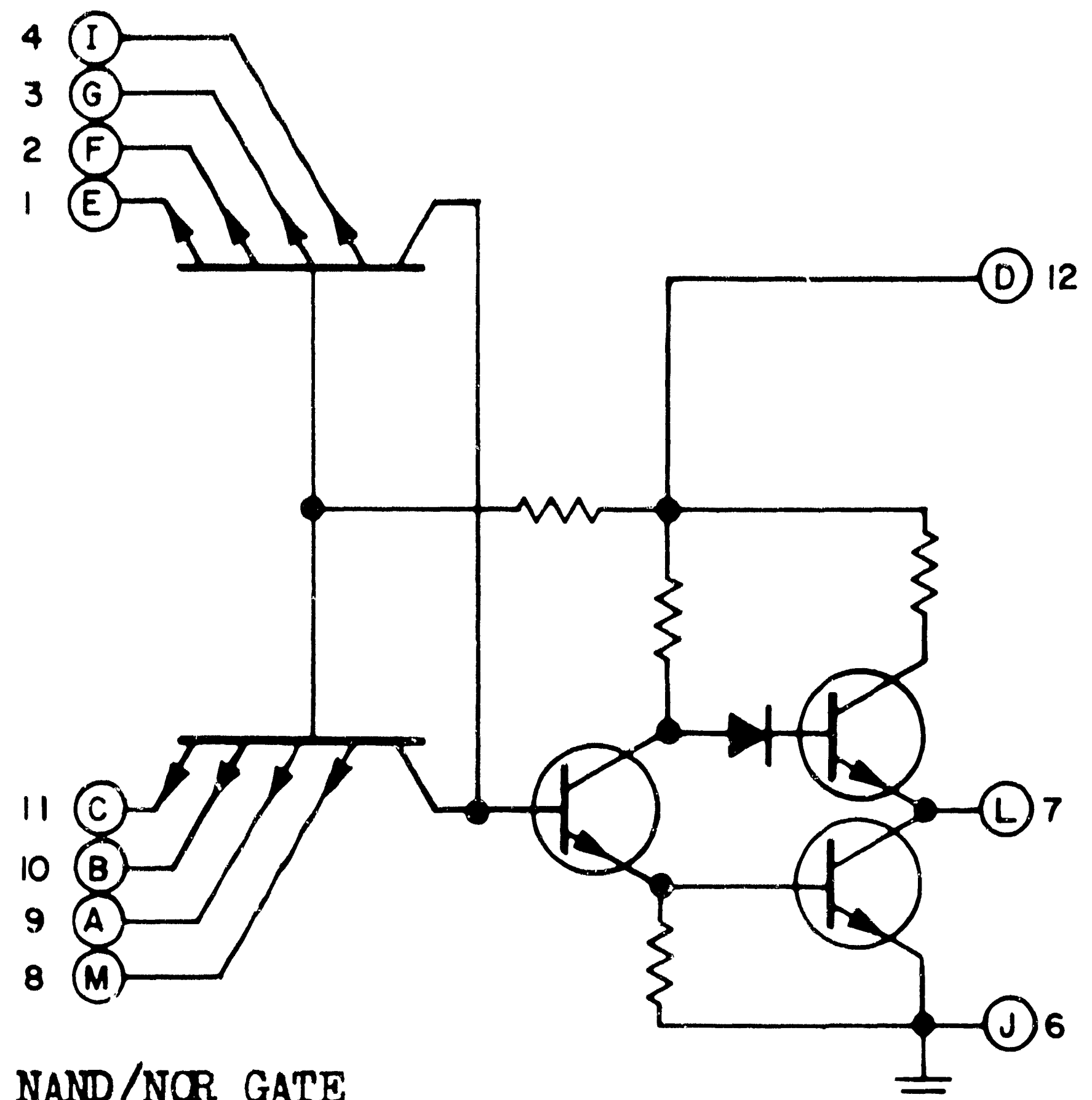
IN
 OUT



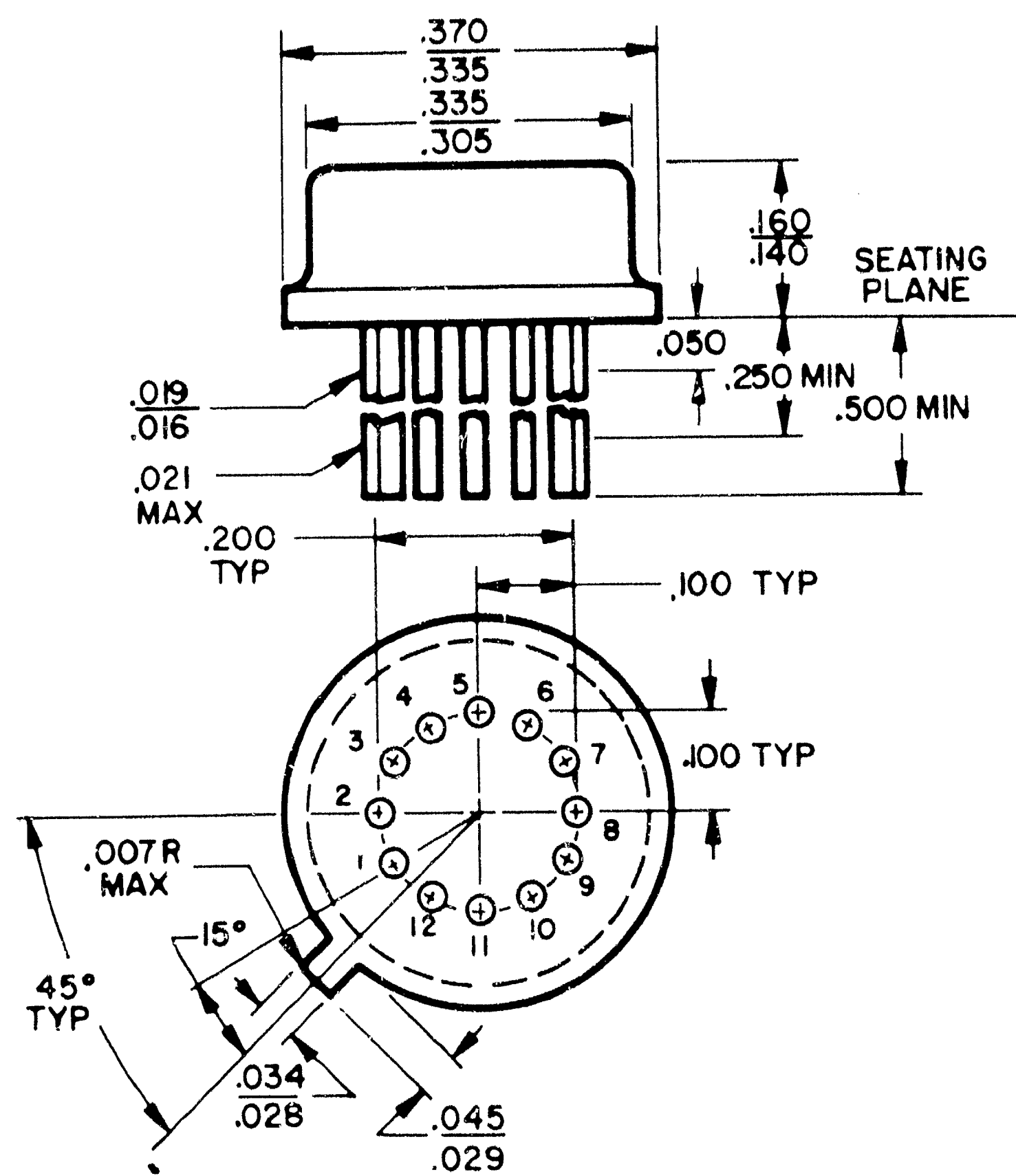
50 nsec./div.

SNG 6A & B
 (+) LOGIC
 $L = A \cdot B \cdot C \cdot M \cdot E \cdot F \cdot G \cdot I$
 (-) LOGIC
 $L = \overline{A+B+C+M+E+F+G+I}$

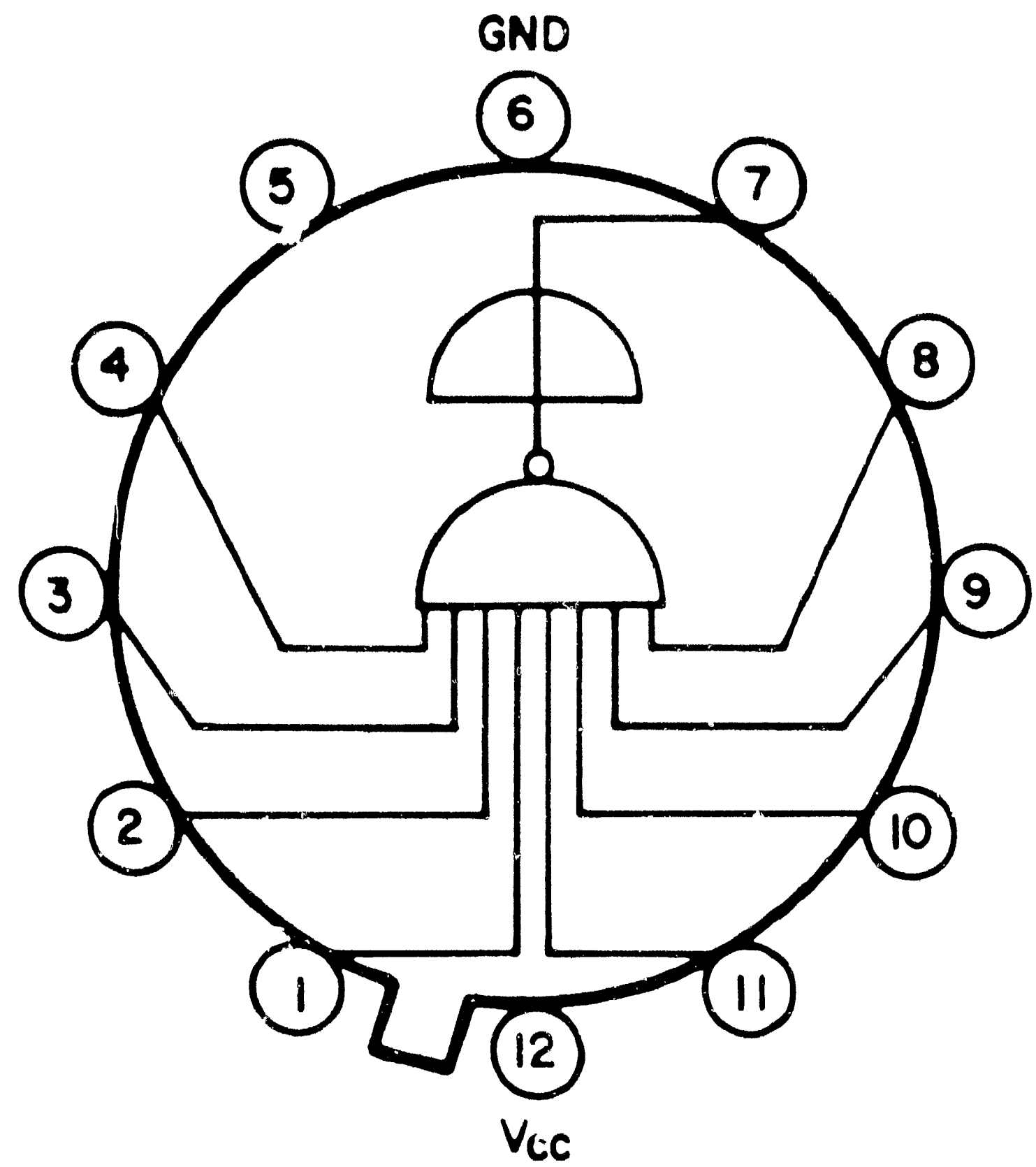
HIGH FAN-IN NAND/NOR GATE



The SNG-6 circuit is of the planar, epitaxial, and monolithic type and requires only one power supply. The "A" version consists of a single six input AND gate and the "B" version consists of a single eight input AND gate. Both of these circuits are followed by a cascaded amplifier inverting stage.



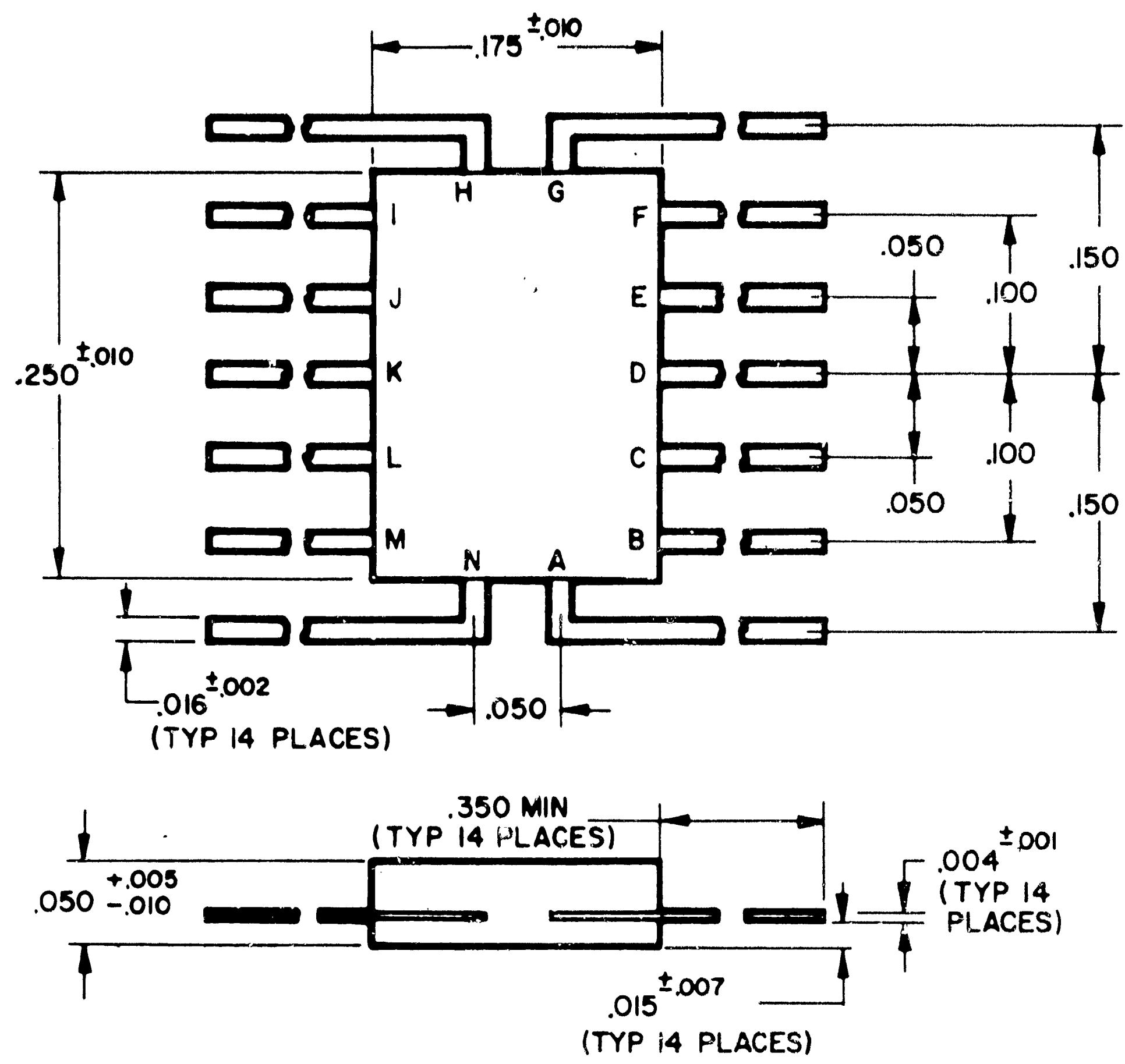
12 LEAD TO-5



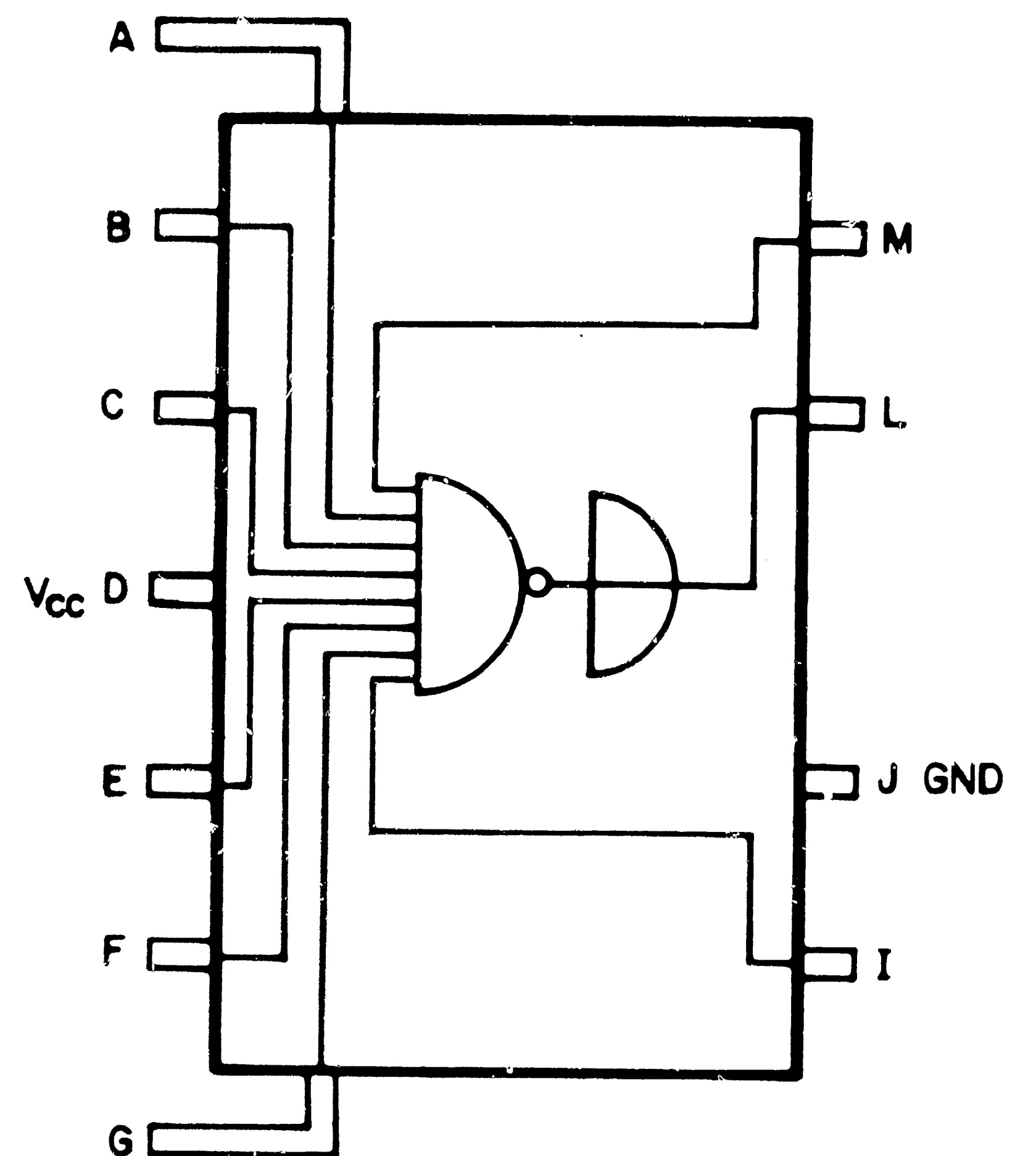
BOTTOM VIEW

SNG-6B

FOR SNG-6A INPUTS 9-A AND 3-G ARE NOT PRESENT



14 LEAD FLAT PACK



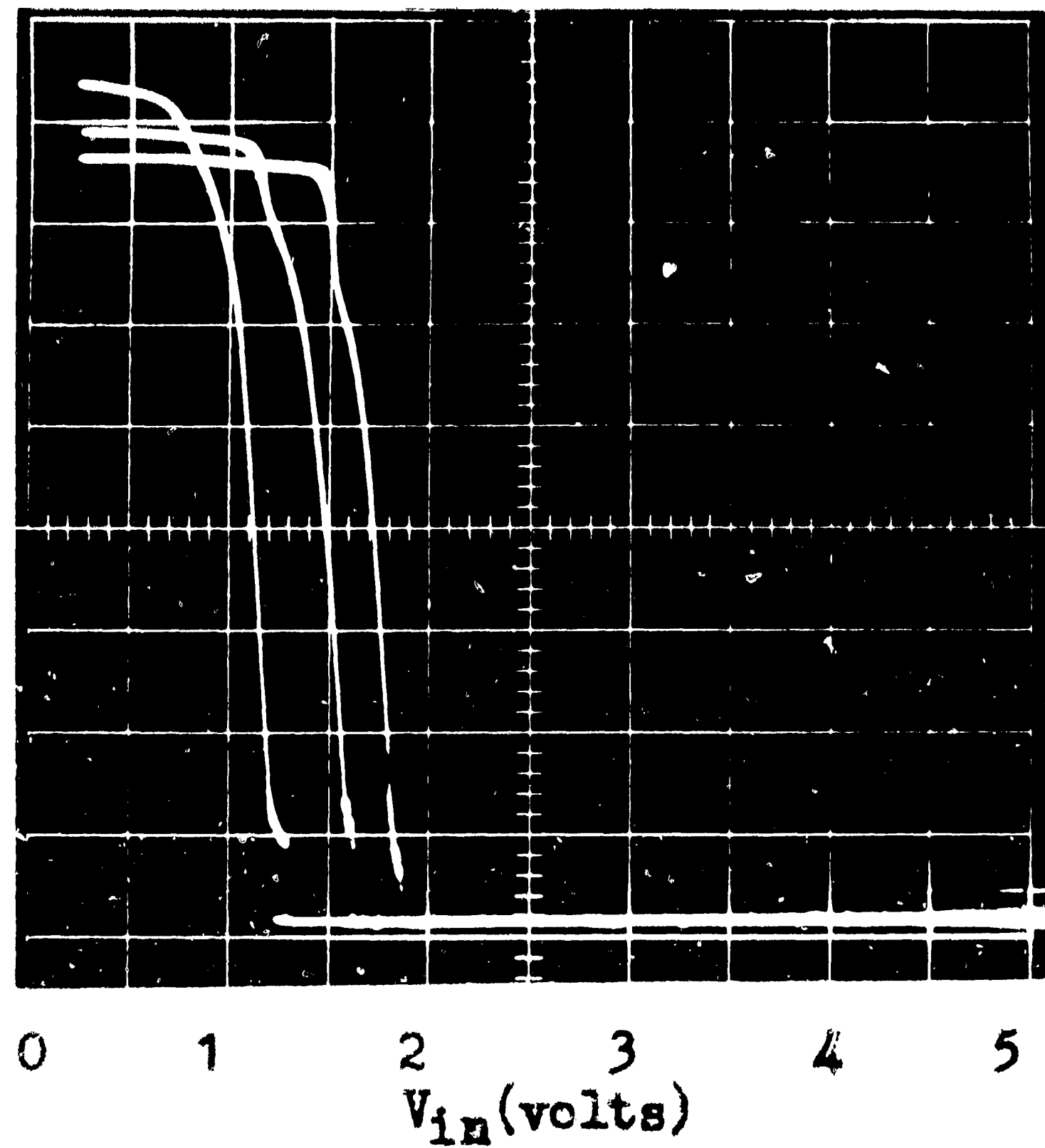
TOP VIEW

V_{in} vs. V_{out}

1.) $V_{cc} = 5 \text{ v.}$

+125°C
+25°C
-55°C

$V_{out}(\text{volts})$
4
3
2
1
0

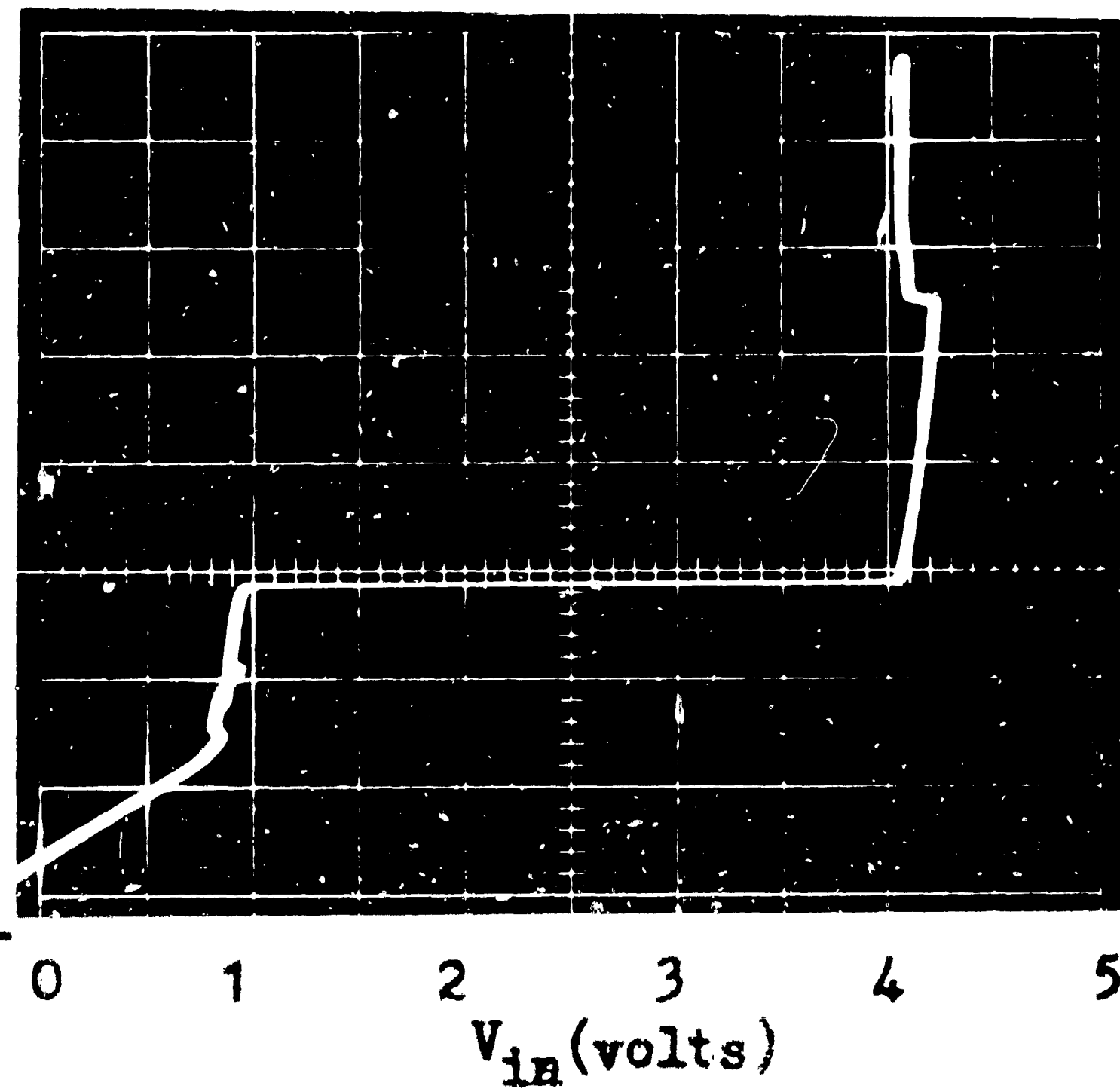


V_{in} vs. I_{in}

1.) $T = 25^\circ\text{C}$

2.) $V_{cc} = 5 \text{ v.}$

$I_{in}(\text{Ma.})$
2
1
0
-1



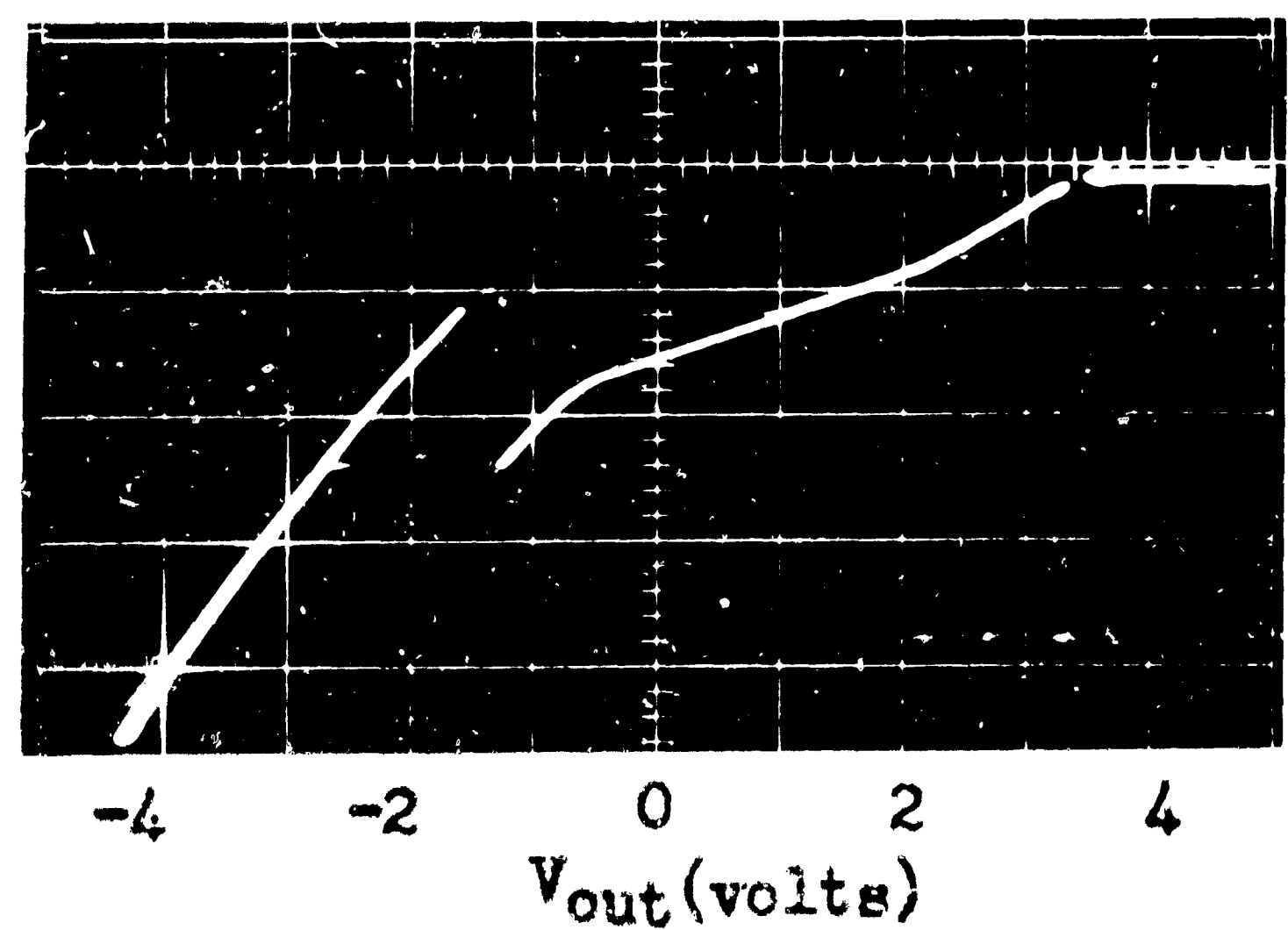
V_{out} vs. I_{out}

1.) $T = 25^\circ\text{C}$

2.) $V_{cc} = 5 \text{ v.}$

3.) Pin #10 @ ground.

$I_{out}(\text{Ma.})$
20
0
-40
-80



Normal operation

V_{out} vs. I_{out}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) $V_{cc} = 5 \text{ v.}$
- 3.) Pin #10 open.

$I_{out}(\text{Ma.})$

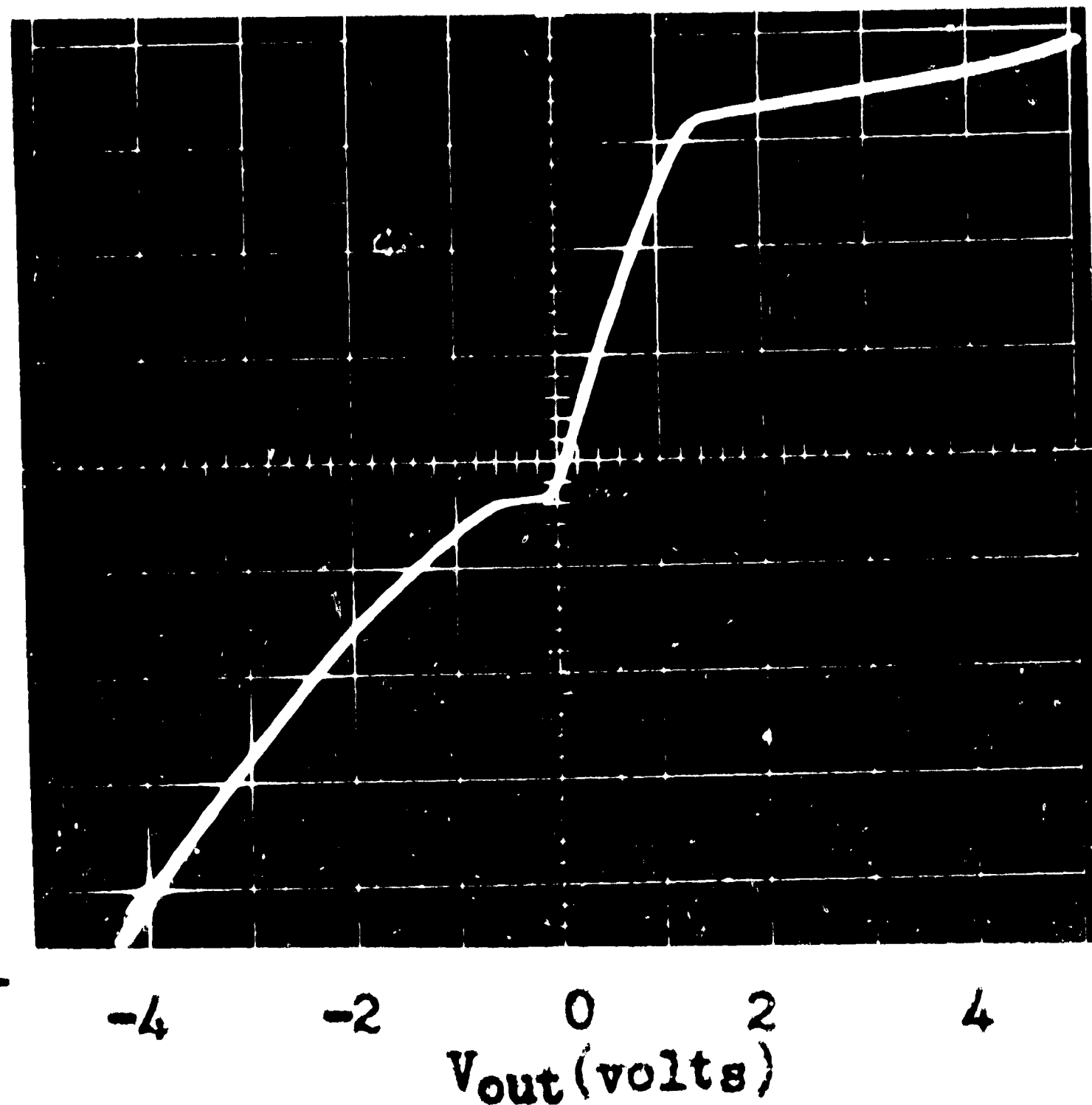
80

40

0

-40

-80



V_{cc} vs. I_{cc}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) Top trace with "1" in
- 3.) Bottom trace with "0" in.

$I_{cc}(\text{Ma.})$

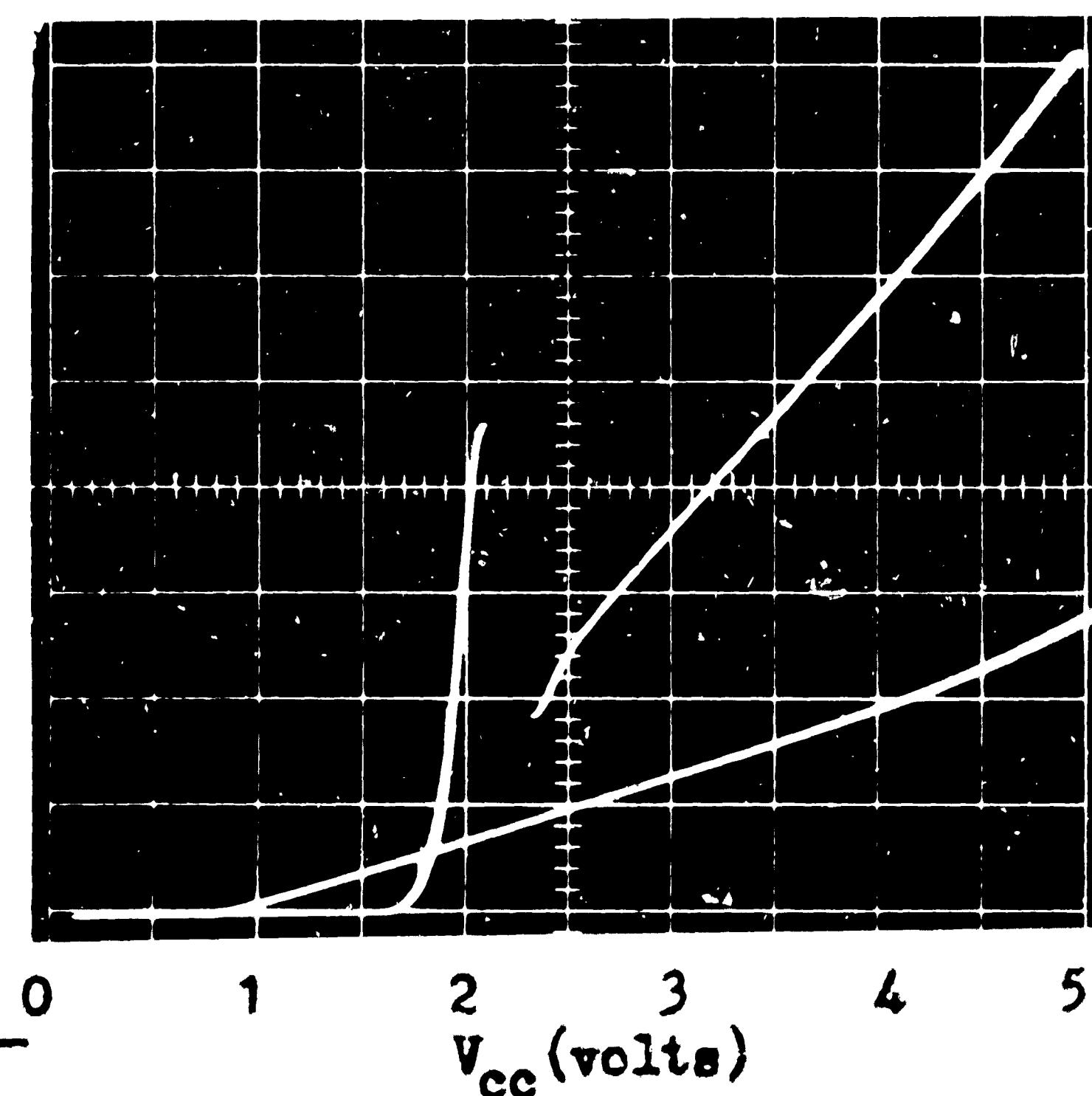
4

3

2

1

0



V_{cc} vs. V_{out}

- 1.) $T = 25^{\circ}\text{C}$

$V_{out}(\text{volts})$

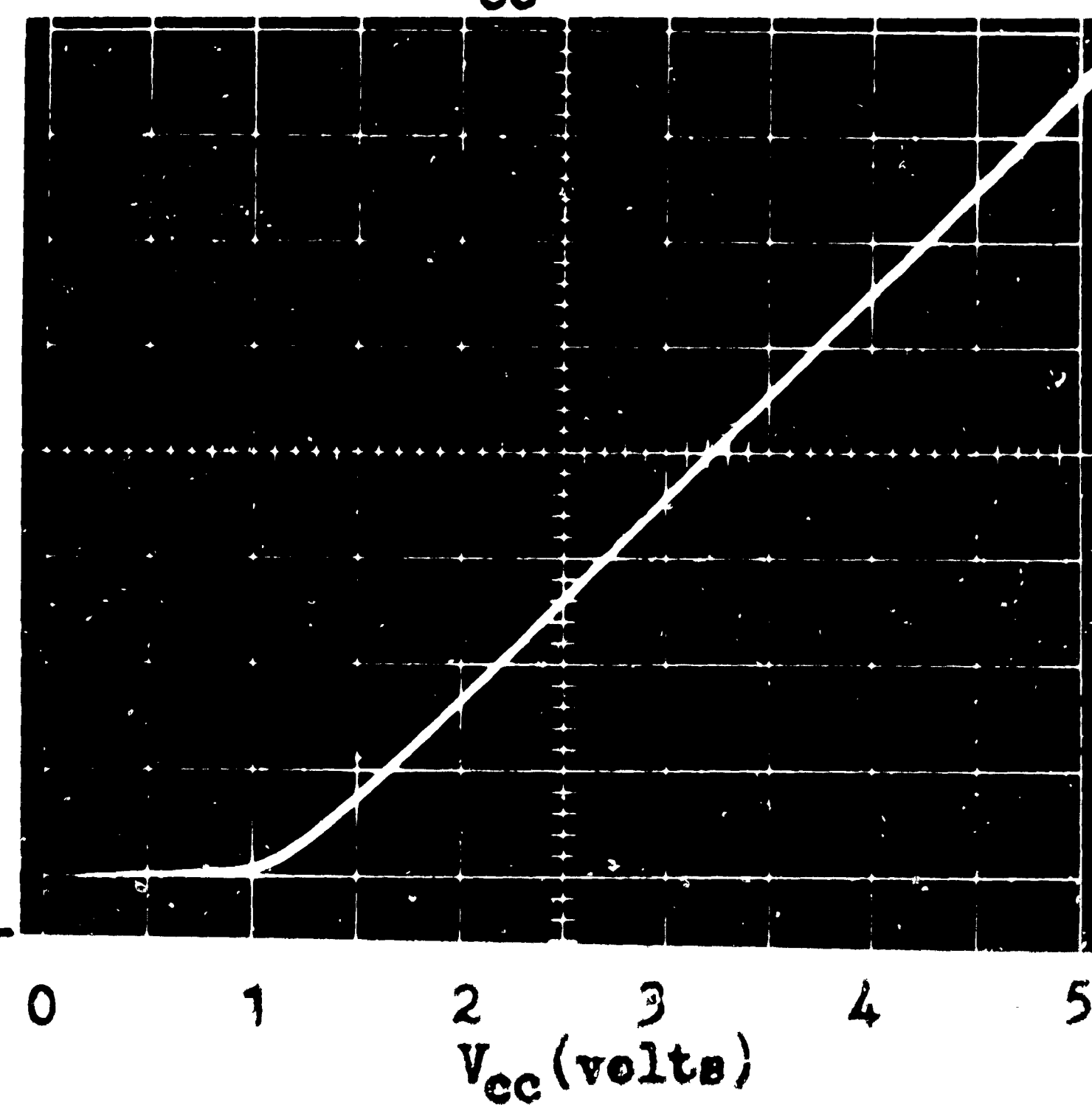
4

3

2

1

0



Circuit SM 6B		Supply Voltage 4.5				Frequency = 1 MC.				Fan-in 1			
Temperature:		-55°C				-40°C				+25°C			
Load		1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})		2.8	2.7	2.9	2.4	2.8	2.8	3.0	2.4	3.0	3.1	3.4	2.7
Pulse Width (ns.)		200	197	200	194	200	198	200	197	200	202	200	205
T_r (ns.)		5.0	45	5.0	51	5.0	45	6.0	48	7.0	64	10	43
T_f (ns.)		8.0	13	8.0	33	7.0	12	7.0	29	5.0	10	4.5	17
T_d (ns.)			13		14		12		14		11		12
T_s (ns.)			9.0		9.0		9.0		9.0		8.0		8.0
T_{pd} (ns.)			14.5		20		14		19		13.5		17
Temperature:		+85°C				+125°C							
Load		1	1	20	20	1	1	20	20				
Test Circuit		input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})		3.2	3.4	3.7	3.0	3.3	3.6	3.8	3.1				
Pulse Width (ns.)		200	206	200	213	200	211	200	220				
T_r (ns.)		11	66	15	41	14	52	17	50				
T_f (ns.)		5.0	9.0	5.0	15	5.0	10	5.0	15				
T_d (ns.)			11		12		10		11				
T_s (ns.)			9.0		11		9.0		12				
T_{pd} (ns.)			14		18		15		20				

Circuit SM 6B		Supply Voltage 5.0		Frequency = 1 ms. Fan-in 1											
Temperature:		-55°C					-40°C					+25°C			
Load		1	1	20	20	20	1	1	20	20	20	1	1	20	20
Test Circuit		input	output	input	output	input	input	output	input	output	input	input	output	input	output
Pulse Amplitude (V_{pp})		3.3	3.2	3.5	2.8		3.3	3.3	3.6	2.9		3.5	3.6	4.0	3.2
Pulse Width (ns.)		200	200	200	201		200	201	200	203		200	204	200	208
T_r (ns.)		5.0	36	7.0	46		6.0	36	8.0	44		7.5	45	12	38
T_f (ns.)		7.0	11	7.0	30		6.0	10	6.0	28		4.5	8.5	4.5	14
T_d (ns.)			11		12			10		11			9.0		11
T_s (ns.)			9.0		9.0			8.0		8.0			8.0		8.0
T_{pd} (ns.)			13		18			12.5		17			12		16
Temperature:		+85°C					+125°C								
Load		1	1	20	20	20	1	1	20	20	20				
Test Circuit		input	output	input	output	input	input	output	input	output	input				
Pulse Amplitude (V_{pp})		3.7	3.9	4.2	3.4		3.8	4.0	4.3	3.5					
Pulse Width (ns.)		200	208	200	216		200	214	200	224					
T_r (ns.)		12	41	17	40		15	48	20	50					
T_f (ns.)		5.0	9.0	5.0	14		4.5	9.0	5.0	14					
T_d (ns.)			10		11			10		11					
T_s (ns.)			9.0		11			9.0		12					
T_{pd} (ns.)			13		18			14		20					

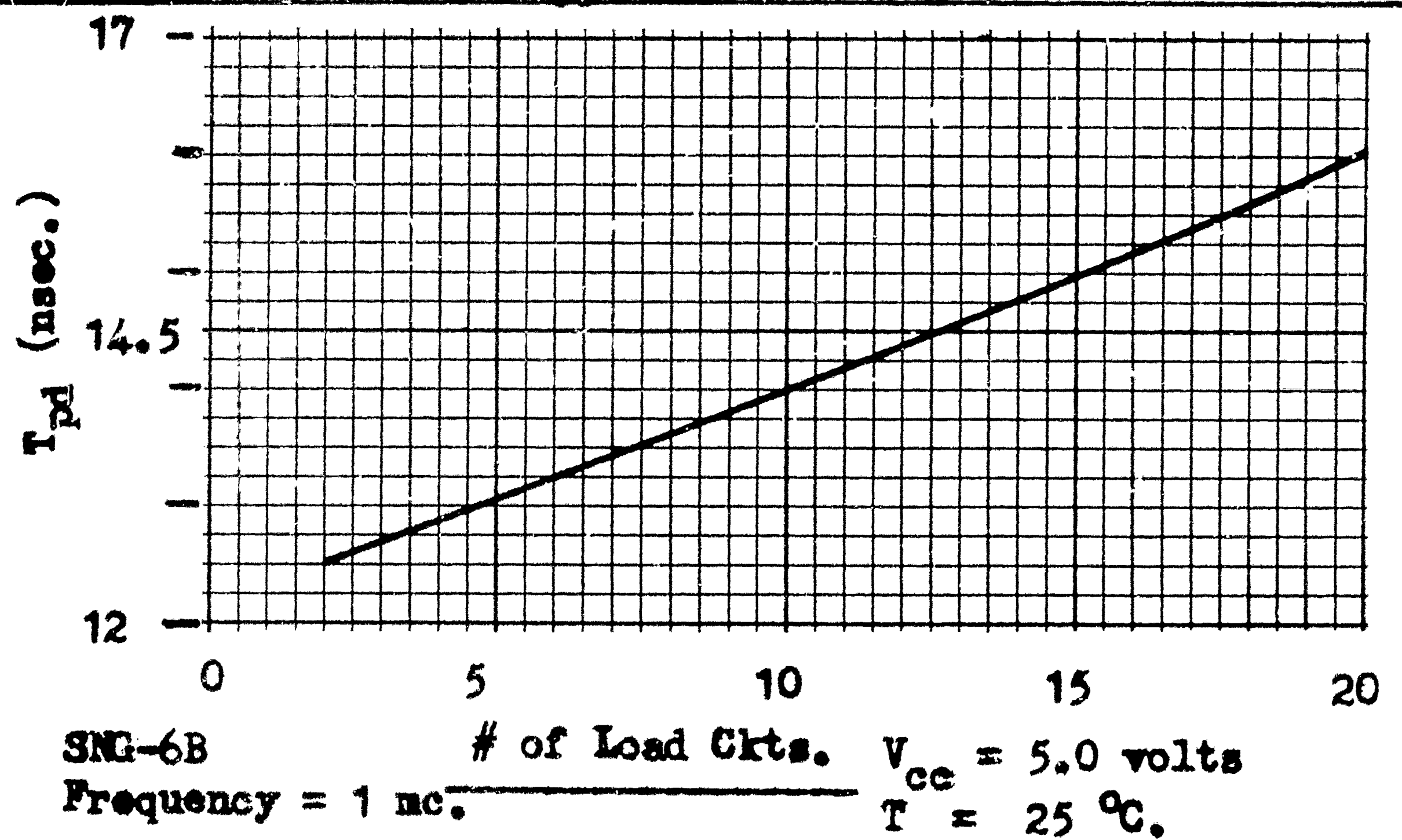
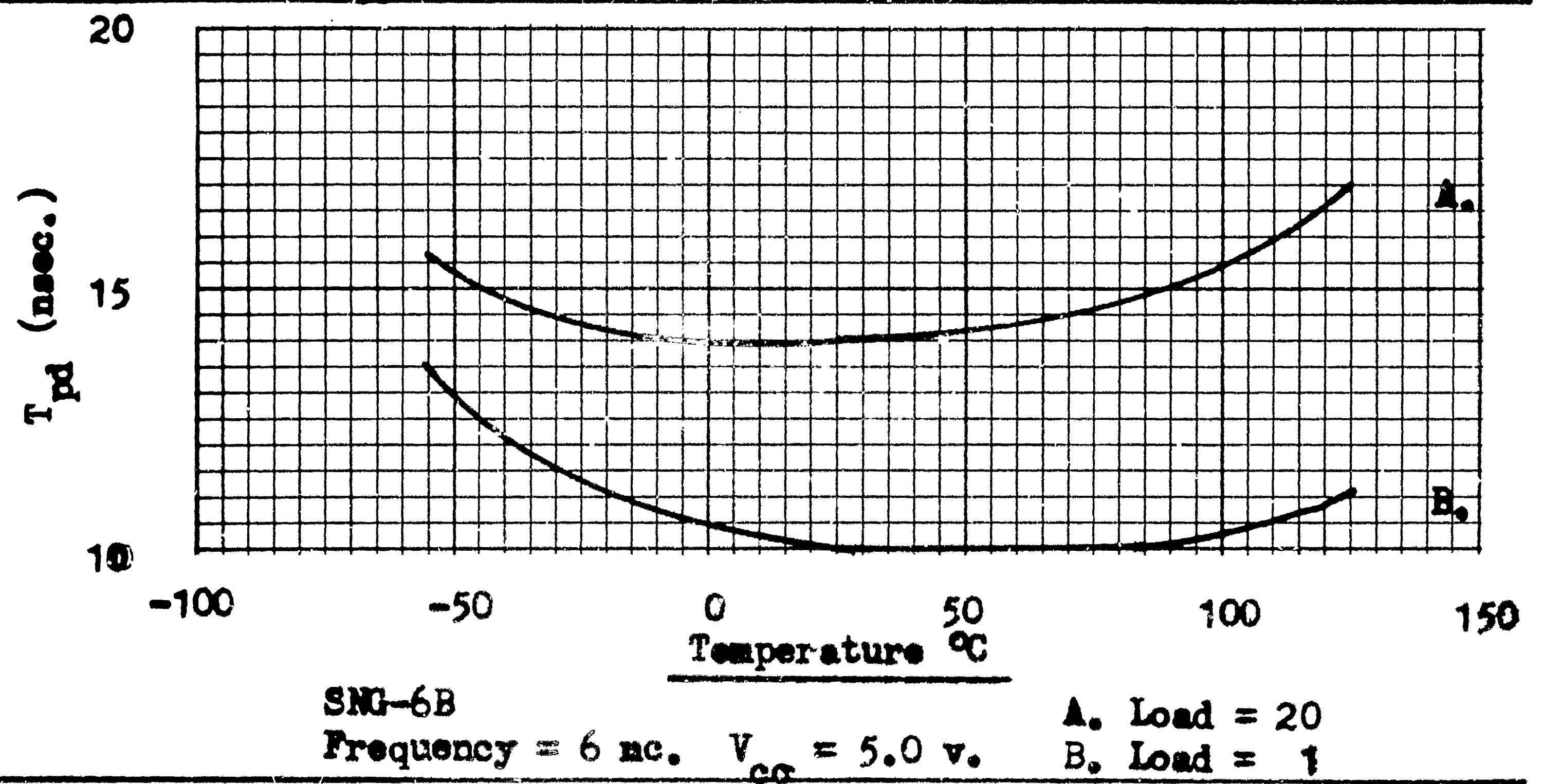
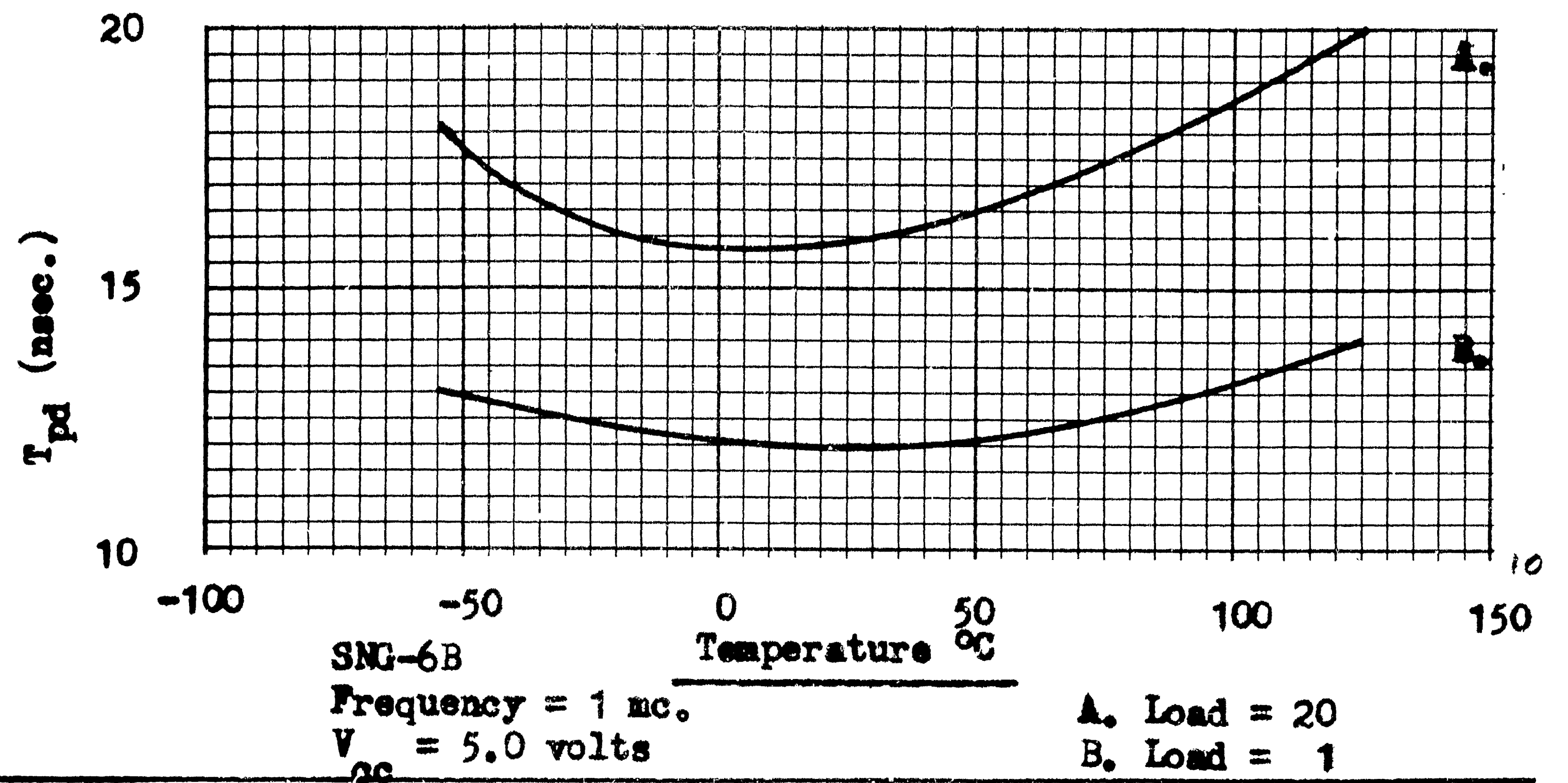
Circuit SK 6B		Supply Voltage 5.5				Frequency = 1 mc.				Fan-in 1			
Temperature:		-55°C				-40°C				+25°C			
Load		1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})		3.8	3.7	4.1	3.3	3.8	3.8	4.3	3.4	4.0	4.1	4.6	3.6
Pulse Width (ns.)		200	202	200	204	200	202	200	206	200	205	200	211
T_r (ns.)		6.0	31	8.0	44	6.0	31	9.0	42	8.5	36	14	37
T_f (ns.)		6.0	9.4	5.0	30	5.5	9.0	5.0	19	4.2	8.0	5.0	13
T_d (ns.)			10		11		9.0		11		9.0		10
T_s (ns.)			9.0		9.0		8.0		8.0		8.0		10
T_{pd} (ns.)			12		17		12		16		11		16
Temperature:		+85°C				+125°C							
Load		1	1	20	20	1	1	20	20				
Test Circuit		input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})		4.2	4.1	4.9	3.9	4.3	4.6	4.9	4.0				
Pulse Width (ns.)		200	211	200	219	200	216	200	227				
T_r (ns.)		13	38	39	40	17	46	41	51				
T_f (ns.)		4.0	8.0	5.0	13	4.0	9.0	4.5	13				
T_d (ns.)			9.0		10		9.0		10				
T_s (ns.)			9.0		11		10		12				
T_{pd} (ns.)			12.5		17.5		13		20				

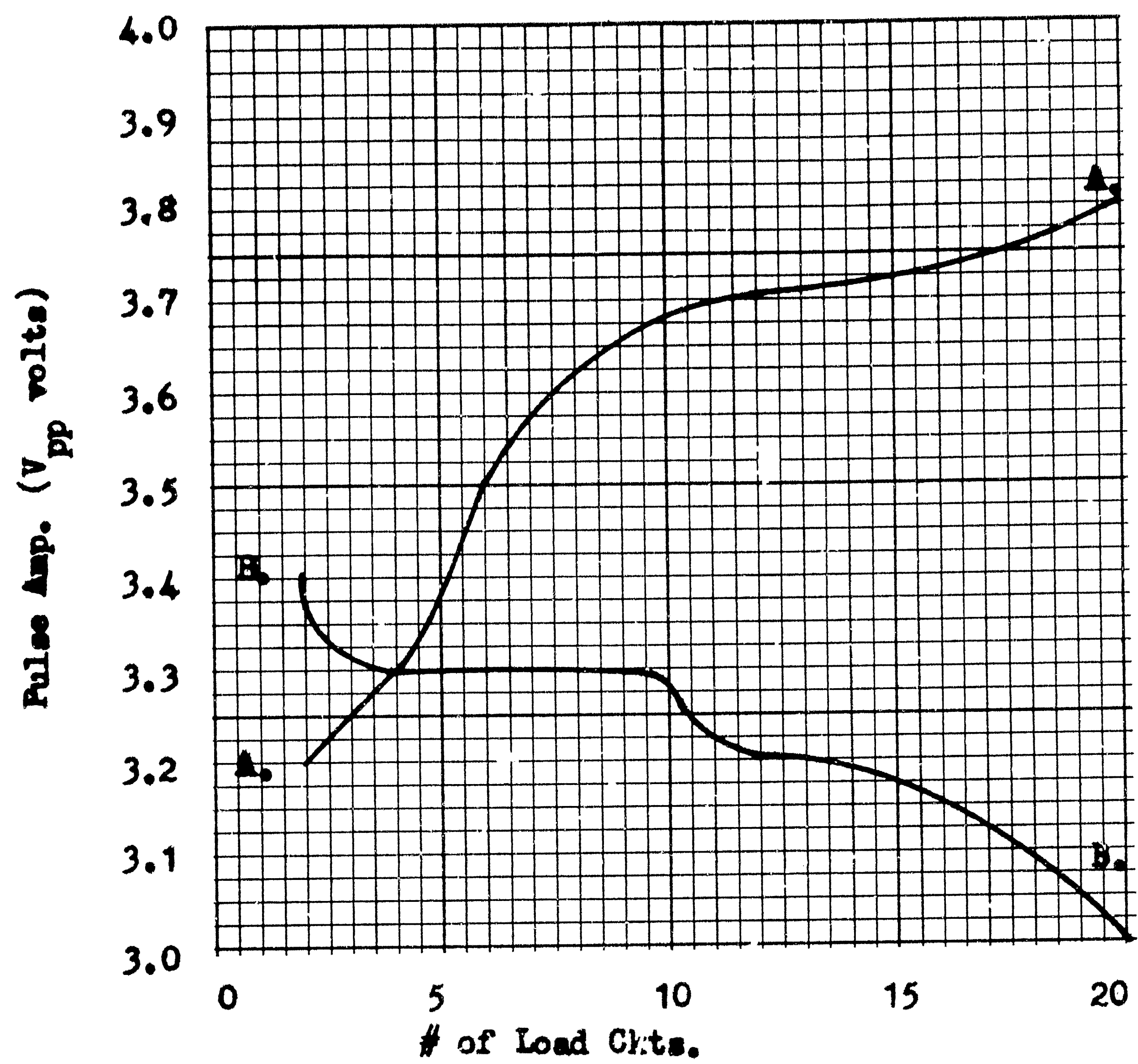
Circuit <u>SMG 6B</u>		Supply Voltage <u>5.0</u>				Frequency = <u>6 mc.</u>				Fan-in <u>1</u>			
Temperature:		-55°C				-40°C				+25°C			
Load		1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})		3.2	3.0	3.8	2.9	3.2	3.1	3.9	2.9	3.4	3.3	4.1	3.2
Pulse Width (ns.)		50	51	50	52	50	52	50	53	50	54	50	58
T_r (ns.)		5.0	25	7.0	43	5.0	24	9.0	39	8.0	25	34	35
T_f (ns.)		6.0	8.0	6.0	30	5.0	7.0	5.0	17	4.0	6.0	4.0	13
T_d (ns.)			9.0		11		8.0		10		7.0		8.0
T_s (ns.)			8.0		6.0		8.0		9.0		7.0		8.0
T_{pd} (ns.)			11.5		15.5		11		14.5		10		14
Temperature:		+85°C				+125°C							
Load		1	1	20	20	1	1	20	20				
Test Circuit		input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})		3.6	3.6	4.4	3.3	3.7	3.7	4.4	3.4				
Pulse Width (ns.)		50	59	50	68	50	66	50	78				
T_r (ns.)		11	29	37	39	14	36	39	48				
T_f (ns.)		4.0	6.0	4.0	13	4.0	6.0	4.0	13				
T_d (ns.)			7.0		8.0		7.0		7.0				
T_s (ns.)			7.0		10		8.0		11				
T_{pd} (ns.)			10		15		11		17				

SNG 6B: $V_{cc} = 5.0$ v. Frequency = 1 mc. Input P. Width = 200 nsec.

Load Ckts.	20	18	16	14	12	10	8	6	4	2
T_{pd}	16.0	15.5	15.0	14.5	14.5	14.0	13.5	13.5	13.0	12.5
T_r Output	37.5	37.0	36.0	34.0	33.0	33.0	33.0	33.0	33.0	33.0
T_f Output	13.5	13.0	12.5	12.0	11.5	11.0	11.0	10.0	10.0	9.0
Pulse Amp. (Input)	3.8	3.8	3.7	3.7	3.7	3.6	3.5	3.5	3.3	3.2
Pulse Amp. (Output)	3.0	3.1	3.1	3.2	3.2	3.3	3.3	3.3	3.3	3.4

Temperature = 25°C.





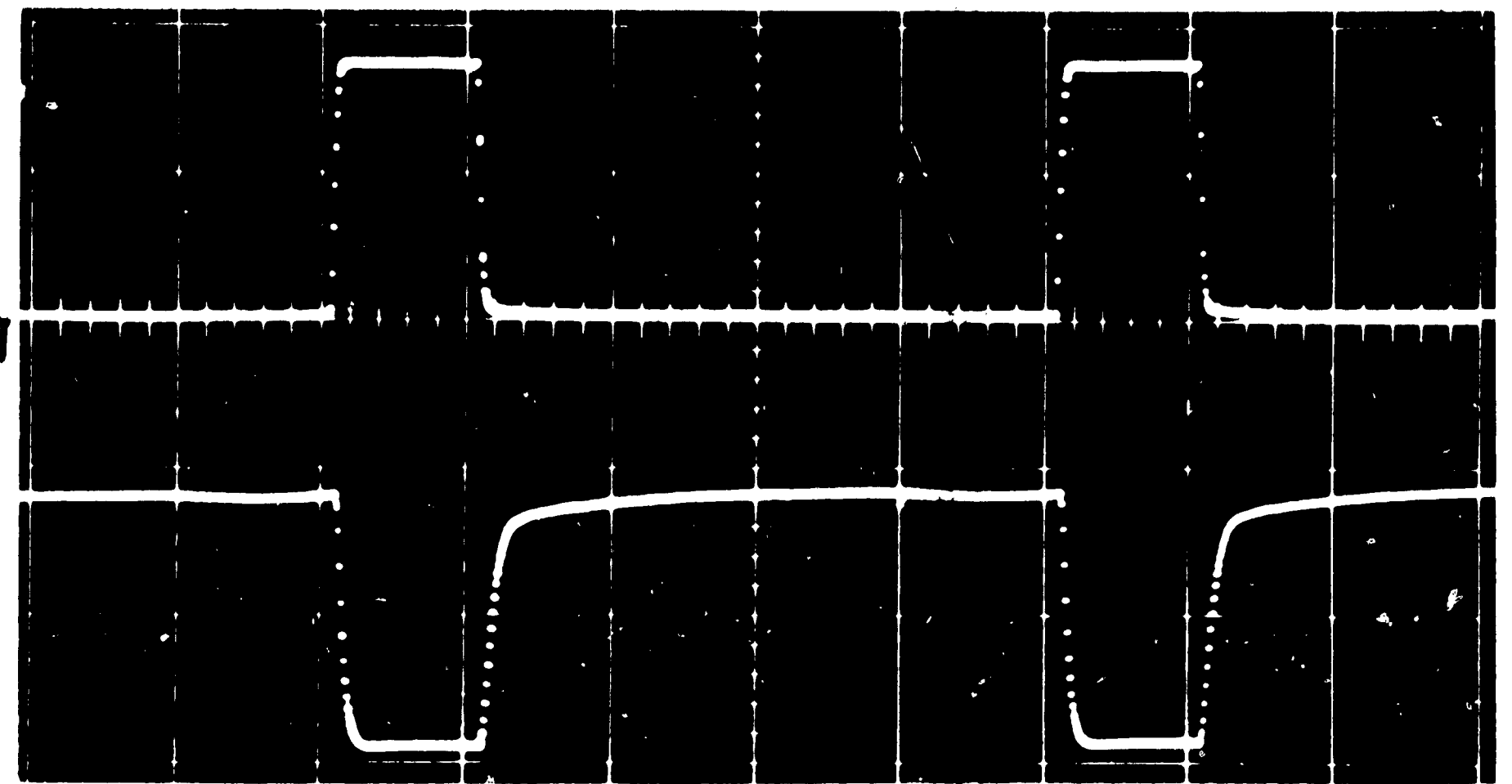
SNG-6B
 Frequency = 1 mc.
 $V_{ce} = 5.0$ volts
 $T = 25^{\circ}\text{C}.$

A. Input Pulse Amp.
 B. Output Pulse Amp.

SNG-6B
 Frequency = 1 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts.
 Temperature = 25°C.

2 v./div.

IN
 OUT

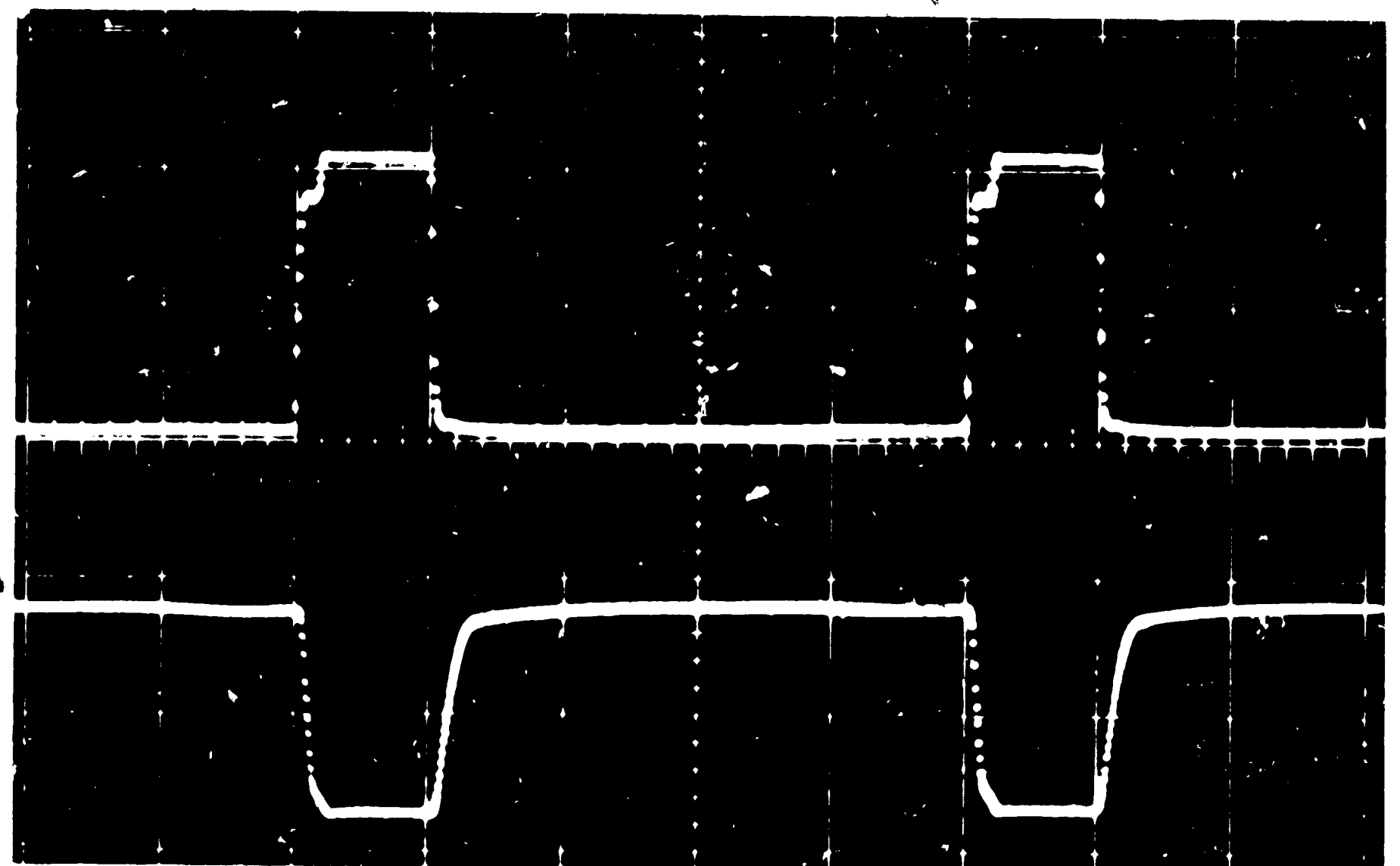


.2 μsec./div.

SNG-6B
 Frequency = 1 mc.
 Load = 20 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C.

2 v./div.

IN
 OUT

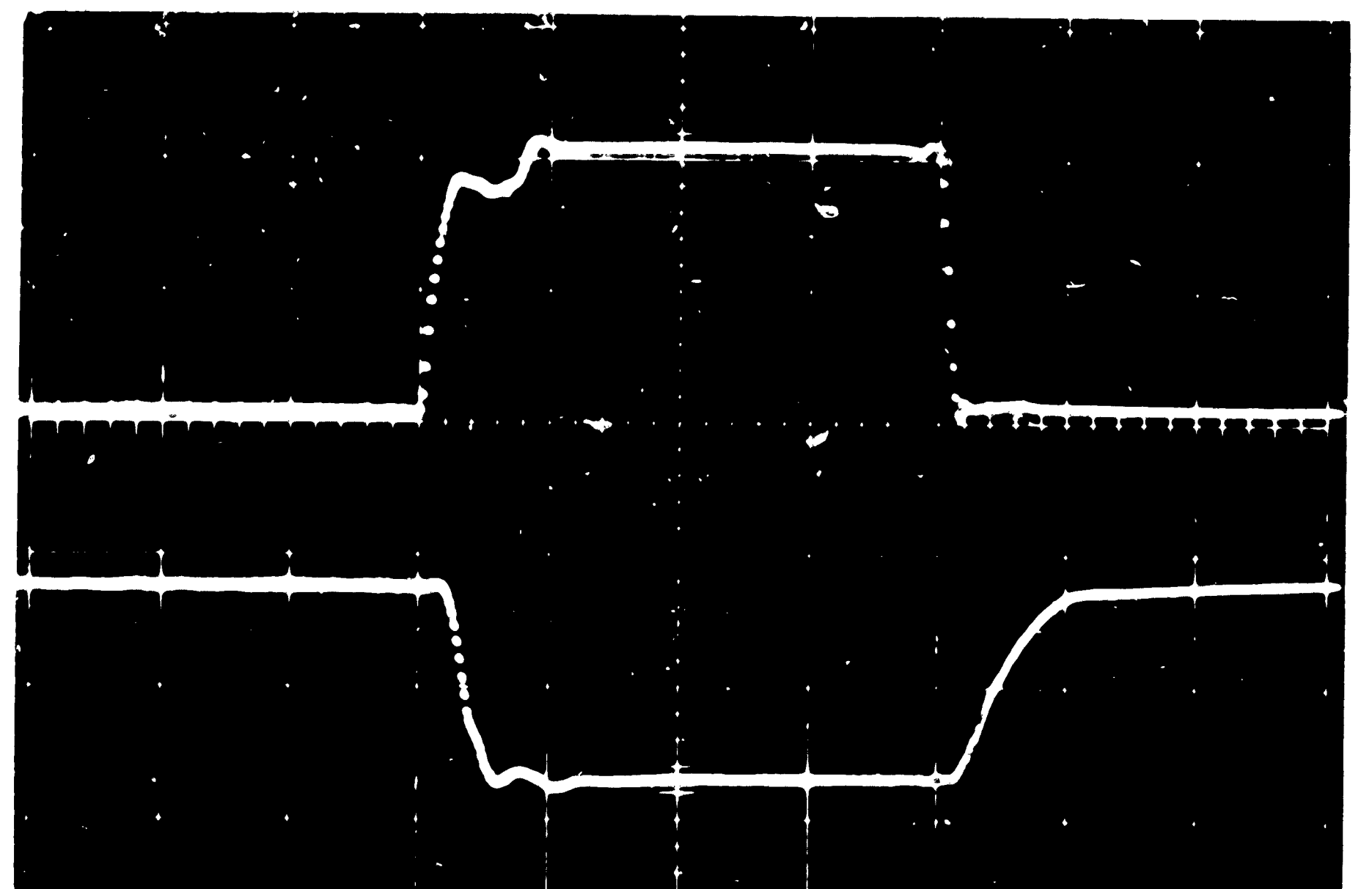


.2 μsec./div.

SNG-6B
 Same as above except
 50 nsec./div.

2 v./div.

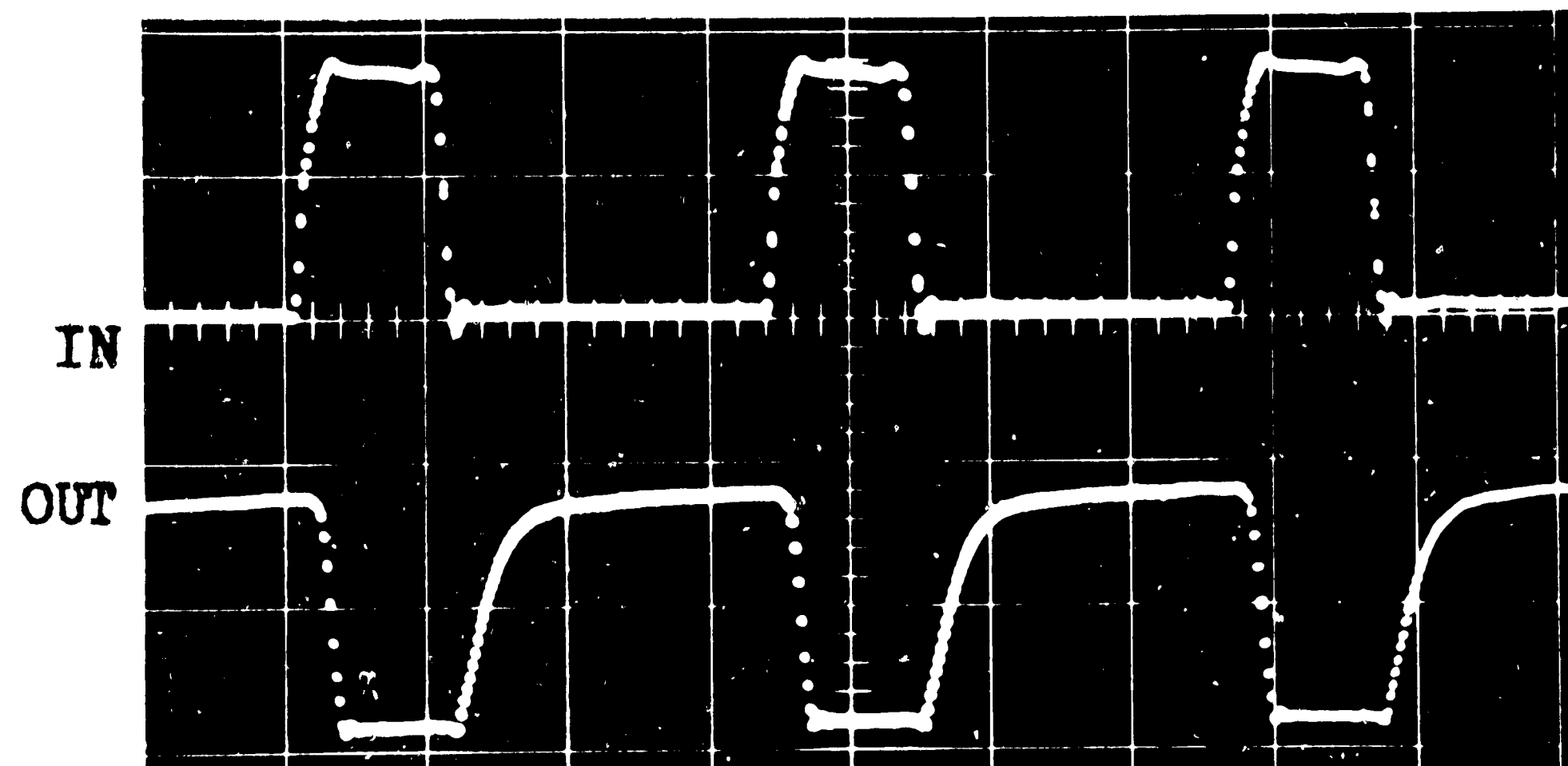
IN
 OUT



50 nsec./div.

SNG-6B
 Frequency = 6 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C.

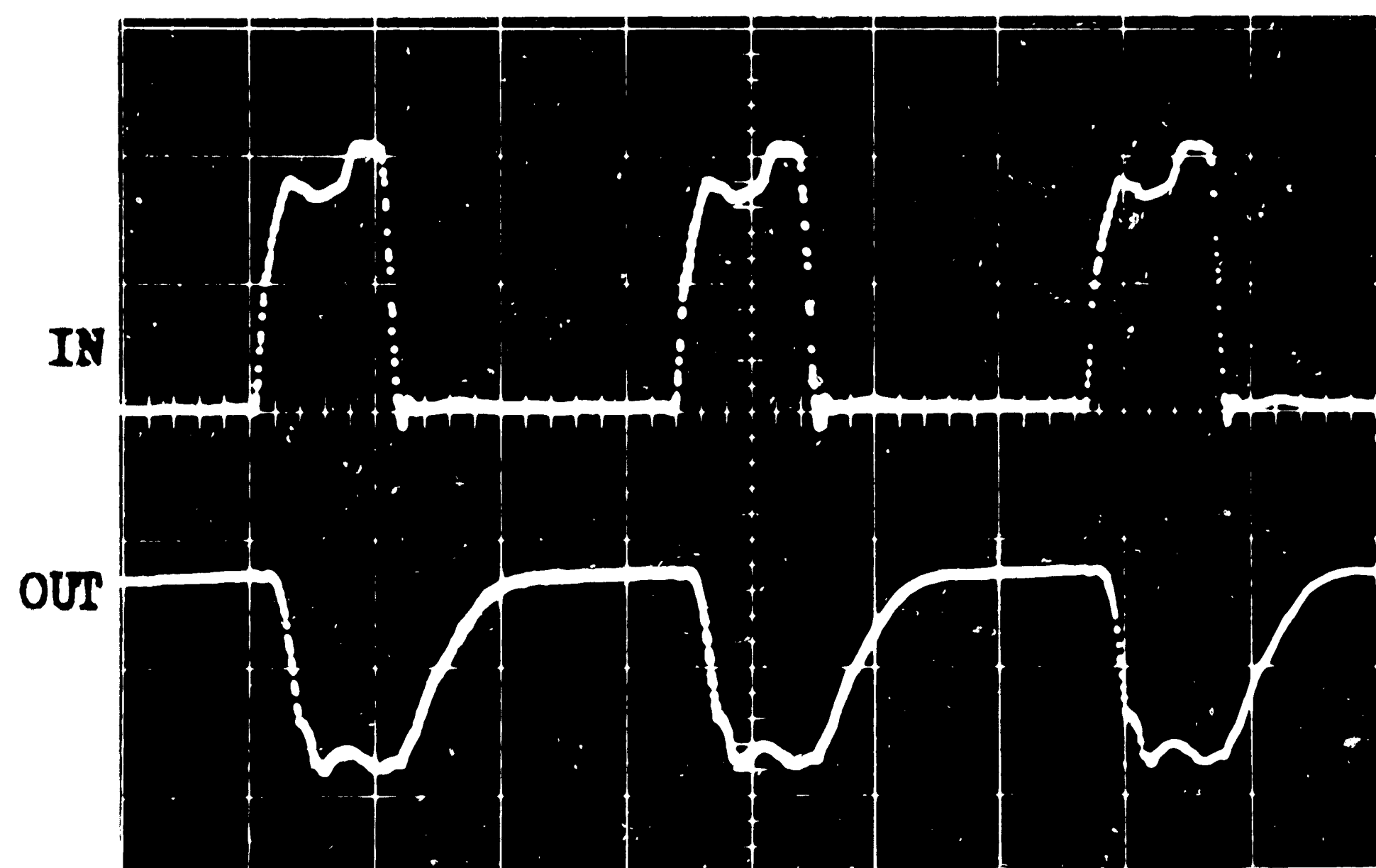
2 v./div.



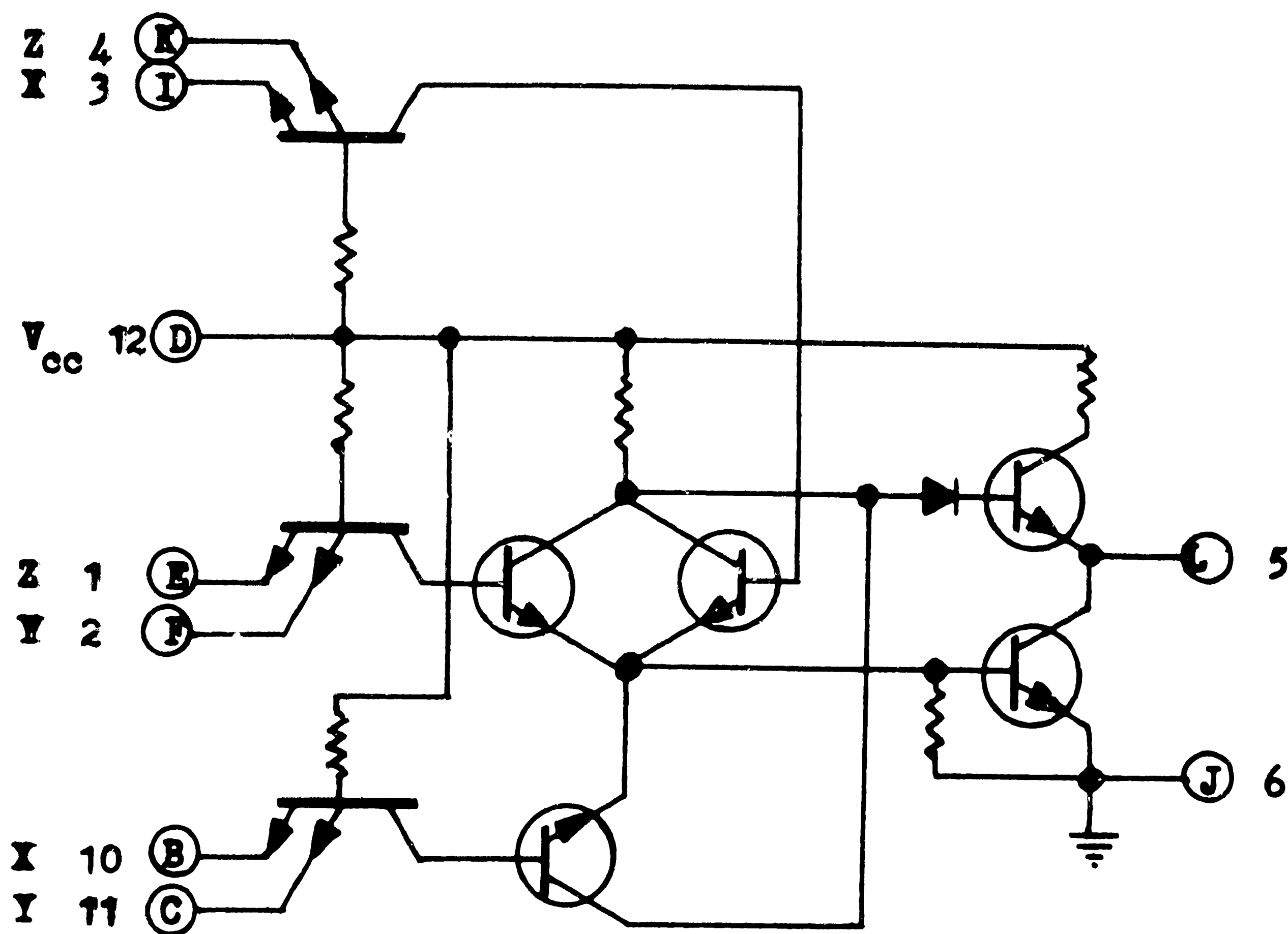
50 nsec./div.

SNG-6B
 Frequency = 6 mc.
 Load = 20 ckts.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C

2 v./div.



50 nsec./div.

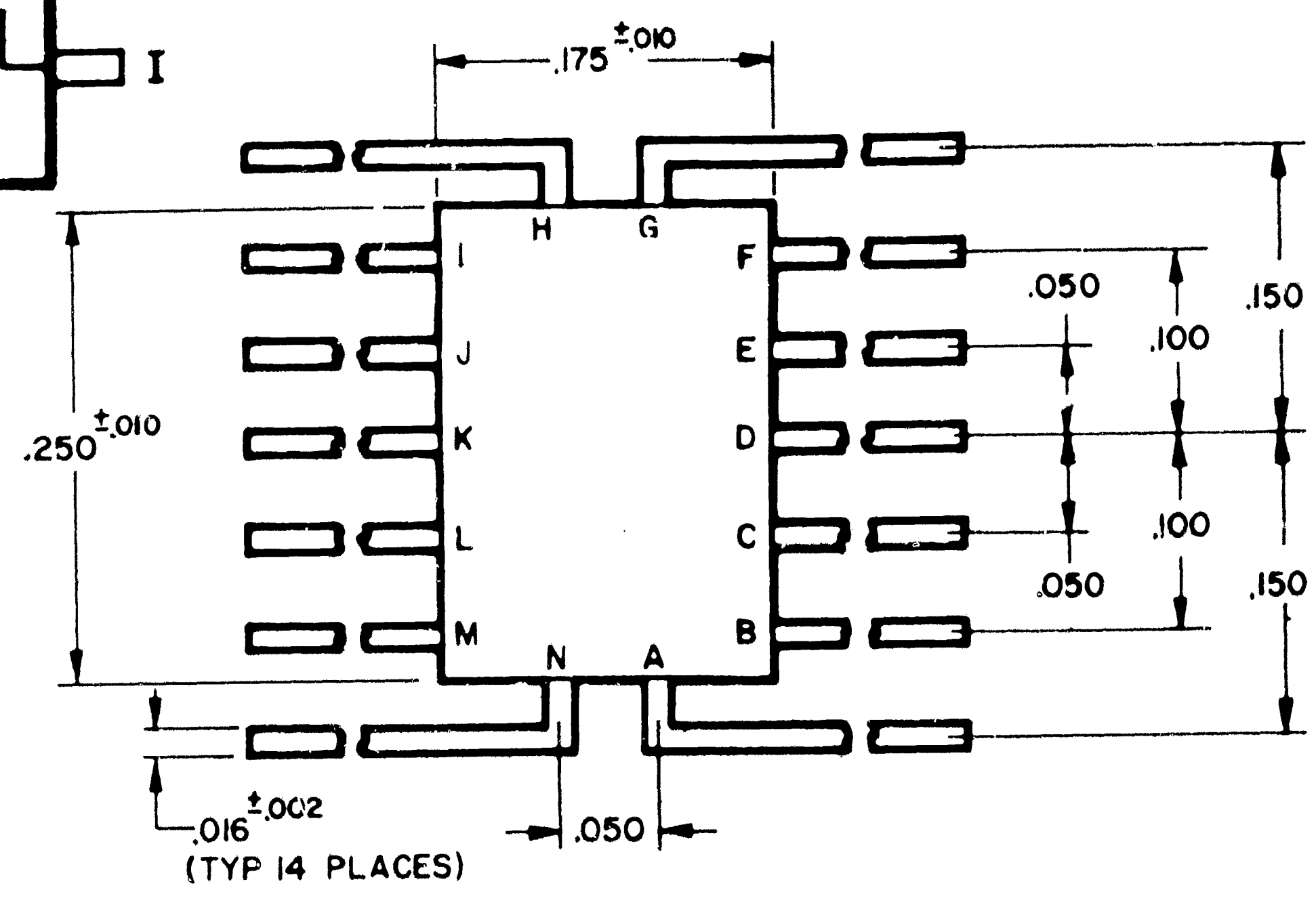
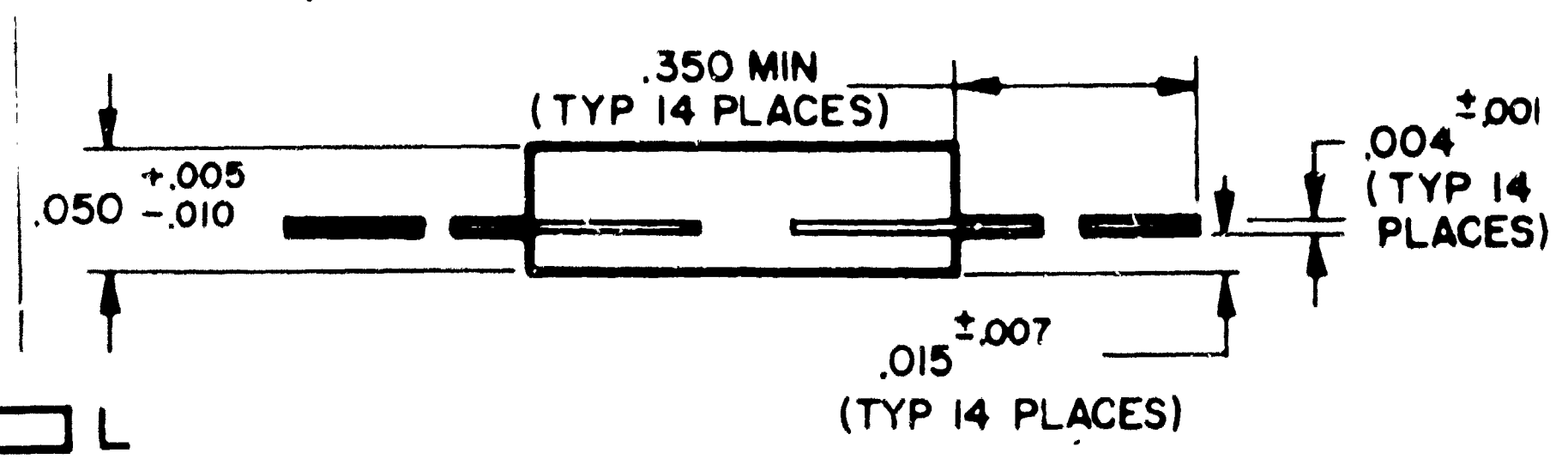
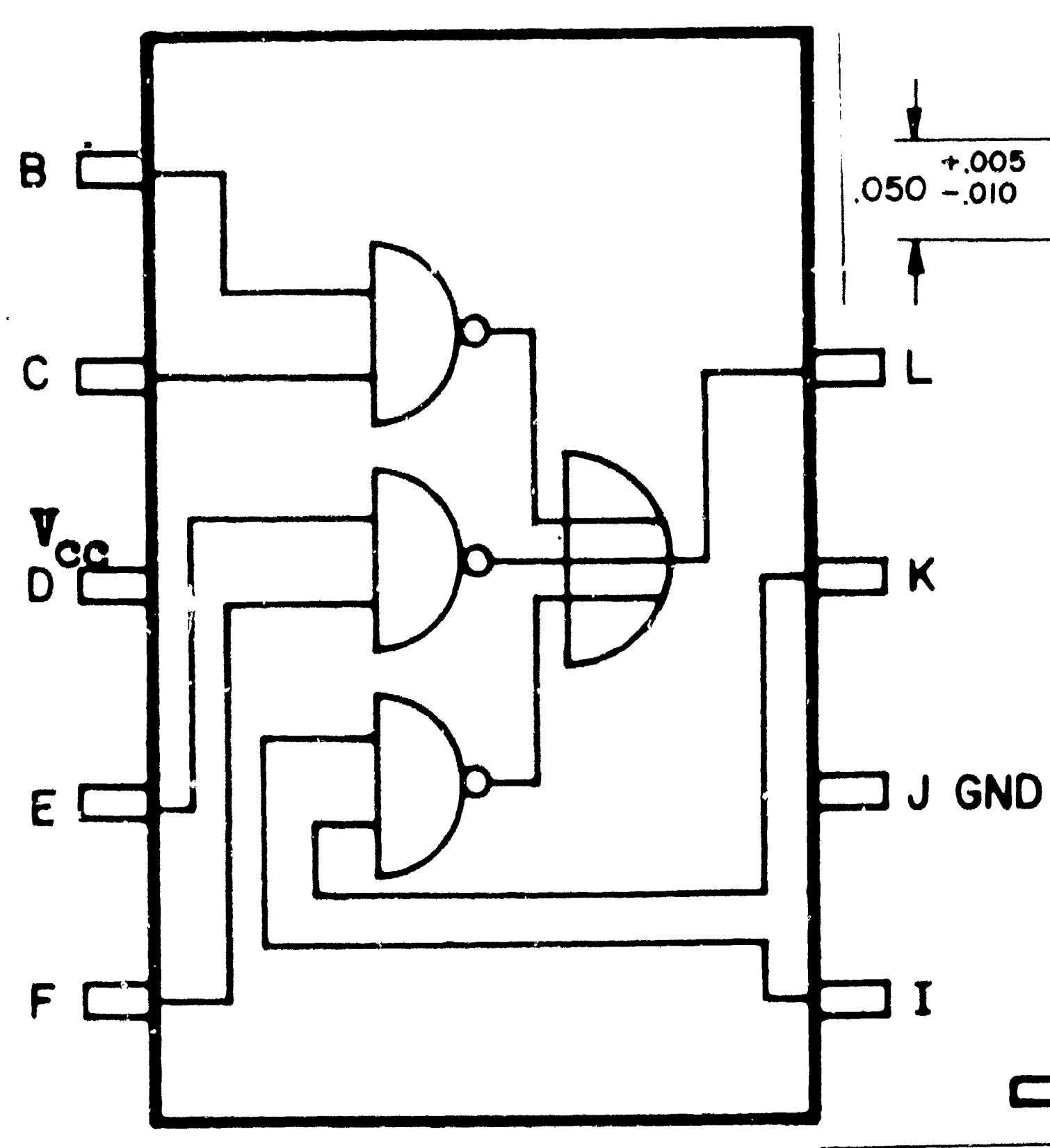
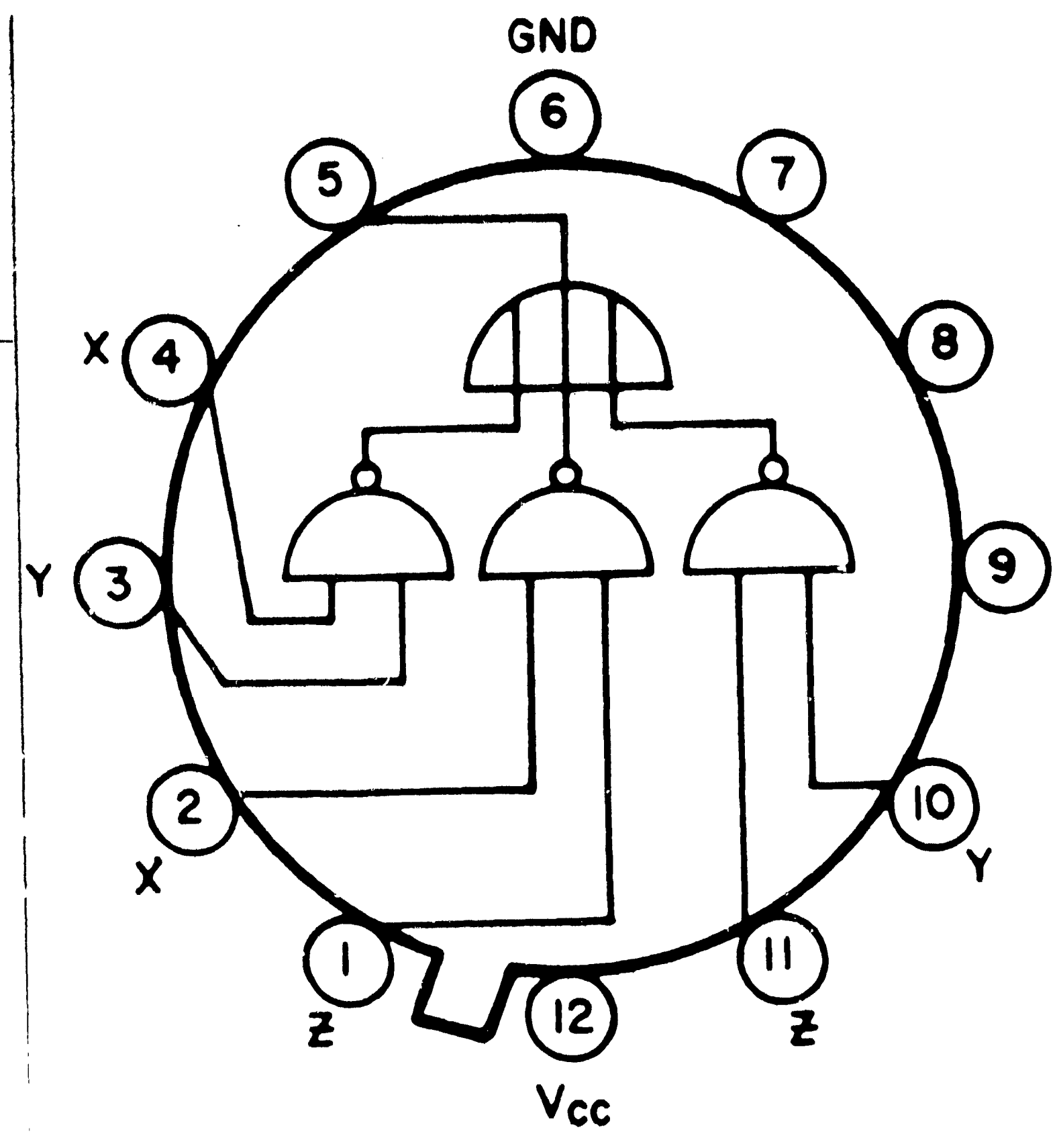
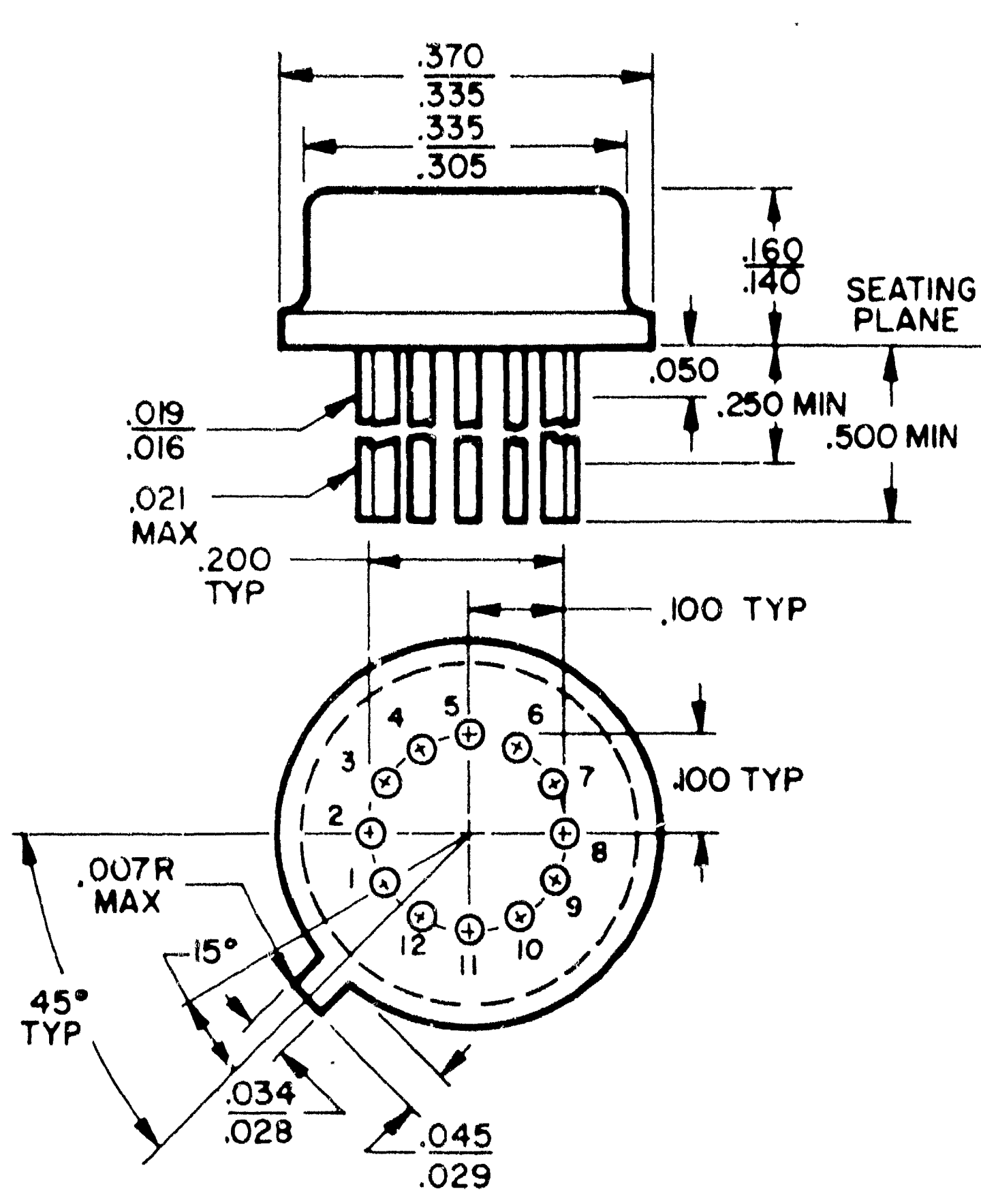


Majority Decision Gate SNG-20

(+) Logic $L = \overline{X \cdot Y} + \overline{X \cdot Z} + \overline{Y \cdot Z}$

(-) Logic $L = \overline{(X+Y)(X+Z)(Y+Z)}$

The SNG-20 AND-NOR Gate (Voter) consists of three, two input AND gates followed by an OR element. It was intended primarily as a majority decision (voter) gate in systems using triple redundancy. The circuit, requiring a single power supply, is of the monolithic, epitaxial, and planar type.

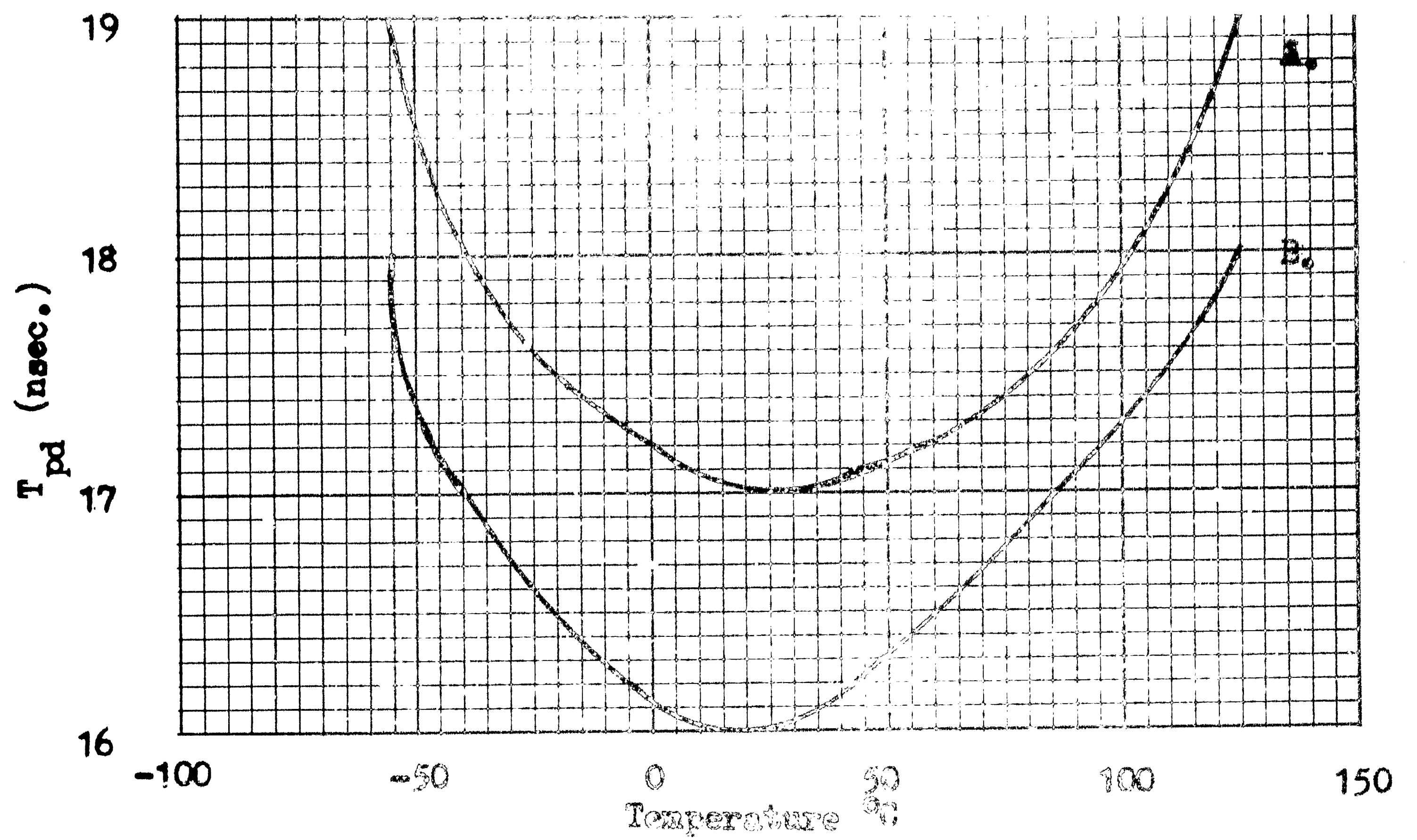


Circuit SNG 20		Supply Voltage 4.5		Frequency = 1mc.		Fan-in 1							
Temperature:		-55°C				-40°C				+25°C			
Lead		1	1	6	6	1	1	6	6	1	1	6	6
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V _{pp})		2.9	3.2	2.9	2.6	2.9	3.3	2.9	2.6	3.0	3.4	3.0	2.7
Pulse Width (ns.)		200	197	200	193	200	200	200	195	200	207	200	205
T _r (ns.)		5.0	273	5.0	35	5.0	261	4.0	28	6.0	200	7.0	23
T _f (ns.)		8.0	10	8.0	16	7.0	10	7.0	14	5.0	8.0	5.0	11
T _d (ns.)			19		20		17		17		13		13
T _s (ns.)			14		13		14		13		14		14
T _{pd} (ns.)			20		22		19		20		18		18.5
Temperature:		+85°C				+125°C				Measured from 90% to 20% instead of 90% to 10% (The larger measurement is from 90% to 10%.)			
Lead		1	1	6	6	1	1	6	6				
Test Circuit		input	output	input	output	input	output	input	output				
Pulse Amplitude (V _{pp})		3.2	3.5	3.2	2.9	3.3	3.6	3.4	3.0				
Pulse Width (ns.)		200	215	200	212	200	222	200	220				
T _r (ns.)		10	25	10	26	13	38	13	30				
T _f (ns.)		4.0	6.0	4.0	9.0	4.0	6.0	4.0	9.0				
T _d (ns)			12		12		11		11				
T _s (ns.)			16		16		18		17				
T _{pd} (ns.)			18		18		19		19				

Circuit SG 20		Supply Voltage 5.0		Frequency = 1 mc.		Fan-in 1							
Temperature:		-55°C				-40°C				+25°C			
Load		1	1	6	6	1	1	6	6	1	1	6	6
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})		3.3	3.7	3.4	3.0	3.3	3.7	3.3	2.9	3.4	3.8	3.5	3.2
Pulse Width (ns.)		200	202	200	199	200	204	200	201	200	210	200	208
T_r (ns.)		5.0	233	5.0	26	5.0	206	5.0	24	7.0	21	8.0	22
T_f (ns.)		7.0	10	7.0	14	6.0	9.0	6.0	13	4.0	6.0	4.0	10
T_d (ns.)			14		15		13		14		11		11
T_s (ns.)			13		13		13		13		14		14
T_{pd} (ns.)			18		19		17		18		16		17
Temperature:		+85°C				+125°C				*Measured from 90% to 20% instead of 90% to 10% (The larger measurement is from 90% to 10%.)			
Load		1	1	6	6	1	1	6	6				
Test Circuit		input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})		3.6	4.0	3.7	3.3	3.8	4.0	3.9	3.5				
Pulse Width (ns.)		200	218	200	215	200	224	200	224				
T_r (ns.)		11	35	12	25	15	37	14	31				
T_f (ns.)		4.0	5.0	4.0	8.0	4.0	6.0	4.0	7.0				
T_d (ns.)			10		10		10		10				
T_s (ns.)			16		16		19		18				
T_{pd} (ns.)			17		17.5		18		19				

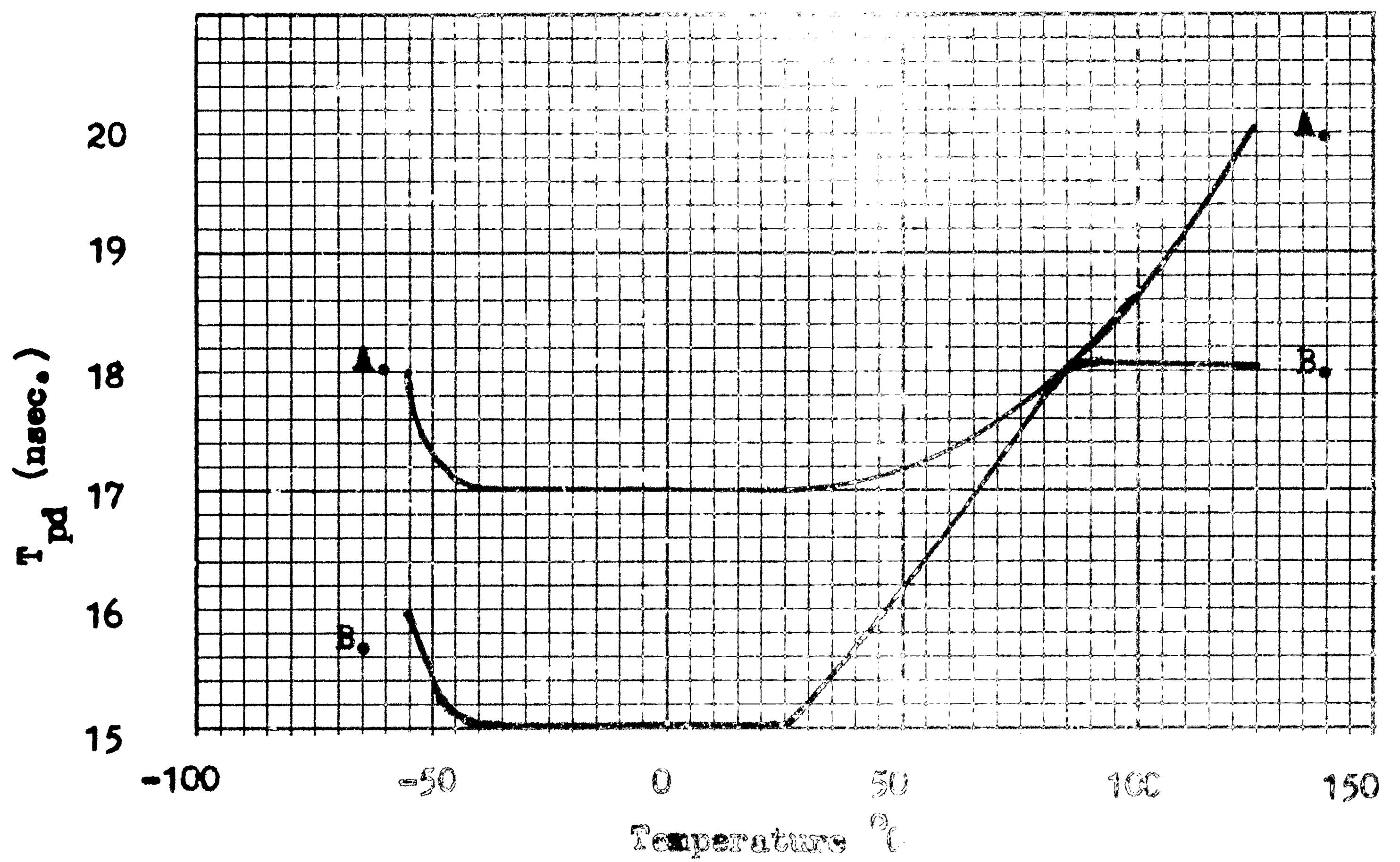
Circuit <u>SN7 20</u>		Supply Voltage <u>5.5</u>		Frequency = <u>1 mc.</u>		Fan-in <u>1</u>							
Temperature:		-55°C				-40°C				+25°C			
Load		1	1	6	6	1	1	6	6	1	1	6	6
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V _{pp})		3.7	4.1	3.8	3.3	3.8	4.2	3.8	3.4	3.9	4.3	4.1	3.6
Pulse Width (ns.)		200	205	200	203	200	207	200	205	200	212	200	209
T _r (ns.)		5.0	22 190	6.0	24	6.0	19 160	8.0	22	8.0	20 22	9.0	22
T _f (ns.)		6.0	9.0	6.0	13	5.0	8.0	5.0	11	4.0	6.0	4.0	8.0
T _d (ns.)			12		12		11		11		10		11
T _s (ns.)			13		13		13		13		14		14
T _{pd} (ns.)			16		17.5		15		17		15		16
Temperature:		+35°C				+125°C				Measured from 90% to 20% instead of 90% to 10% (The larger measurement is from 90% to 10%.)			
Load		1	1	6	6	1	1	6	6	1	1	6	6
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V _{pp})		4.2	4.5	4.3	3.3	4.4	4.5	4.4	3.9				
Pulse Width (ns.)		200	219	200	218	200	227	200	225				
T _r (ns.)		12	32	13	26	16	35	16	32				
T _f (ns.)		4.0	5.0	4.0	7.0	4.0	6.0	4.0	7.0				
T _d (ns.)			10		10		9.0		10				
T _s (ns.)			17		16		19		18				
T _{pd} (ns.)			16		17		17.5		19				

Circuit SNG 20		Supply Voltage 5.0		Frequency = 6 mc. Fan-in 1									
Temperature:		-55°C				-40°C				+25°C			
Load		1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit		input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V _{pp})		3.3	3.0	3.3	2.9	3.4	3.1	3.4	3.0	3.5	3.3	3.5	3.1
Pulse Width (ns.)		50	51	50	50	50	53	50	52	50	58	50	58
T _r (ns.)		5.0	18	5.0	25	5.0	18	5.0	24	7.0	21	8.0	23
T _f (ns.)		6.0	9.0	6.0	14	5.0	8.0	5.0	13	4.0	6.0	4.0	9.0
T _d (ns.)			13		13		12		12		11		11
T _s (ns.)			13		11		12		11		13		14
T _{pd} (ns.)			16		18		15		17		15		17
Temperature:		+85°C				+125°C							
Load		1	1	20	20	1	1	20	20				
Test Circuit		input	output	input	output	input	output	input	output				
Pulse Amplitude (V _{pp})		3.6	3.7	3.8	3.6	3.8	3.9	3.9	3.7				
Pulse Width (ns.)		50	66	50	66	50	74	50	75				
T _r (ns.)		11	28	13	30	14	35	16	36				
T _f (ns.)		4.0	6.0	4.0	9.0	4.0	6.0	4.0	8.0				
T _d (ns.)			10		10		10		10				
T _s (ns.)			15		15		18		17				
T _{pd} (ns.)			18		18		18		20				



SNG-20
Frequency = 1 mc.
 V_{cc} = 5.0 volts

A. Load = 6
B. Load = 1



SNG-20
Frequency = 6 mc.
 V_{cc} = 5.0 volts

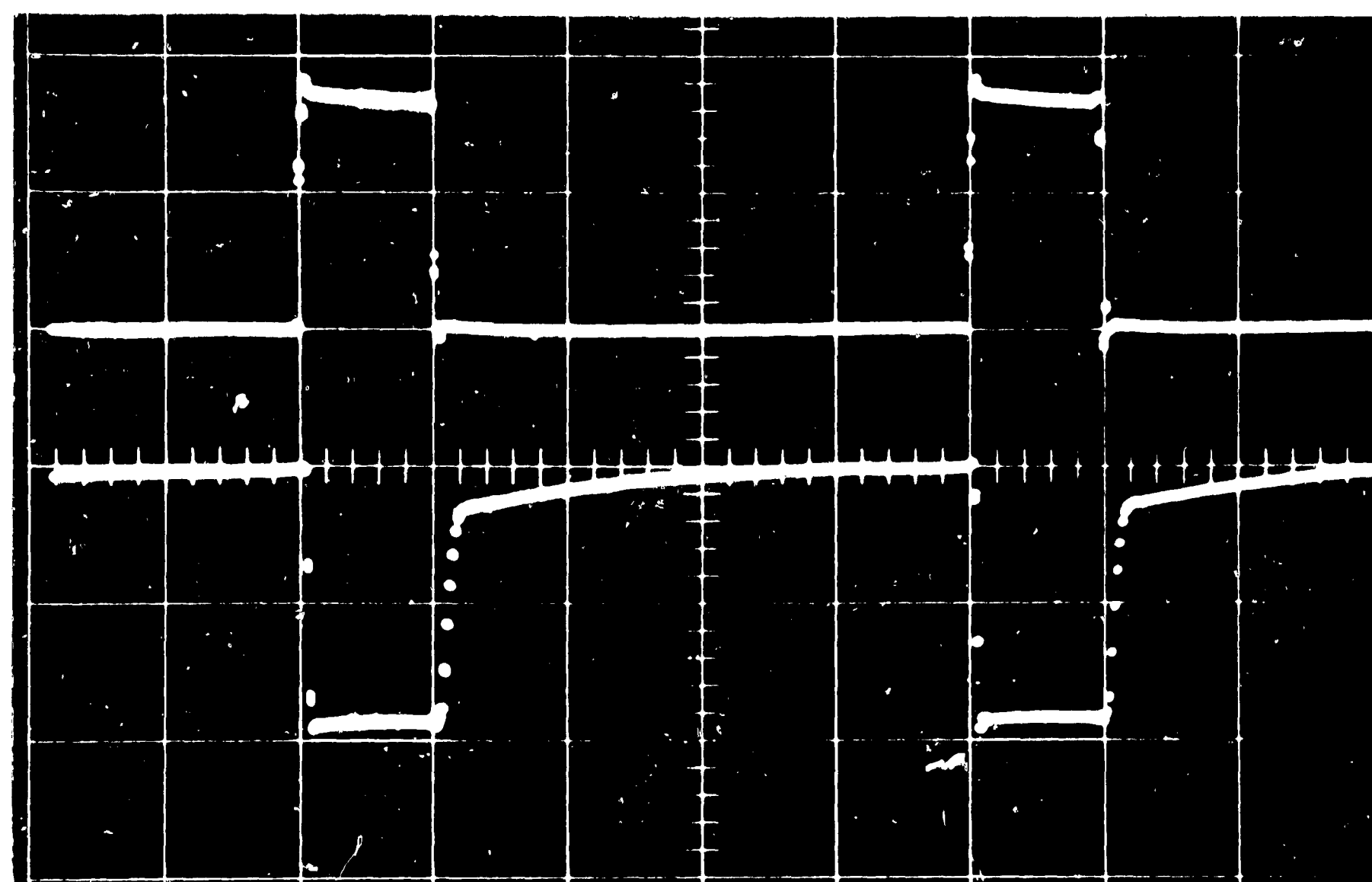
A. Load = 20
B. Load = 1

SNG-20
 Frequency = 1 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C.

IN

OUT

2 v./div.

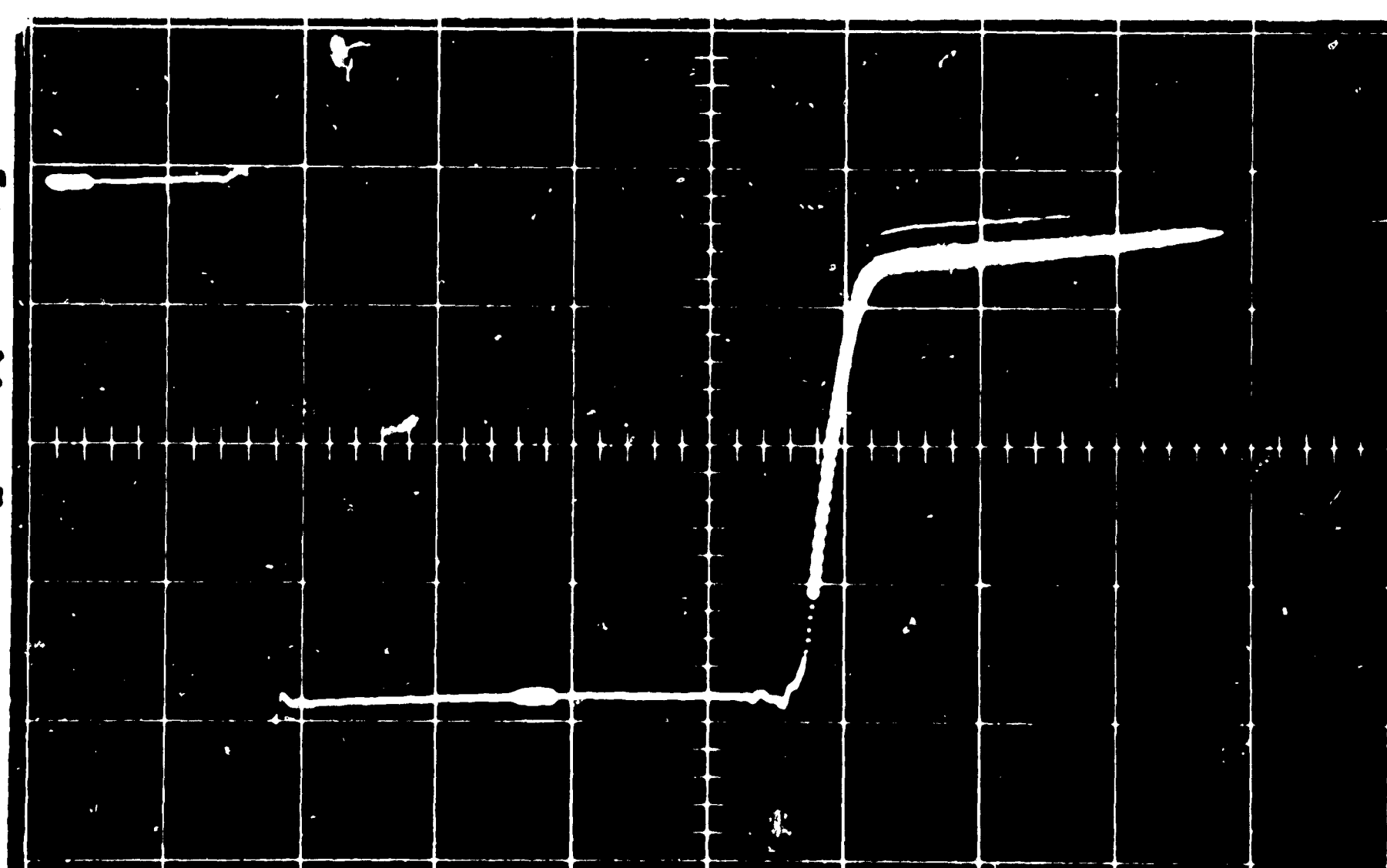


0.2 μsec./div.

SNG-20
 Frequency = 1 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C.
 Intensified zone showing
 90% to 10% measurement
 of rise time on negative
 going output pulse.
 The 90% to 20%
 measurement was also
 given since the in-
 tensified zone ex-
 tended over the
 knee of the rise time.

OUT

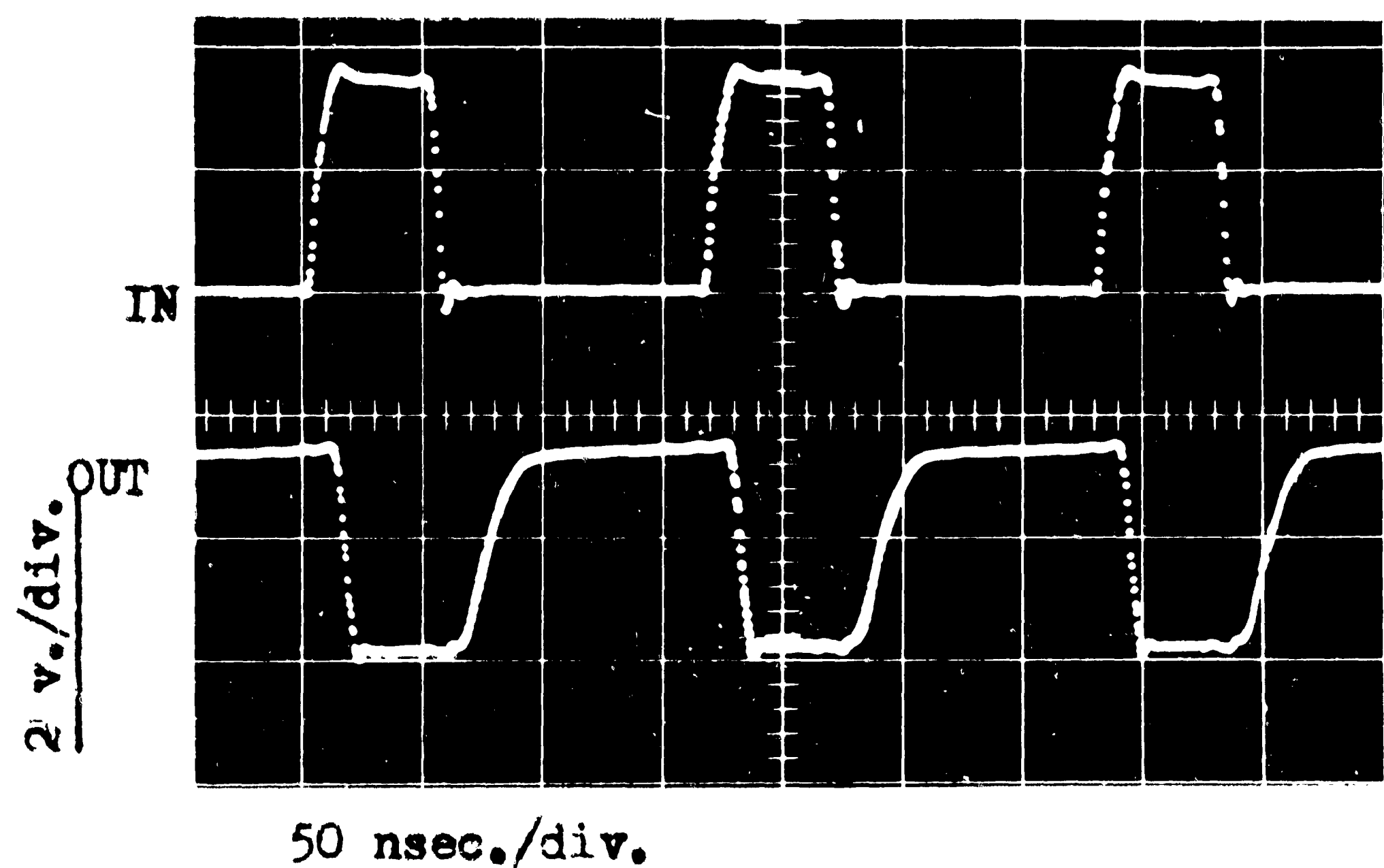
1 v./div.



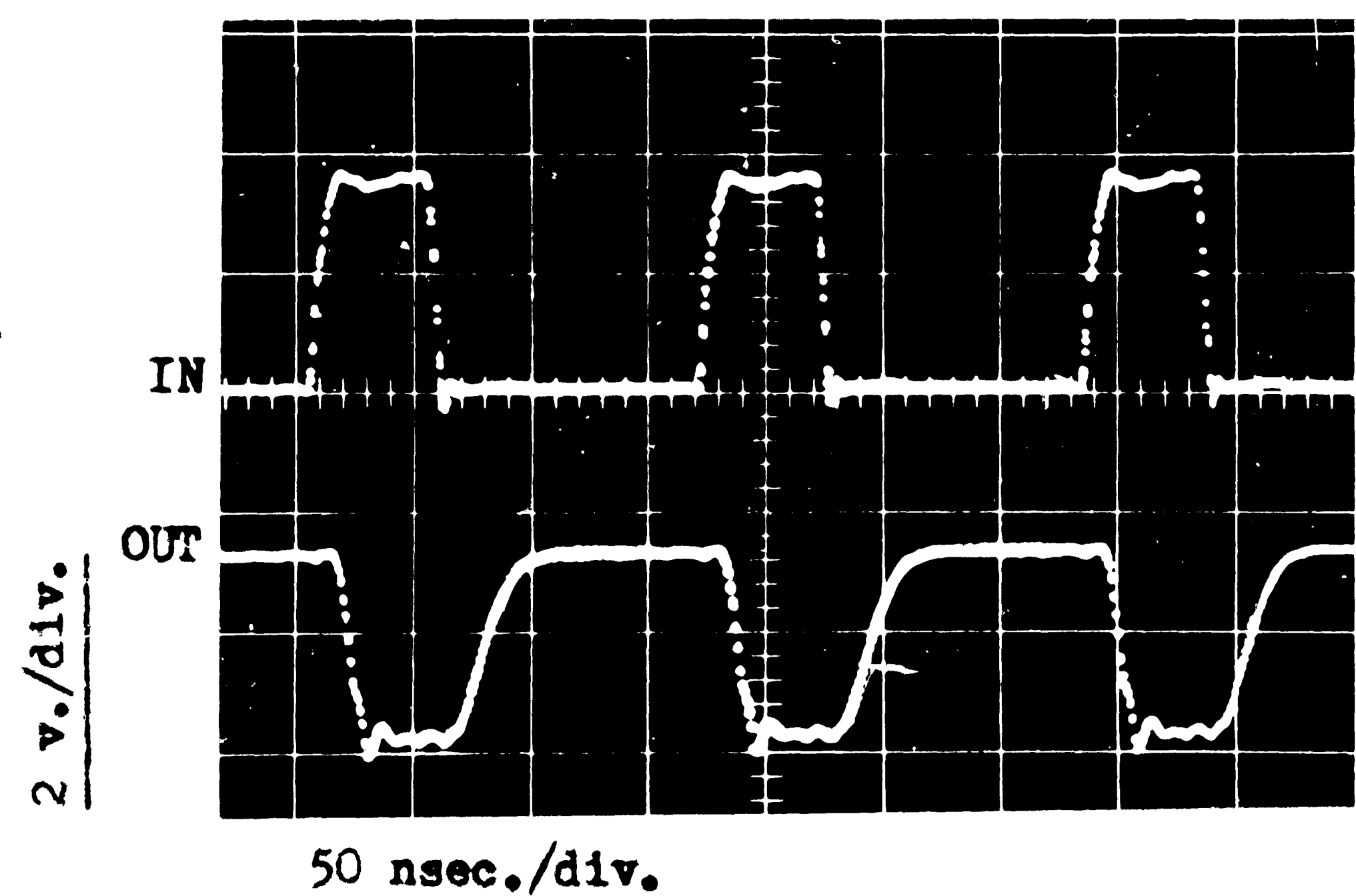
50 nsec./div.

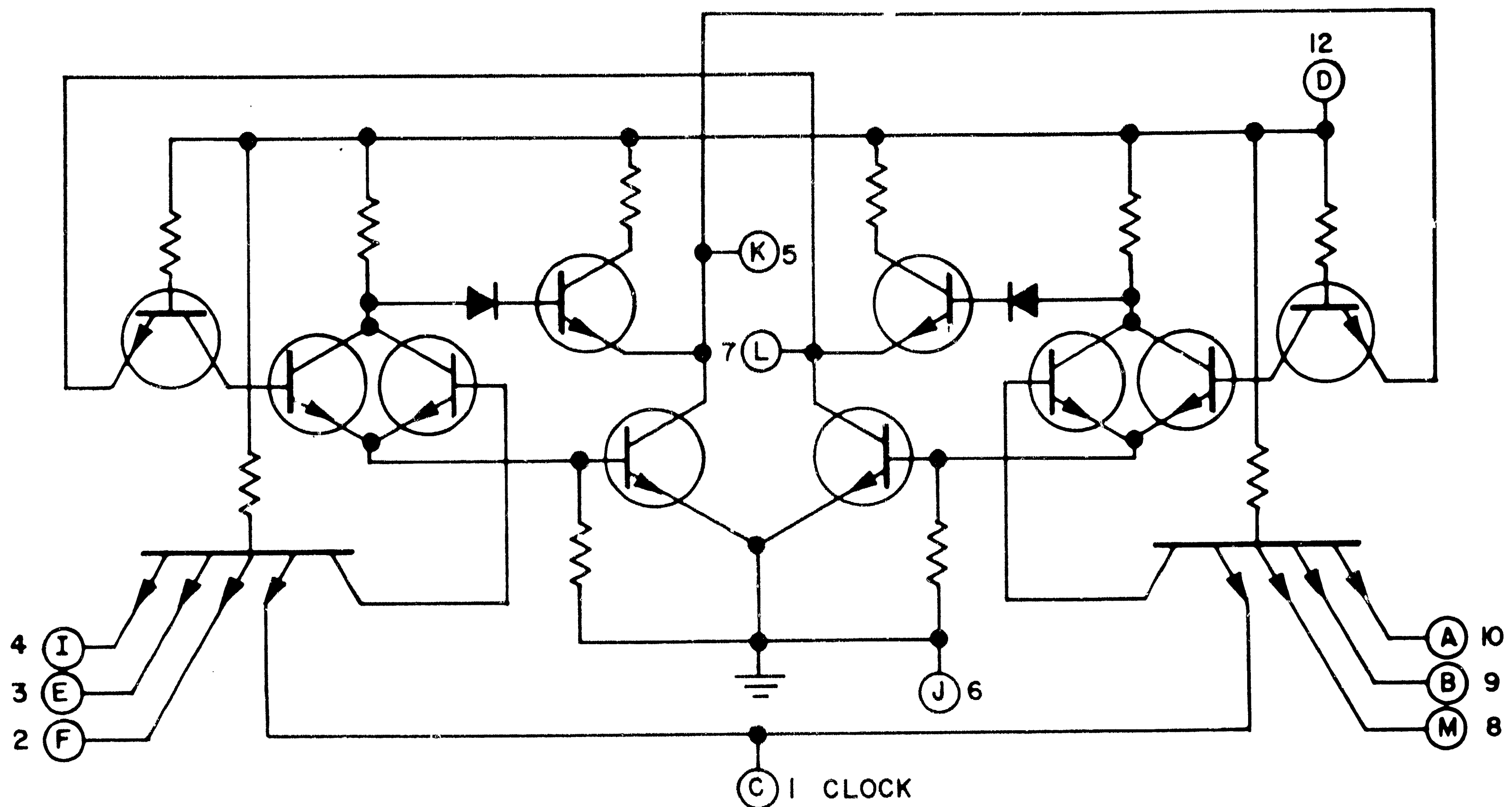
The 90% to 20% reading was much smaller than the 90% to 10% reading.

SNG-20
 Frequency = 6 mc.
 Load = 1 ckt.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C.



SNG-20
 Frequency = 6 mc.
 Load = 6 ckts.
 $V_{cc} = 5.0$ volts
 Temperature = 25°C.





SFF 2A & B

(+) LOGIC

$$\bar{K} = E \cdot F \cdot I \cdot C + L$$

$$\bar{L} = A \cdot B \cdot M \cdot C + K$$

(-) LOGIC

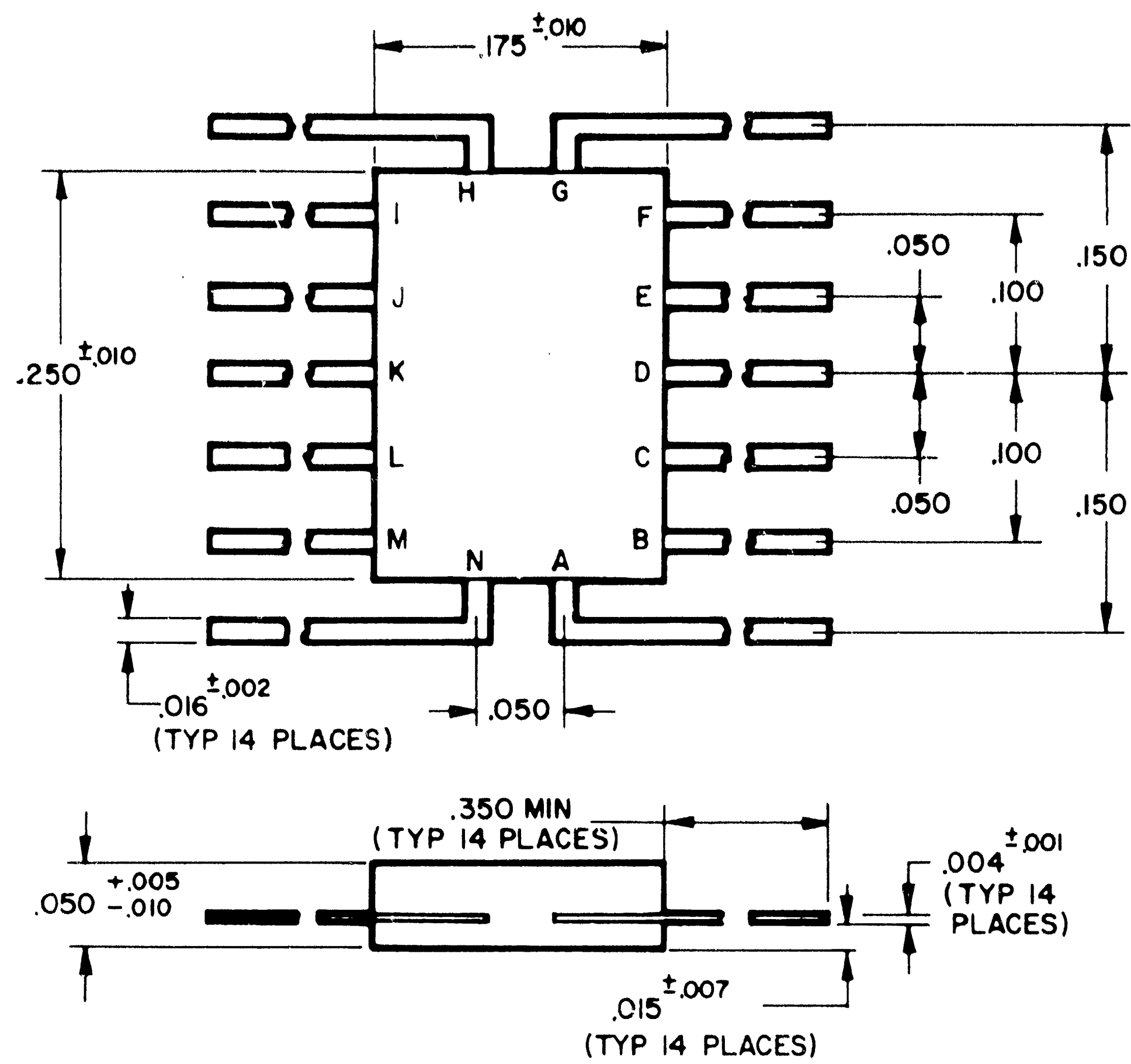
$$K = \bar{E} \cdot \bar{F} \cdot \bar{I} \cdot \bar{C} = \bar{L}$$

$$L = \bar{A} \cdot \bar{B} \cdot \bar{M} \cdot \bar{C} + K$$

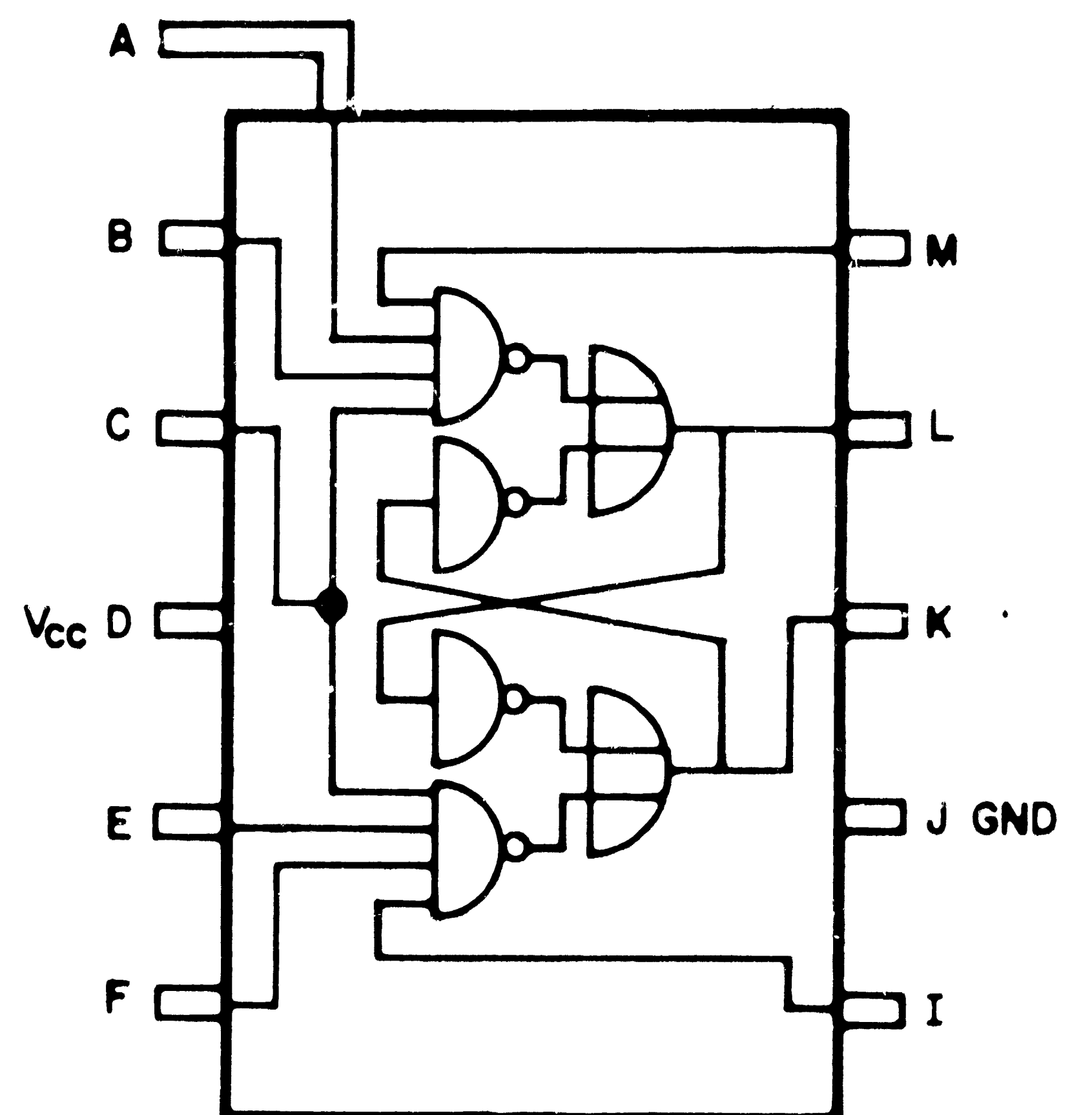
SET-RESET TRIGGER FLIP-FLOP

The SFF-2B set-reset two phase trigger flip-flop is made up of two AND-NOR gates interconnected to operate in the set-reset-trigger flip-flop mode. The circuit is manufactured with planar epitaxial techniques and is constructed on a monolithic silicon substrate.

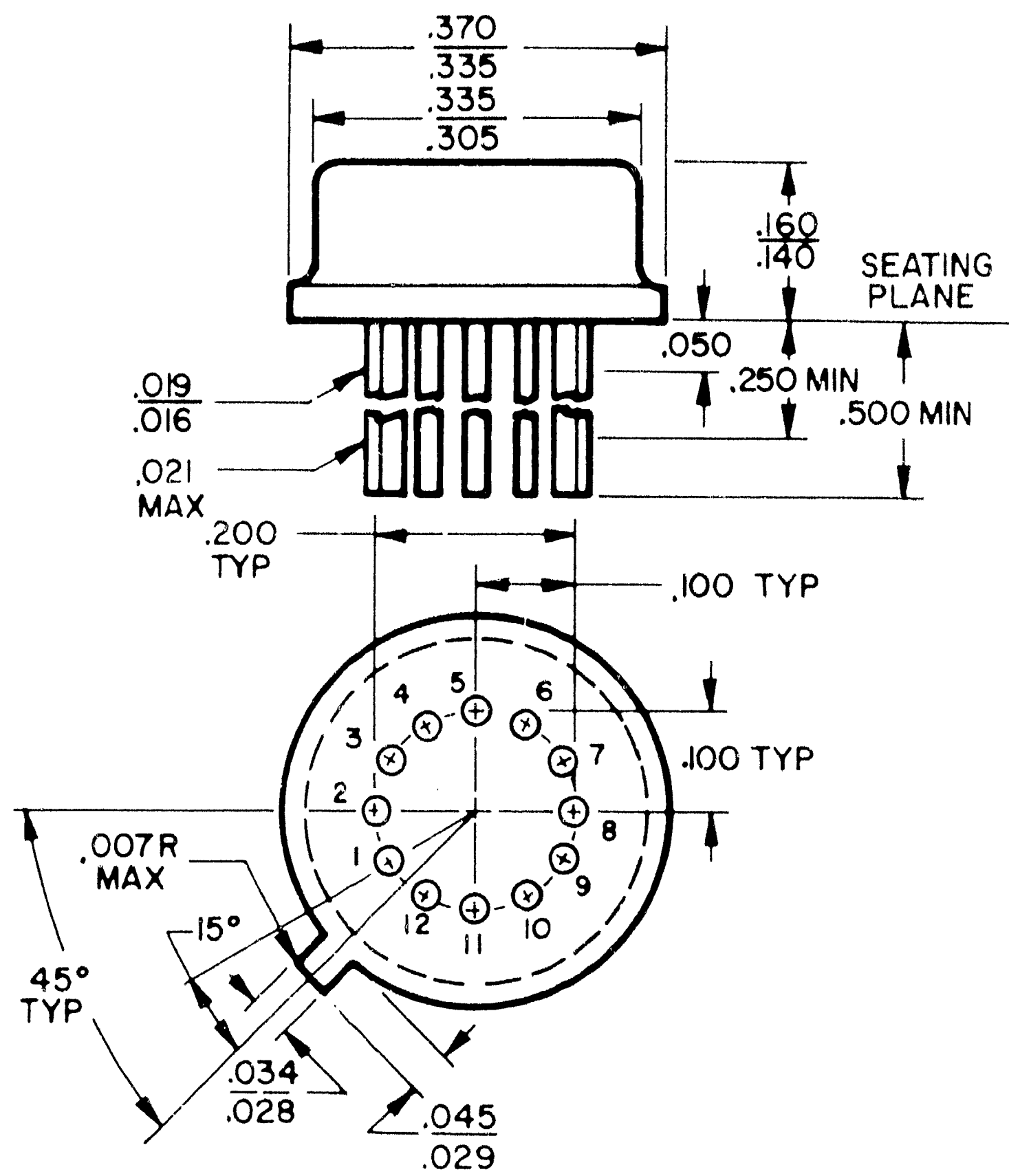
There are two versions of the SFF-2 flip-flop; the "A" version has two inputs on each side, while the "B" version has three inputs on each side. Both of these circuits require only one power supply.



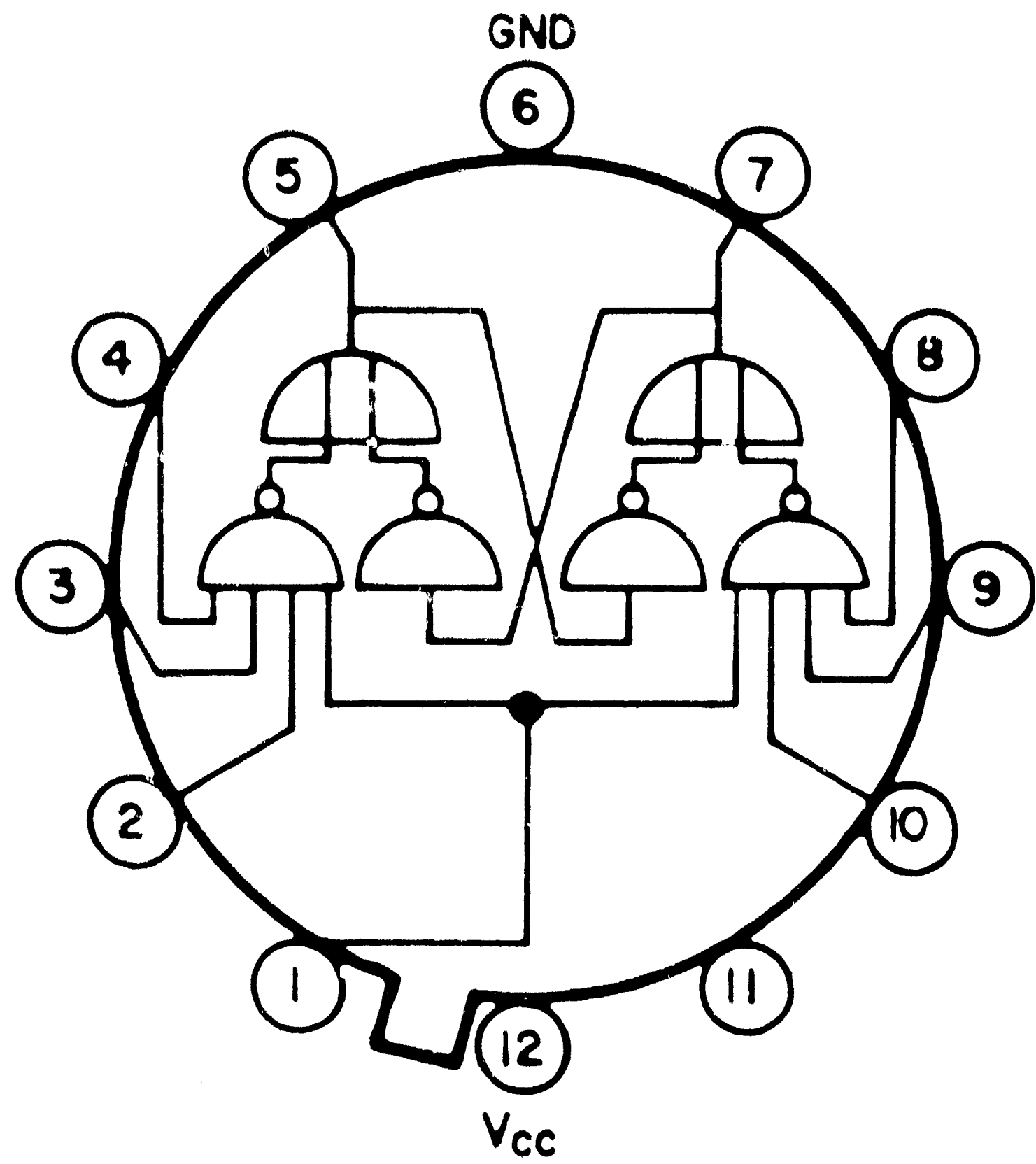
14 LEAD FLAT PACK



TOP VIEW



12 LEAD TO-5



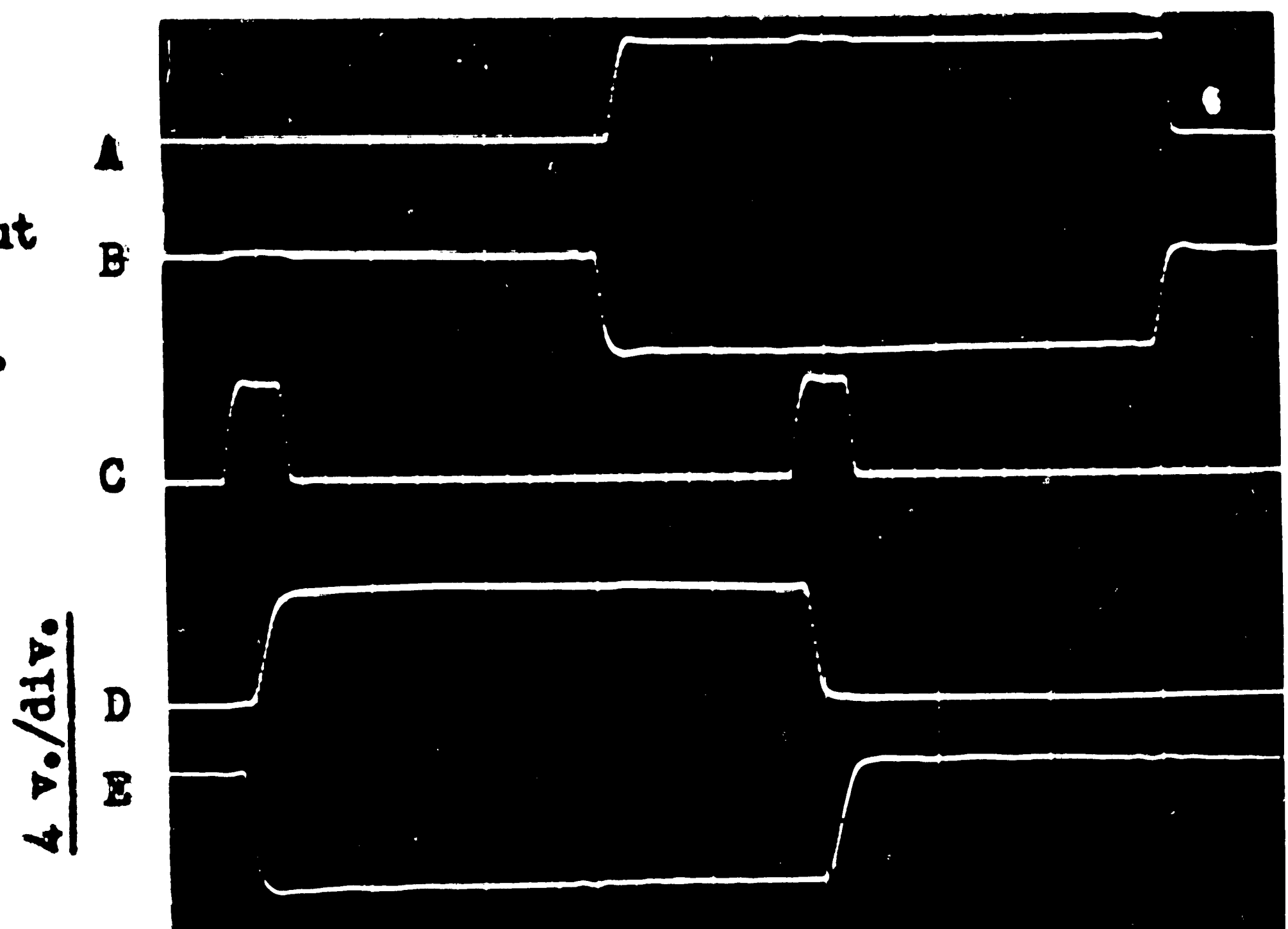
BOTTOM VIEW

SFF - 2B

FOR SFF-2A INPUTS 9-A AND 4-I ARE NOT PRESENT

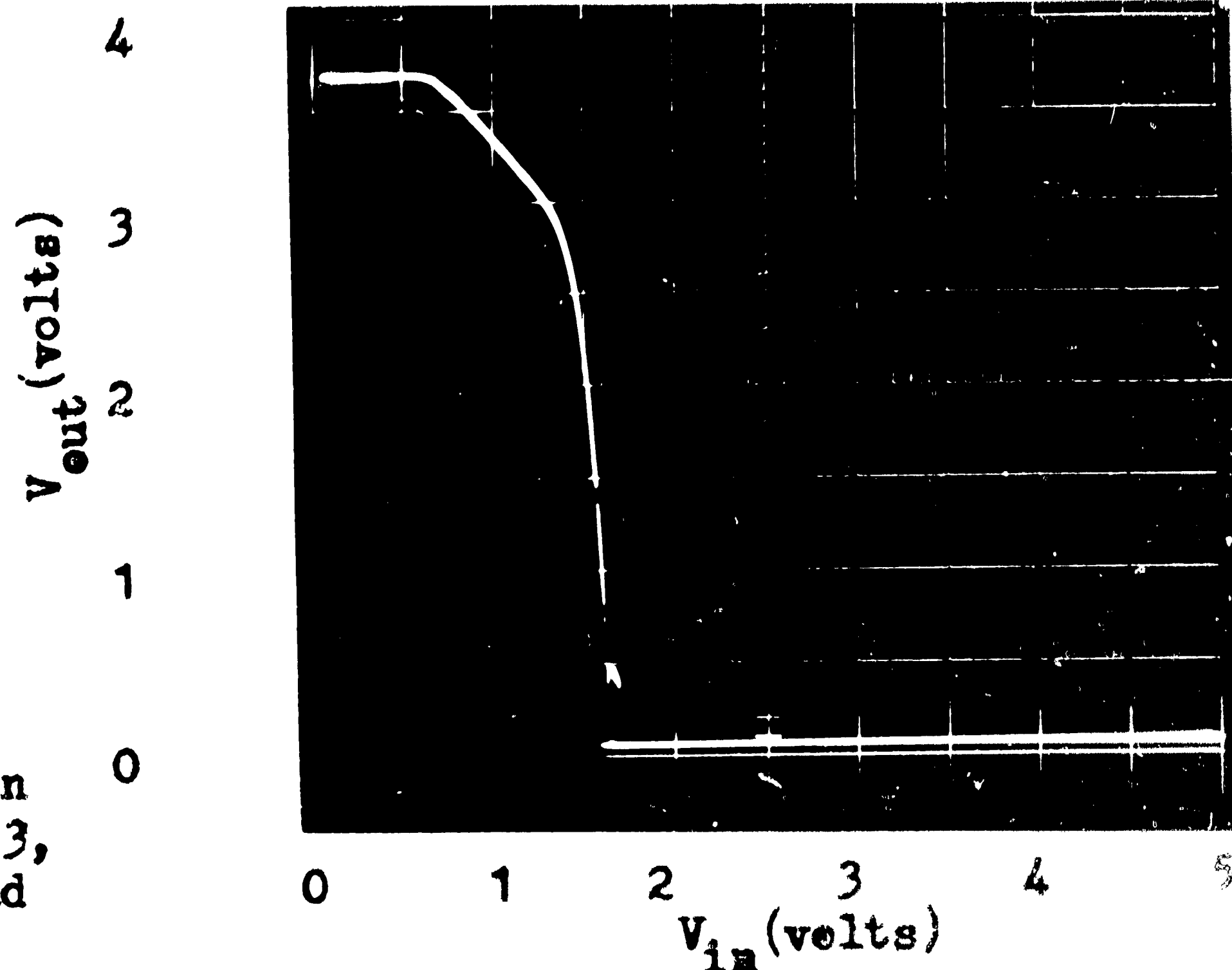
SFF-2B

Input freq. = 1 mc.
Clock freq. = 2 mc.
Load = 1 k Ω /output
 V_{cc} = 5.0 volts
Temperature = 25°C.
A. = #3 input
B. = #9 input
C. = Clock Input
D. = #5 output
E. = #7 output



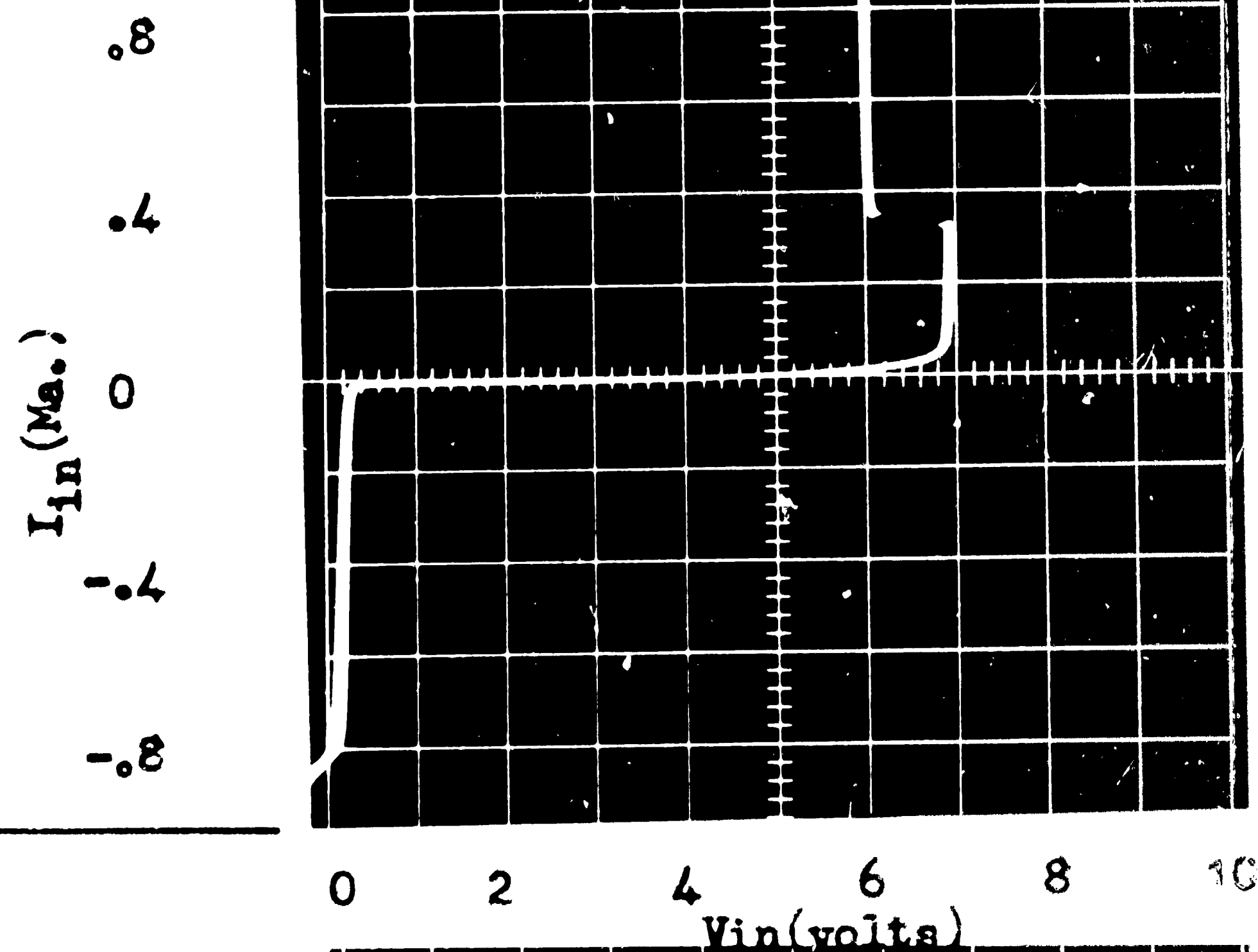
V_{in} vs. V_{out}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) $V_{cc} = 5 \text{ v.}$
- 3.) Output taken on pin #5 with pins #1,2,3, and 4 connected and V_{in} applied to the same.



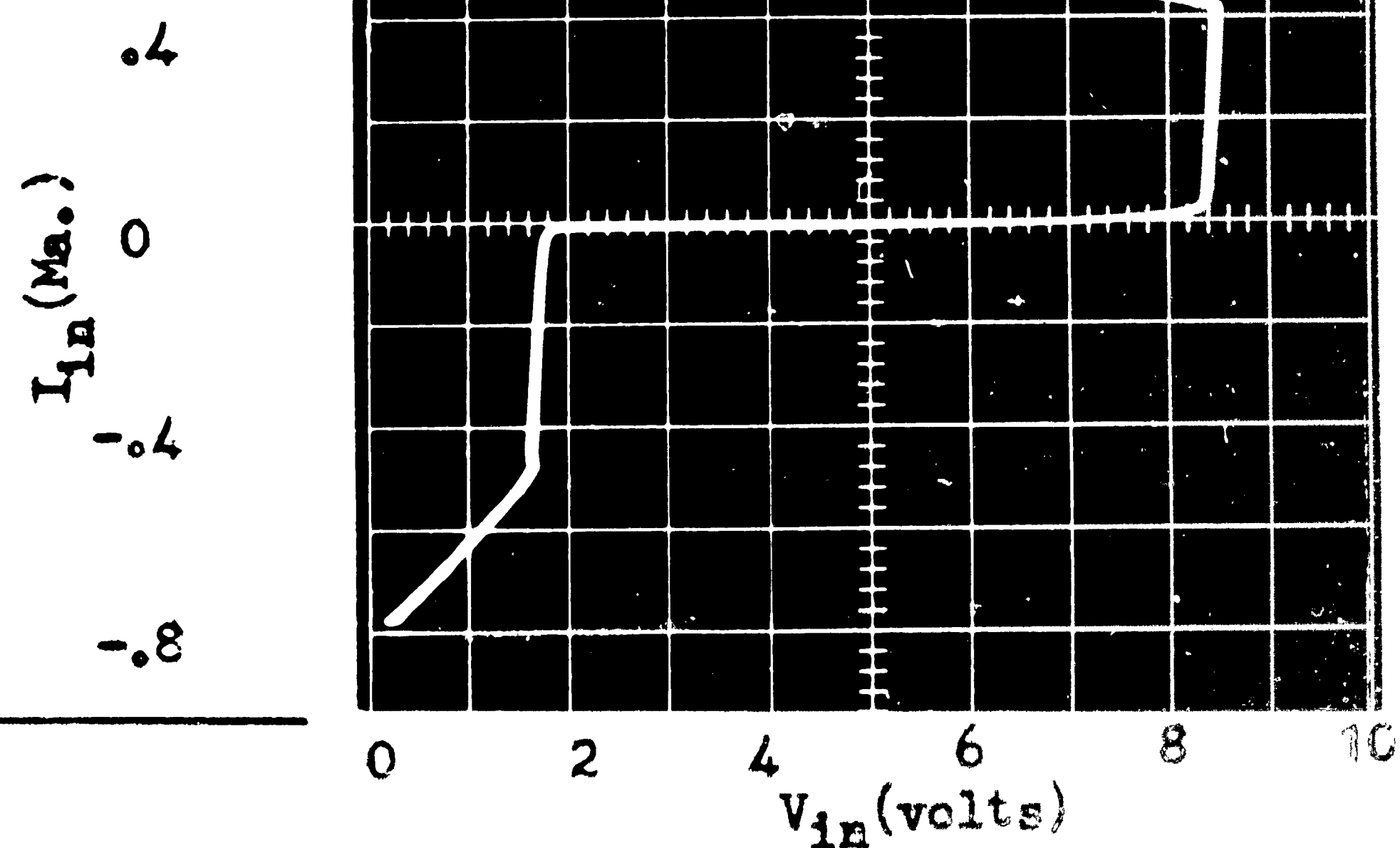
V_{in} vs. I_{in}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) $V_{cc} = 5 \text{ v.}$
- 3.) Pin #1 grounded.



V_{in} vs. I_{in}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) $V_{cc} = 5 \text{ v.}$
- 3.) Pin #1 high.

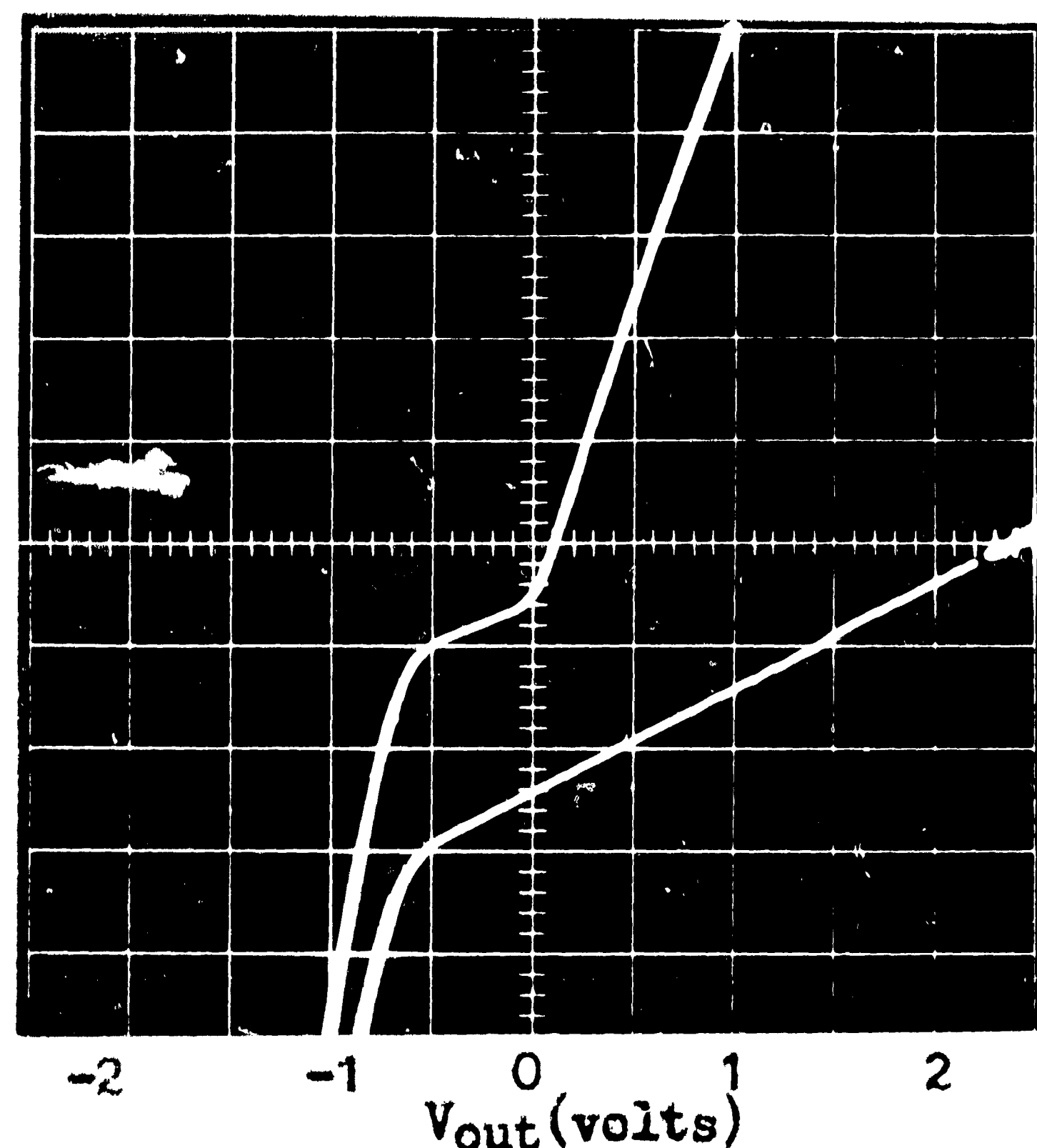


V_{out} vs. I_{out}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) $V_{cc} = 5 \text{ v.}$
- 3.) Top trace is with pin #1 @ ground
bottom trace is with Pin #1 high.

$I_{out}(\text{Ma.})$

40
20
0
-20
-40

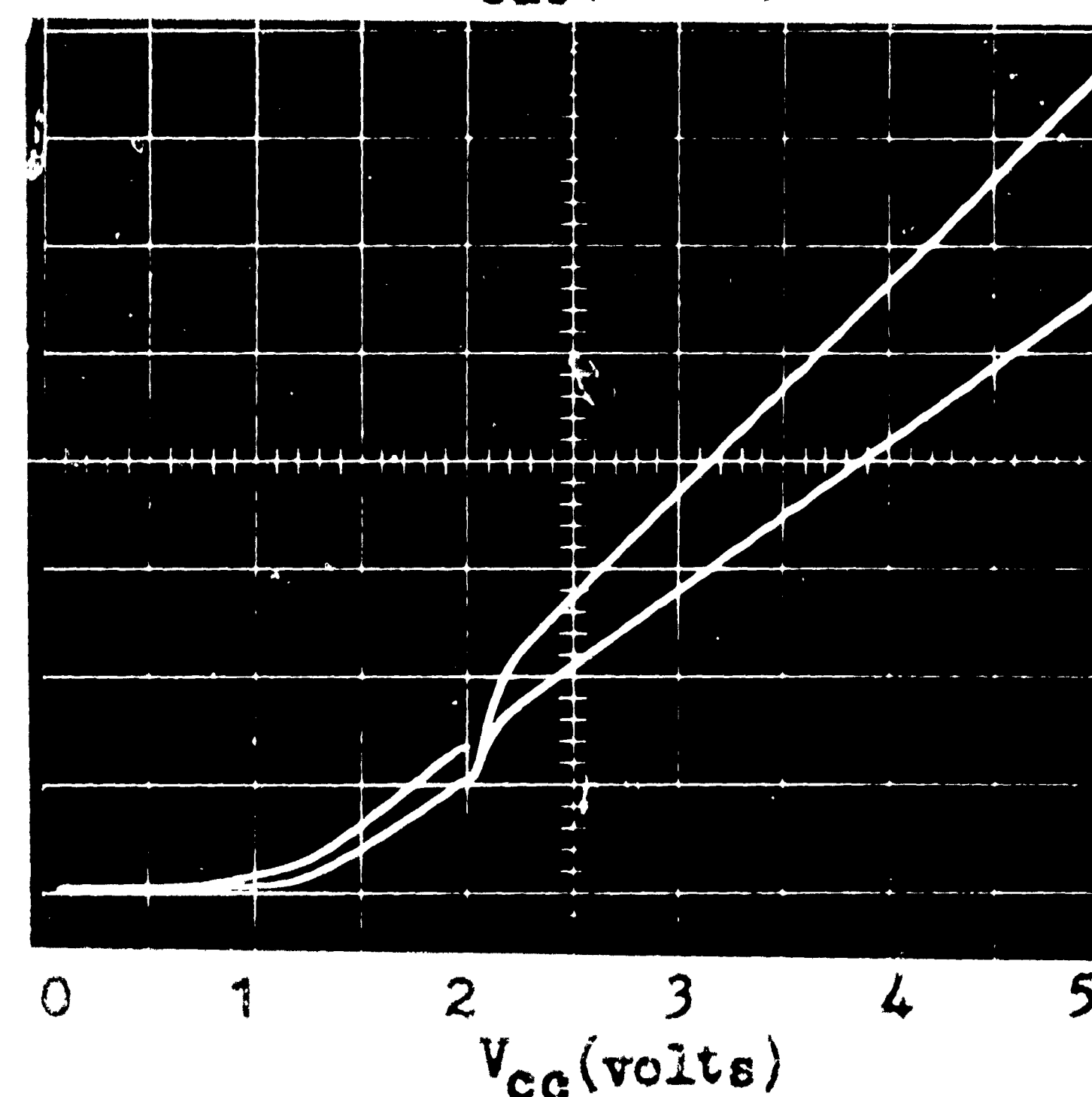


V_{cc} vs. I_{cc}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) Top trace ending with 7.6 ma. is with pins #1,2,3, and 4 high.
Bottom trace ending with 5.6 ma. is with pins #1,2,3, and 4 @ ground.

$I_{cc}(\text{Ma.})$

8
6
4
2
0

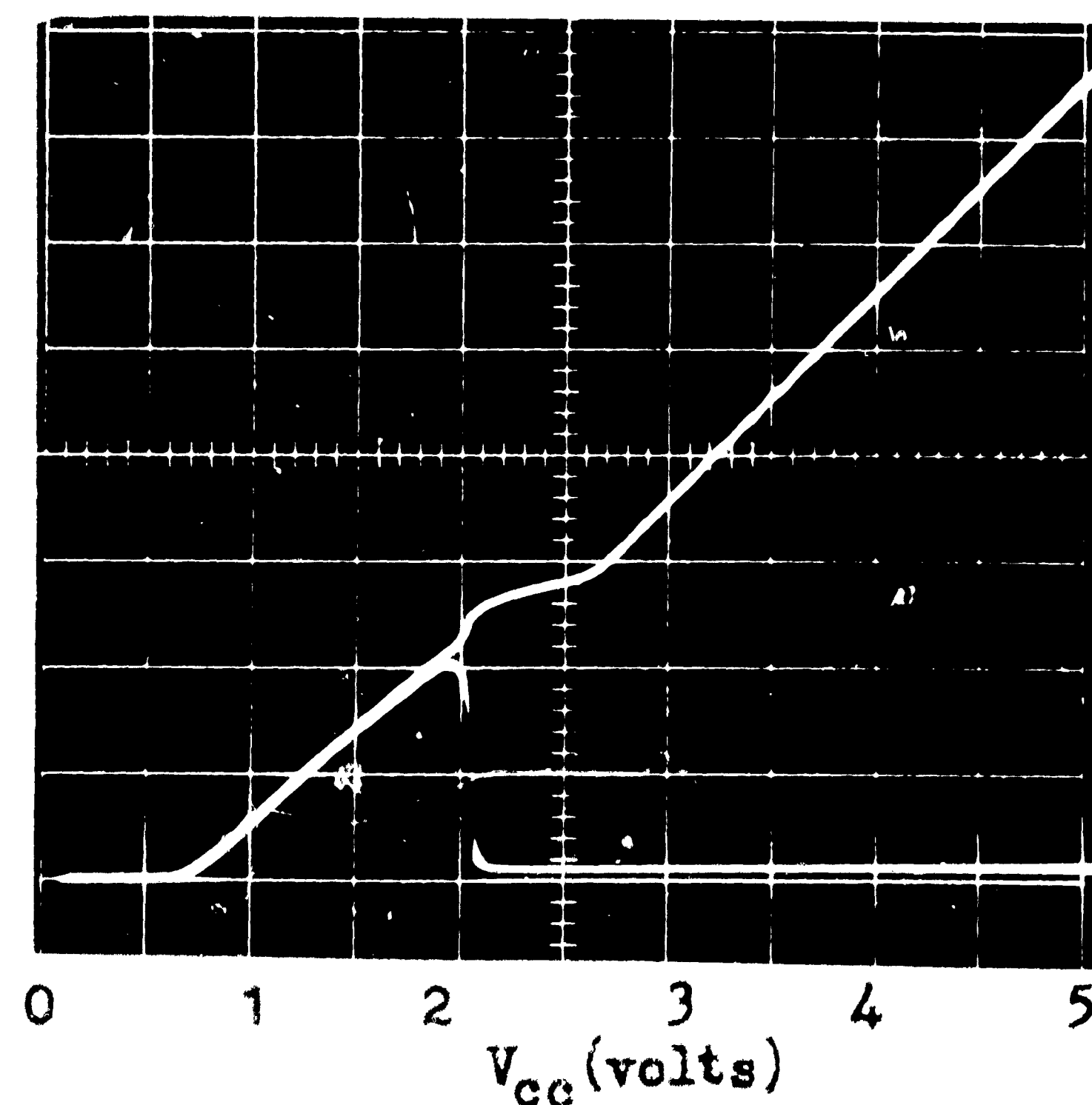


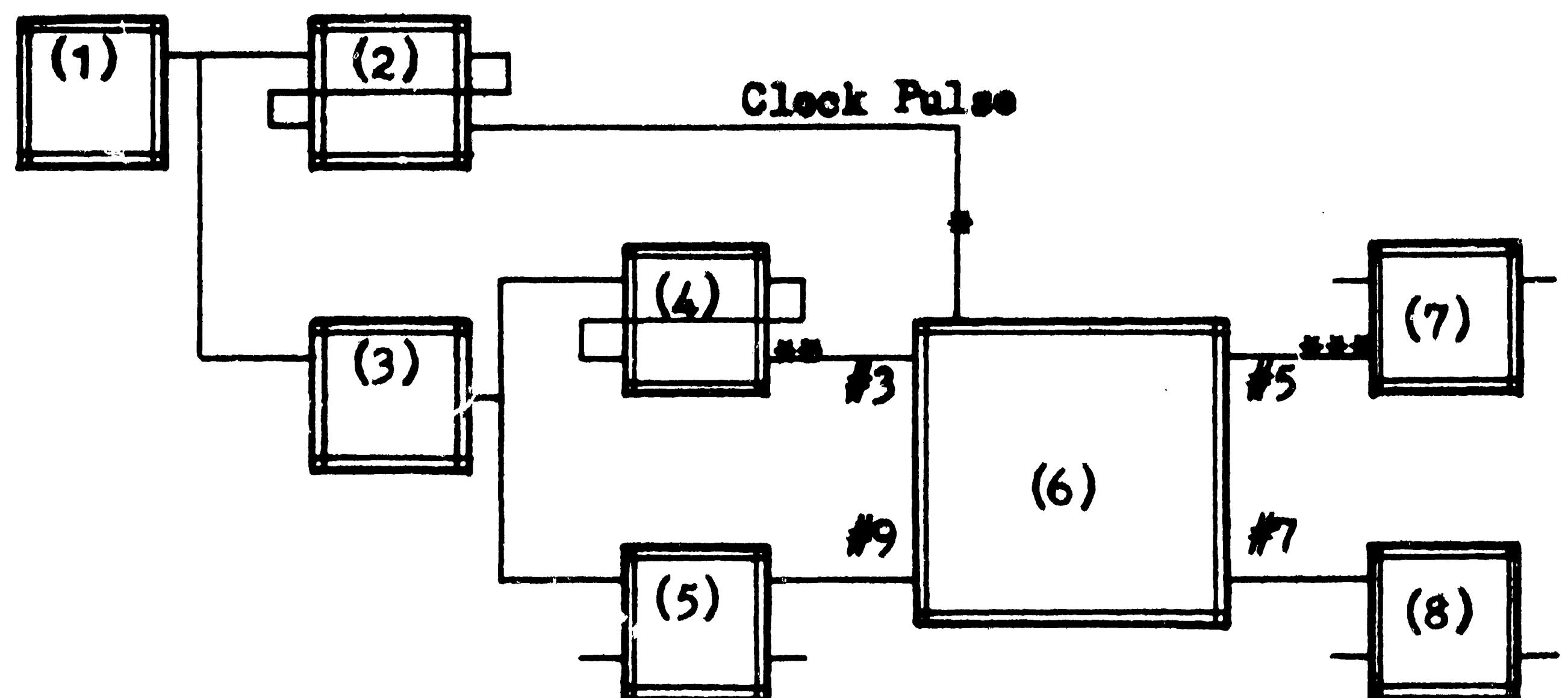
V_{cc} vs. V_{out}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) Top trace is with pin #1 high, and
bottom trace is with pin #1 @ ground.
- 3.) Pin #3 @ ground, and output on pin #5.

$V_{out}(\text{volts})$

4
3
2
1
0





Typical Test Set-up For SFF -2B Flip-Flop

1. Pulse Generator
2. Dual Driver (Clock) SNG-4B
3. Pulse Envelope Generator (Frequency divider)
4. Dual Driver (Input) SNG-4B
5. Driver (Alternate Input) SNG-4B
6. SFF-2B Test Circuit (Flip-Flop)
7. Load = 1 SNG-4B
8. Load = 1 SNG-4B

Clock Frequency = 2 mc.

Logic Inputs = 1 mc.

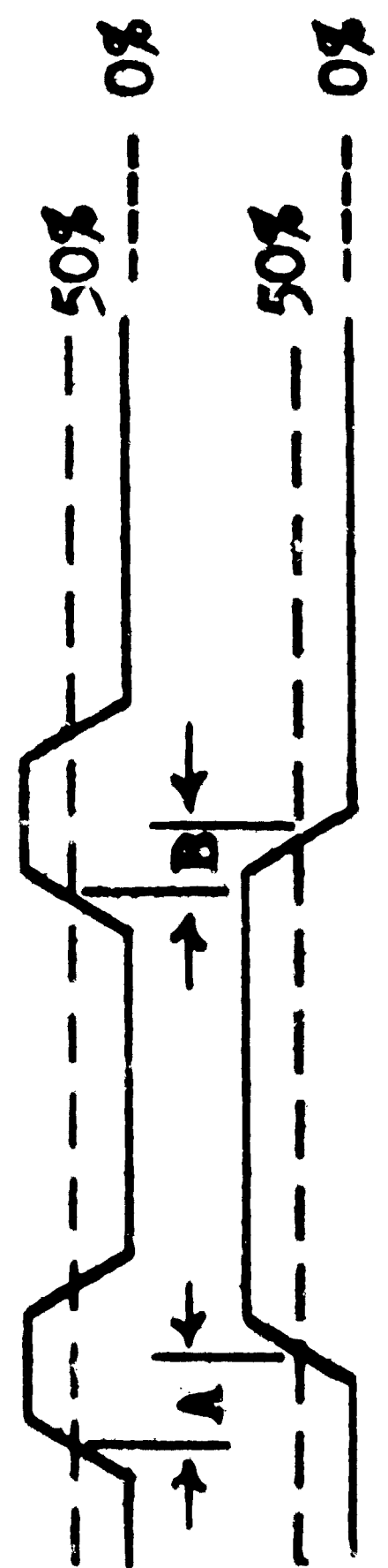
Set-up Drawn Without V_{cc} and Ground For Simplicity.

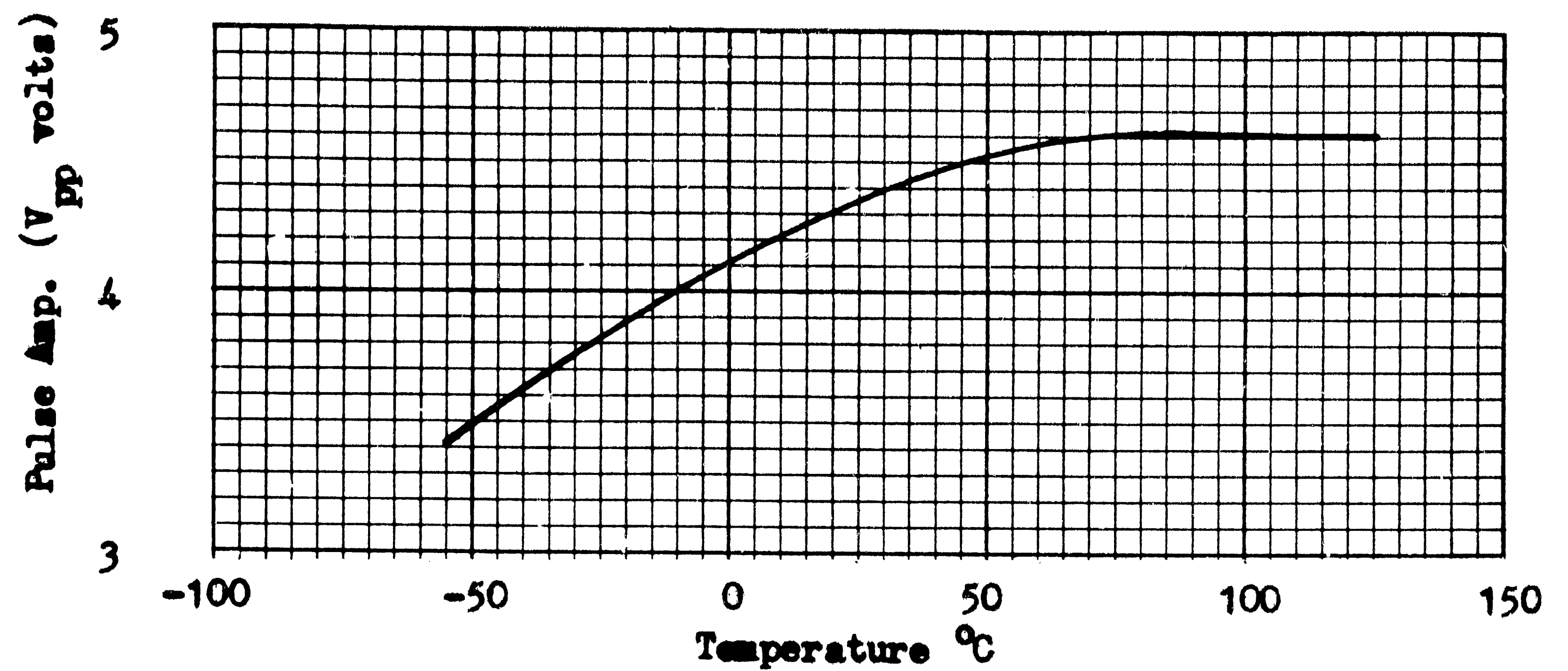
Clock gate, Input gates, Test circuit, and Load circuits were inside of the temperature chamber.

- * Clock Input Monitor
- ** Logic Input Monitor
- *** Logic Output Monitor

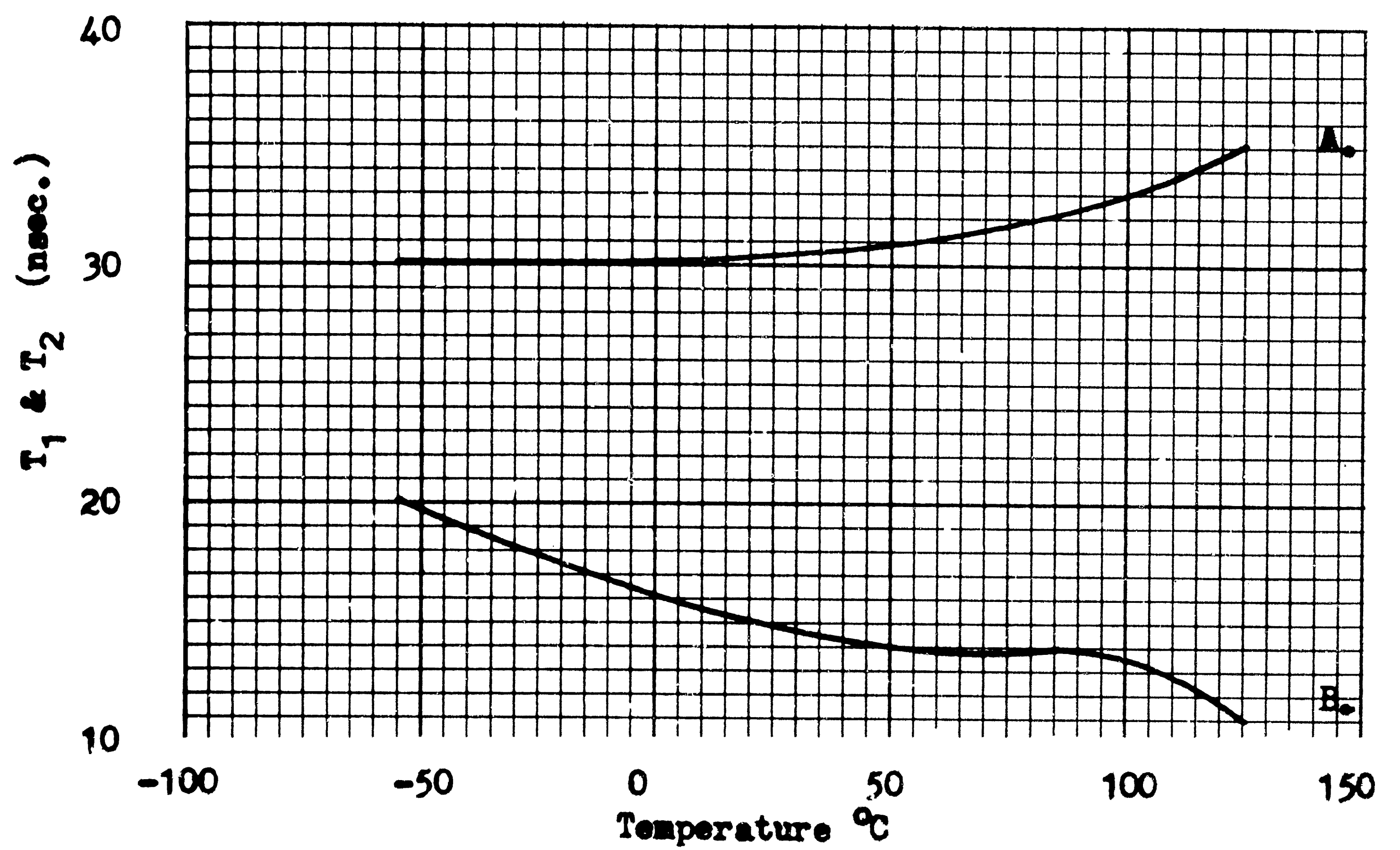
UFF 2B Input = 1 mc. Clock = 2 mc. Fan-in = 1 ckt. Load = 1 ckt./output

Temperature °C	-55				-40				+25				+85				+125			
V _{cc}	4.5	5.0	5.5	5.5	4.5	5.0	5.5	5.5	4.5	5.0	5.5	5.5	4.5	5.0	5.5	5.5	4.5	5.0	5.5	5.5
Input #3	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
Pulse Amp.	2.8	3.3	3.8	3.8	2.8	3.4	3.9	3.9	3.1	3.6	4.1	4.1	3.4	3.8	4.4	4.4	3.5	4.0	4.6	4.6
Pulse Width	497	497	499	499	497	498	499	499	500	500	502	502	500	502	503	504	504	504	507	507
T _r	6.0	8.0	8.0	8.0	7.0	8.0	9.0	9.0	10	11	12	12	15	17	18	20	22	24	24	24
T _f	10	9.0	7.0	7.0	9.0	8.0	6.0	6.0	7.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0
Clock Pulse	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
Pulse Amp.	2.8	3.2	3.6	3.6	2.8	3.2	3.9	3.9	2.9	3.5	3.9	3.9	3.1	3.6	4.1	3.1	3.7	4.1	4.1	4.1
Pulse Width	55	53	51	51	54	52	50	50	51	50	49	49	50	50	49	50	49	48	48	48
T _r	7.0	8.0	8.0	8.0	6.5	7.0	7.0	7.0	9.0	10	11	11	11	12	13	15	16	16	16	16
T _f	12	10	9.0	9.0	10	9.0	7.0	7.0	7.0	7.0	7.0	7.0	6.0	6.0	5.0	7.0	6.0	5.0	5.0	5.0
Output #5	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
Pulse Amp.	2.7	3.4	3.8	3.8	2.8	3.7	4.0	4.0	3.2	4.3	4.6	4.6	3.8	4.6	4.8	3.8	4.6	4.8	4.8	4.8
Pulse Width	492	490	489	489	492	487	486	486	487	486	484	484	480	480	480	480	477	477	477	477
T _r	13	13	14	14	13	13	14	14	20	21	21	21	21	22	23	25	26	27	27	27
T _f	12	12	11	11	12	11	9.0	9.0	12	12	11	11	11	9.0	8.0	10	8.0	8.0	8.0	8.0
T ₁	31	30	26	26	30	30	26	26	33	31	31	31	33	33	31	35	35	33	33	33
T ₂	24	20	15	15	22	19	14	14	20	15	14	14	15	14	10	12	11	9.0	9.0	9.0





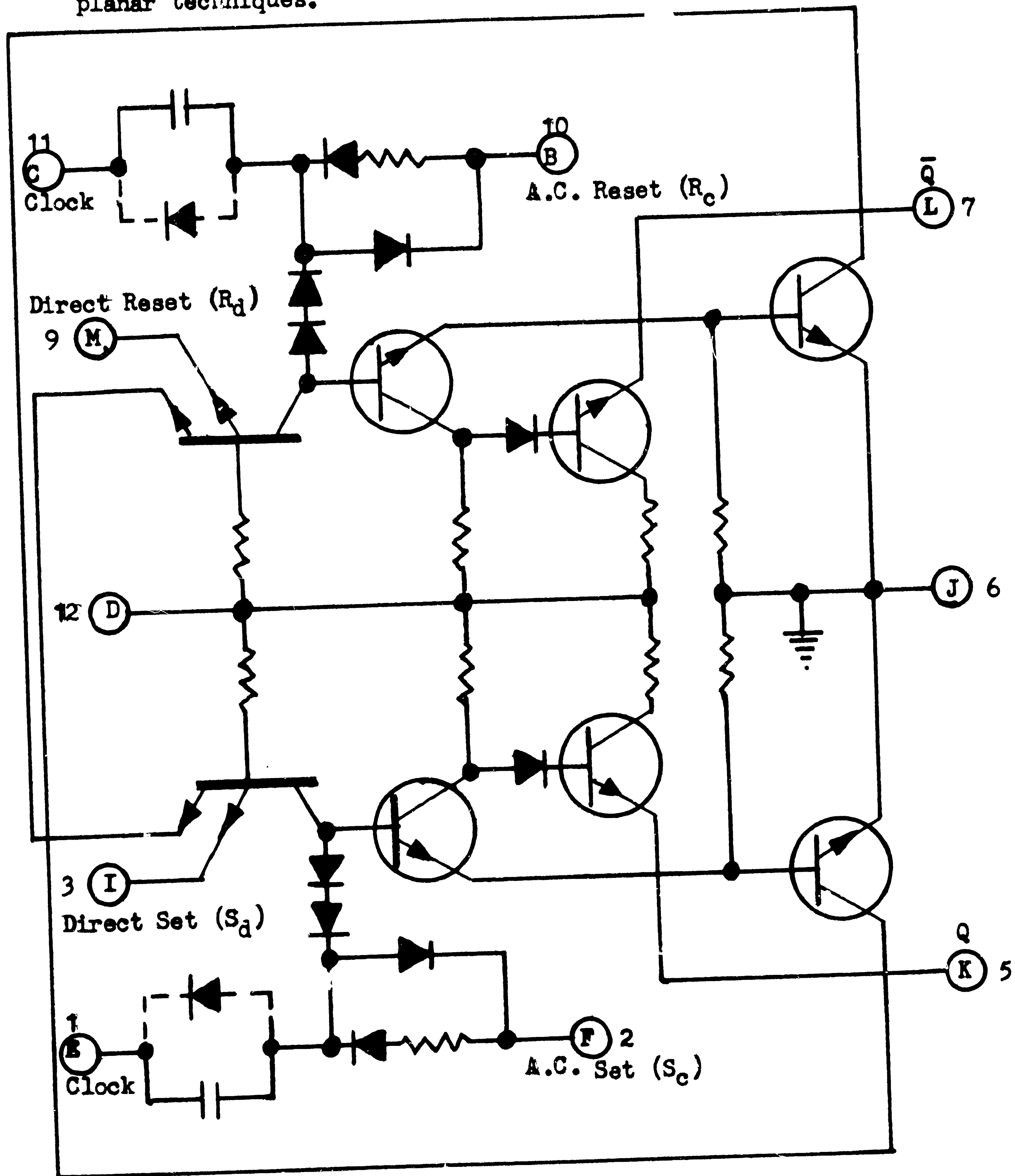
SFF-2B
 Input Frequency = 1 mc.
 Clock Frequency = 2 mc.
 Load = 1 kct./output
 $V_{cc} = 5.0$ volts



SFF-2B
 Input Frequency = 1 mc.
 Clock Frequency = 2 mc.
 Load = 1 kct./output
 $V_{cc} = 5.0$ volts

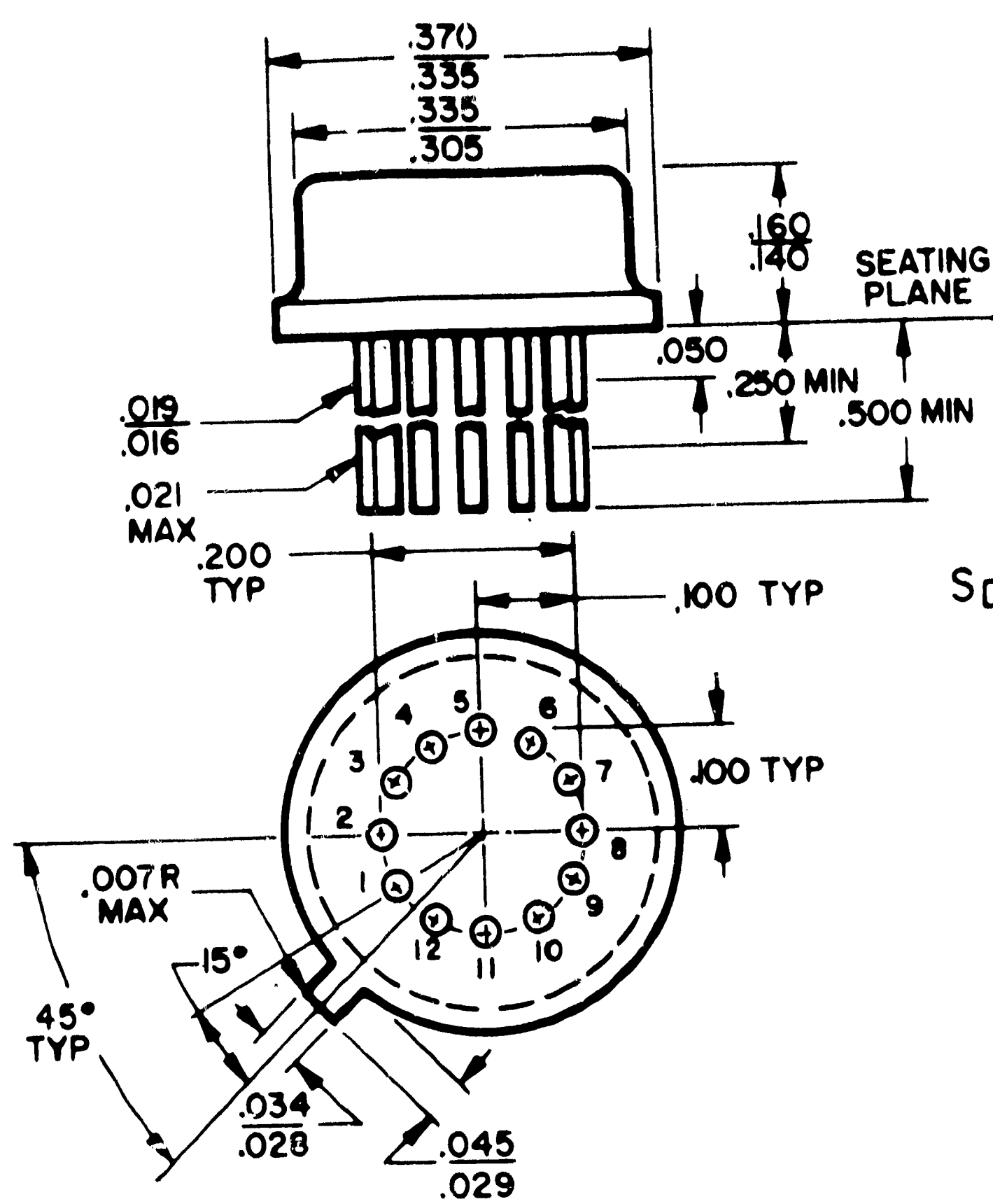
A. = T₁
 B. = T₂

The SFF-3A is a single phase flip-flop constructed on a monolithic silicon substrate and manufactured by epitaxial planar techniques.

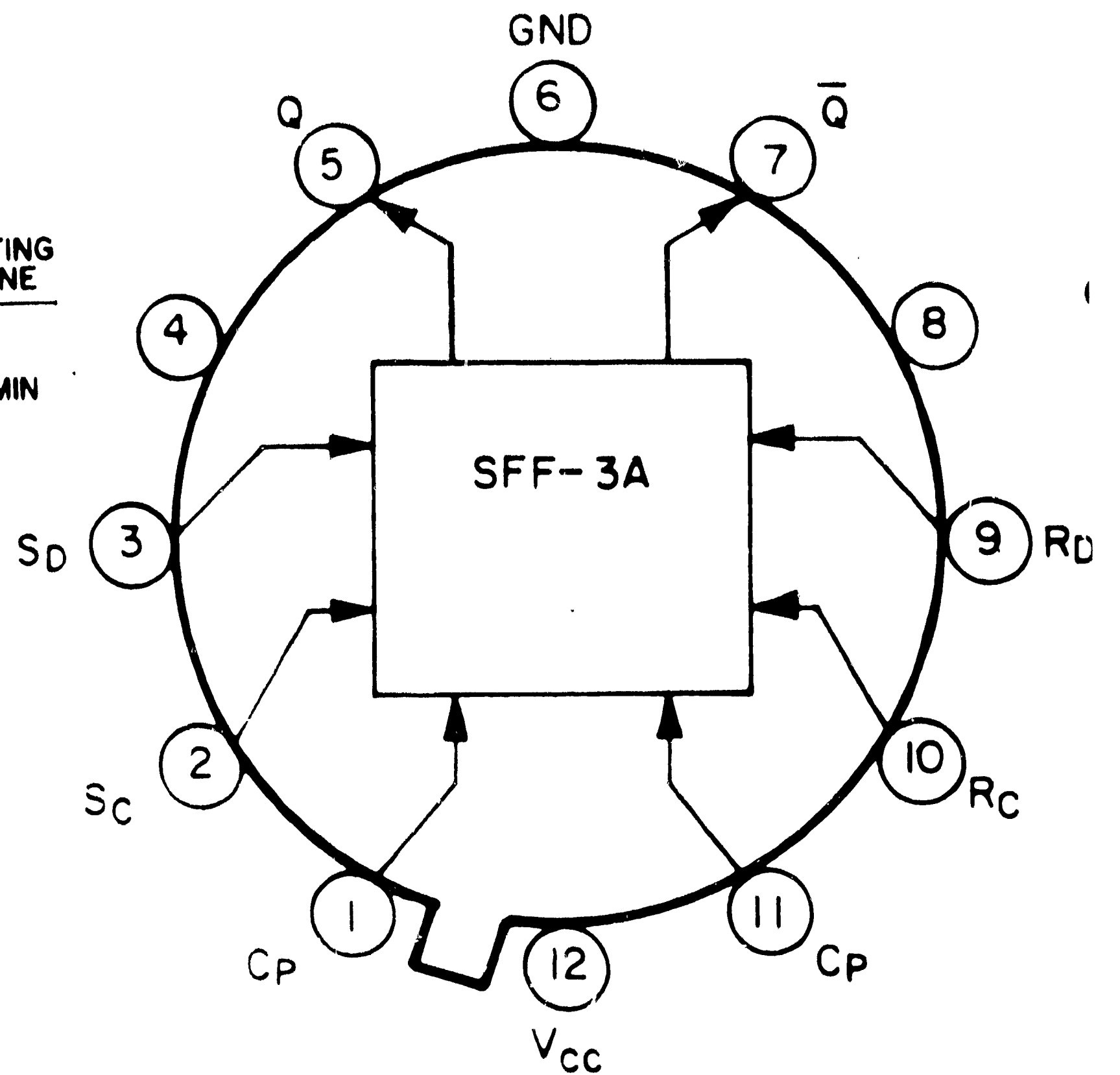


SFF-3A
SET-RESET TRIGGER FLIP-FLOP

Circuit operation requires a single power supply of 8.0 v. max.

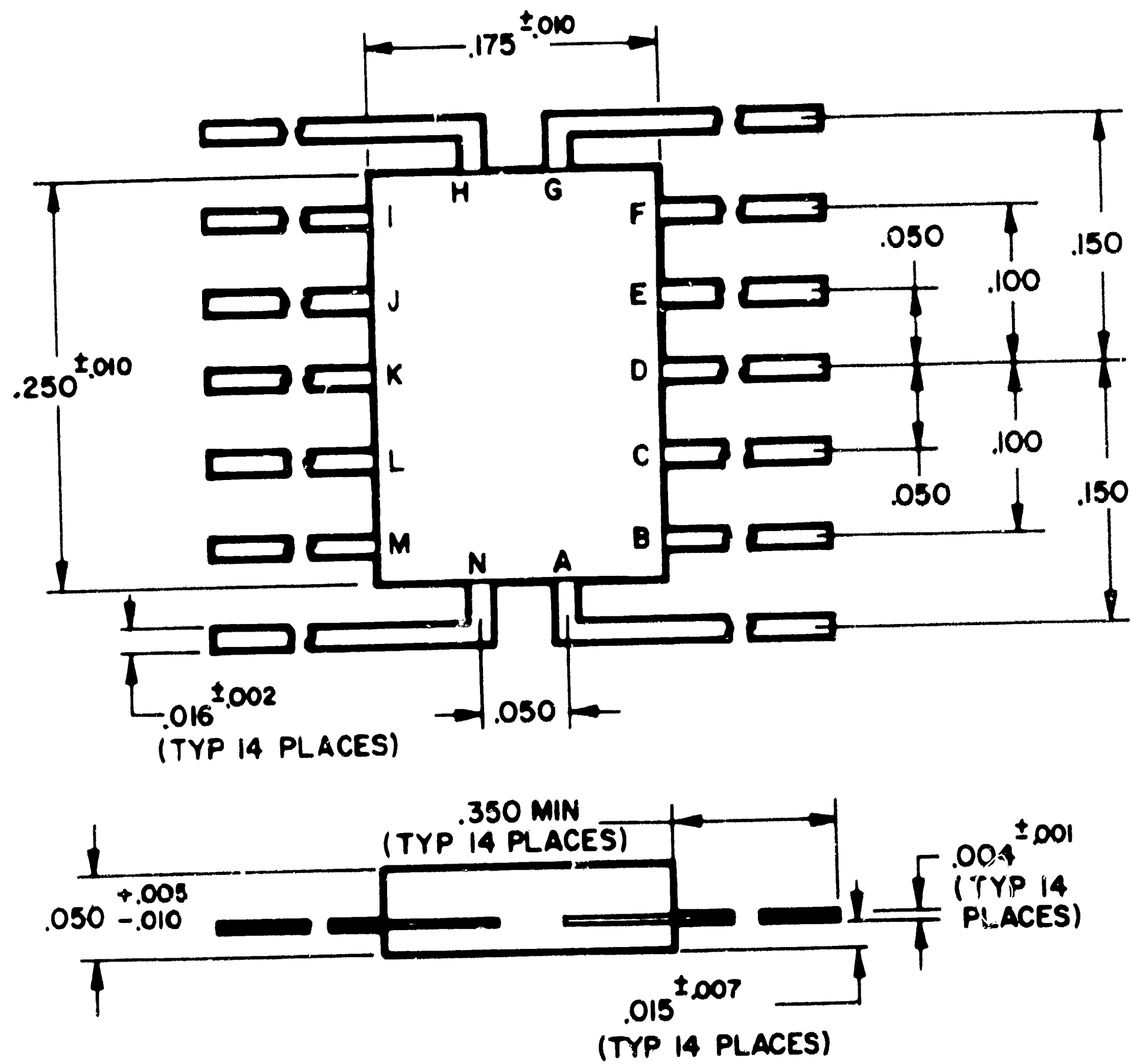


12 LEAD TO-5



TO-5 BOTTOM VIEW

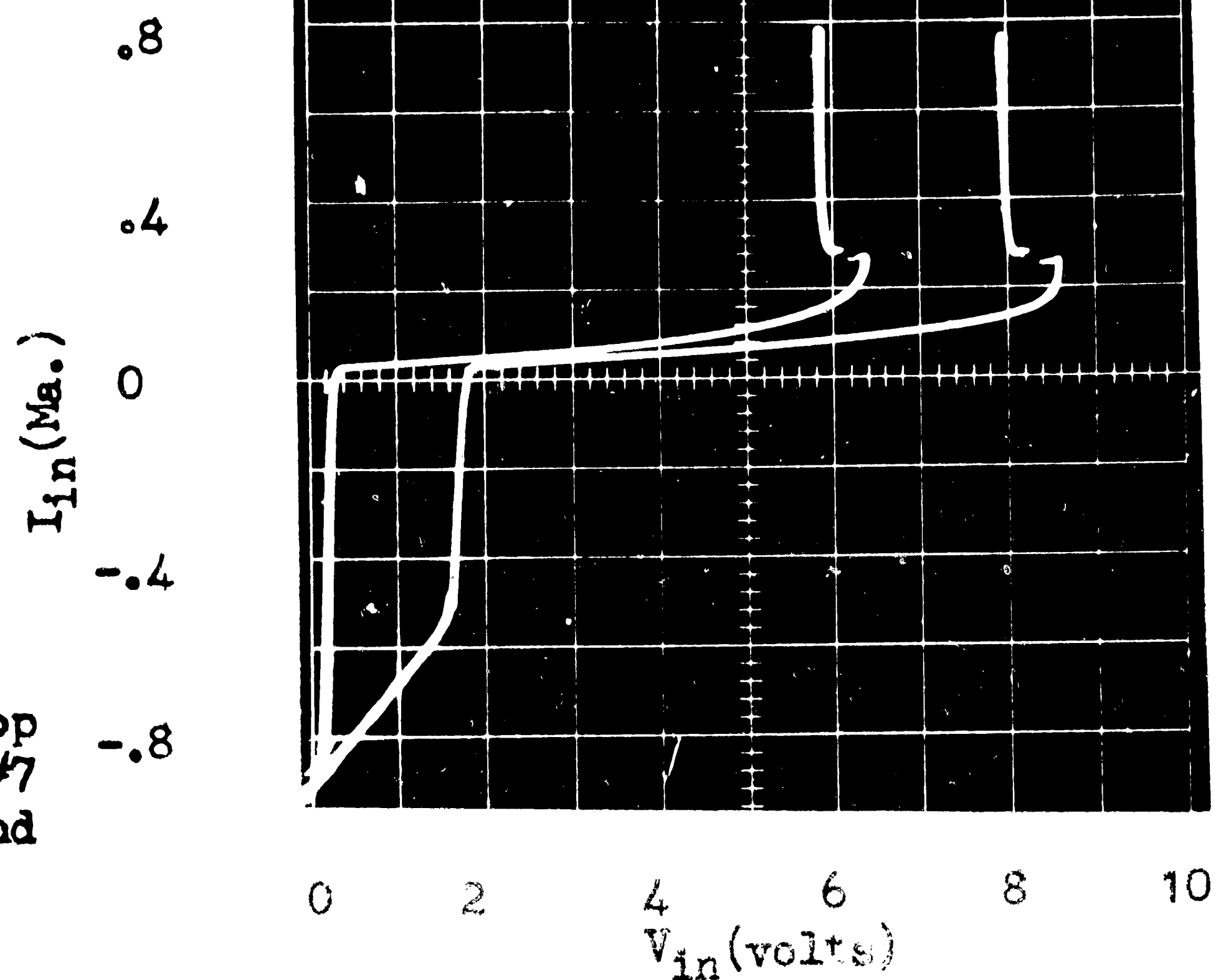
The circuit consists of a dual Nand/Nor element with reactance coupled pulse level trigger inputs interconnected to operate in the set-reset-trigger flip-flop mode.



14 LEAD FLAT PACK

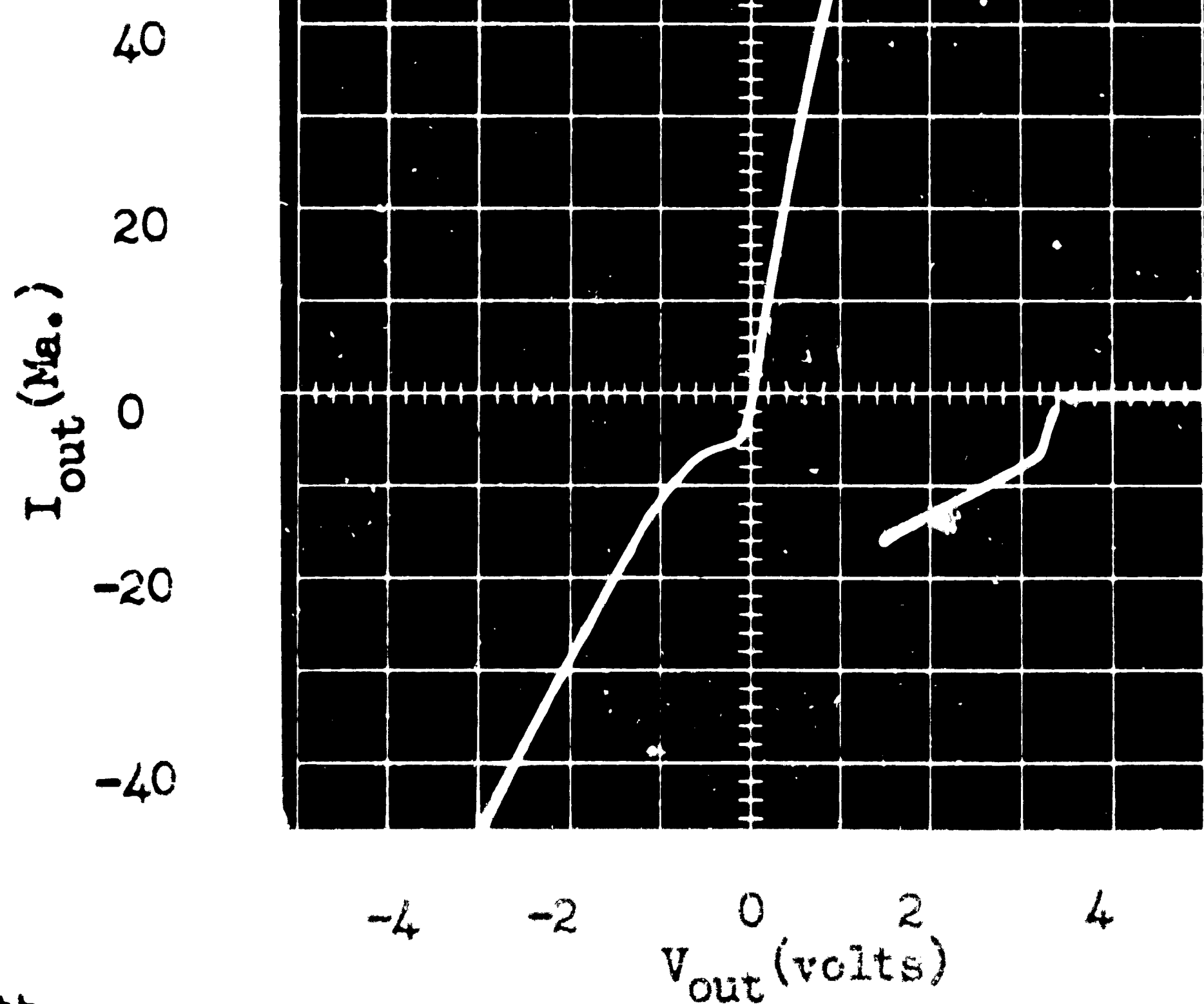
V_{in} vs. I_{in}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) $V_{cc} = 5 \text{ v.}$
- 3.) The left-hand or top trace is with pin #7 high. The right-hand or bottom trace is with pin #7 low.



V_{out} vs. I_{out}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) $V_{cc} = 5 \text{ v.}$
- 3.) The left-hand or top trace is with the output transistor "on", and the right-hand or bottom trace is with the output transistor "off".

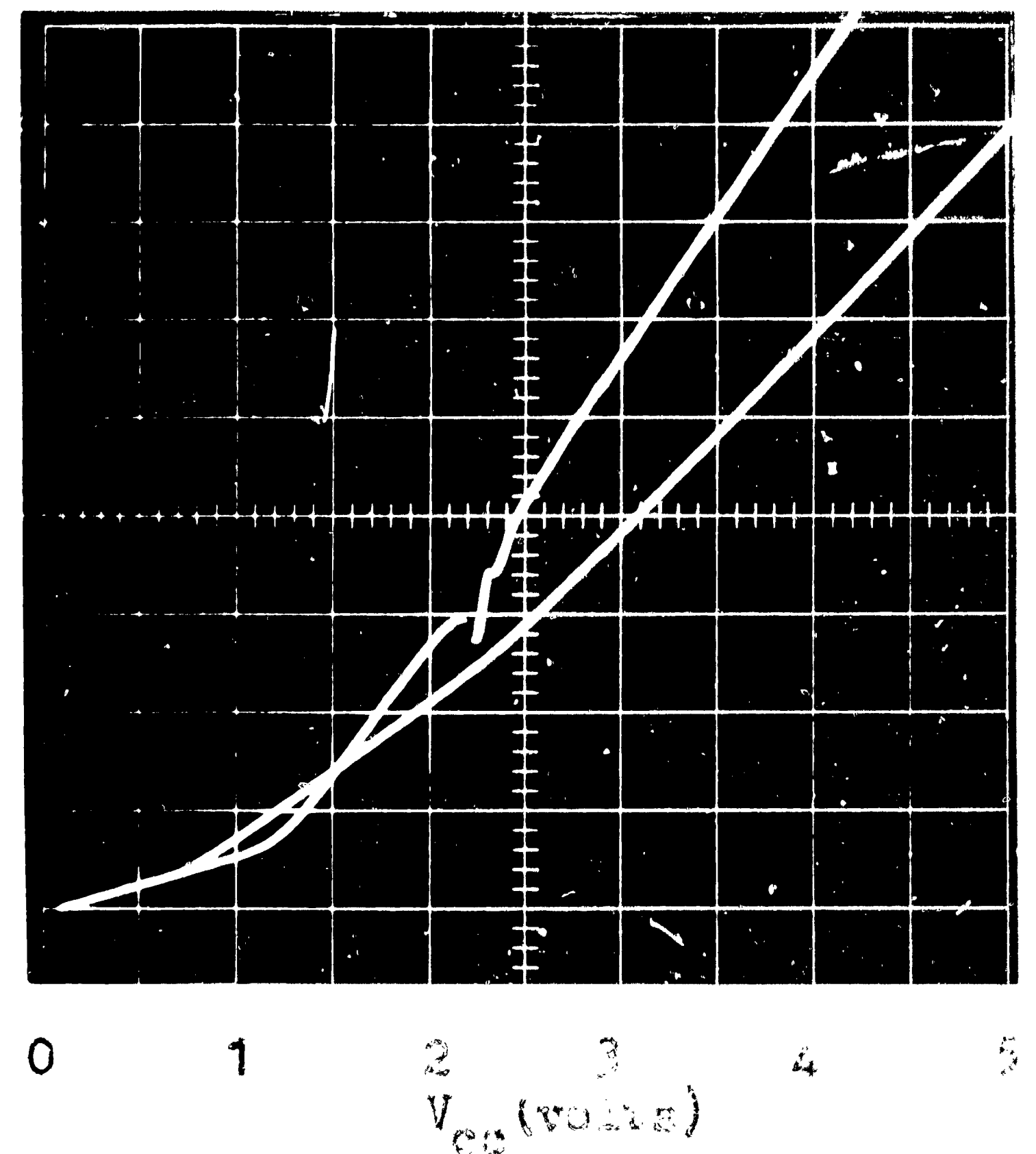


V_{cc} vs. I_{cc}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) Pins #1 & #11 @ ground for both traces.
- 3.) Top trace with pins #9 & #3 open, and bottom trace with pins #9 & #3 at ground level.

I_{cc} (Ma.)

4
3
2
1
0

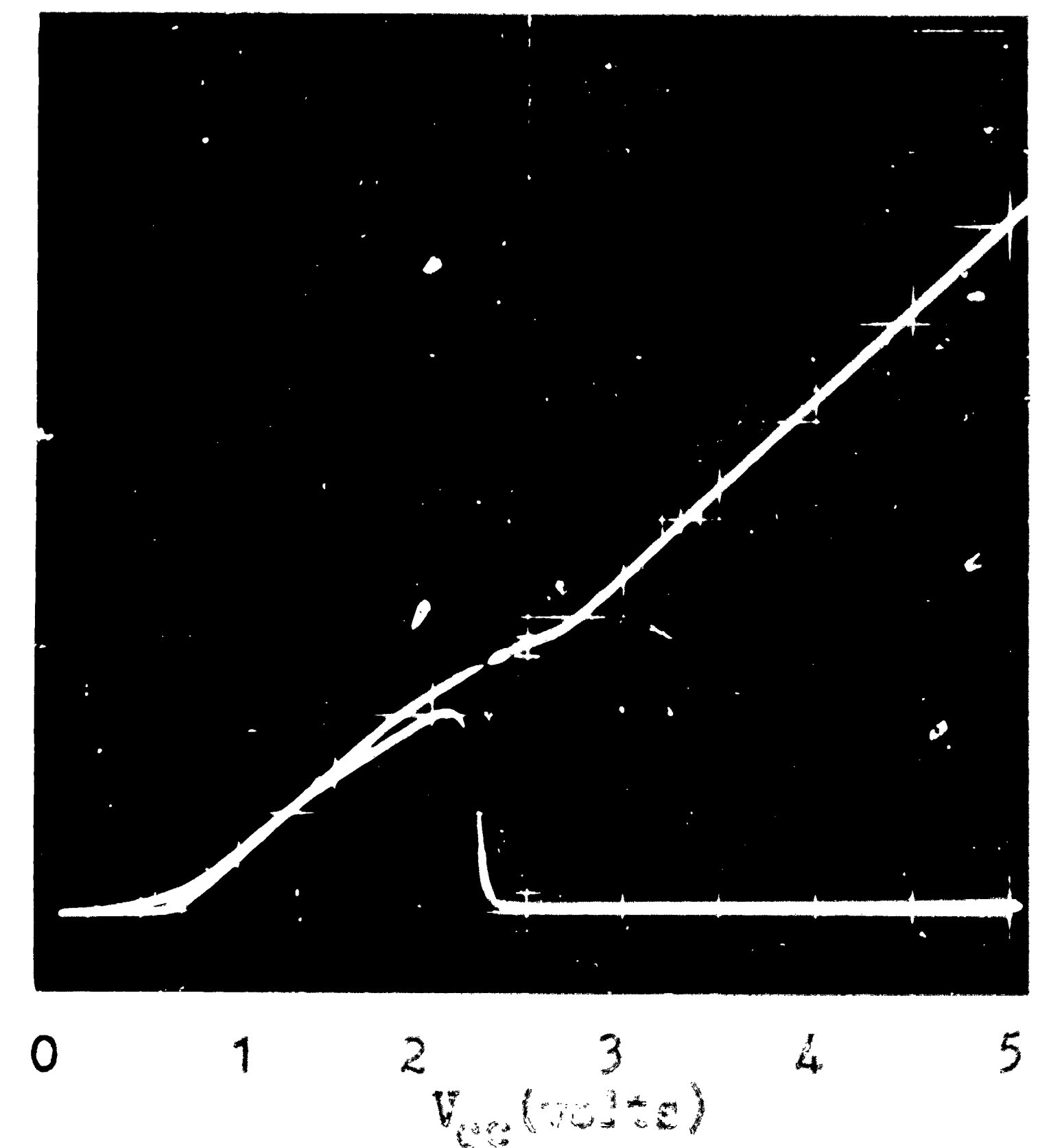


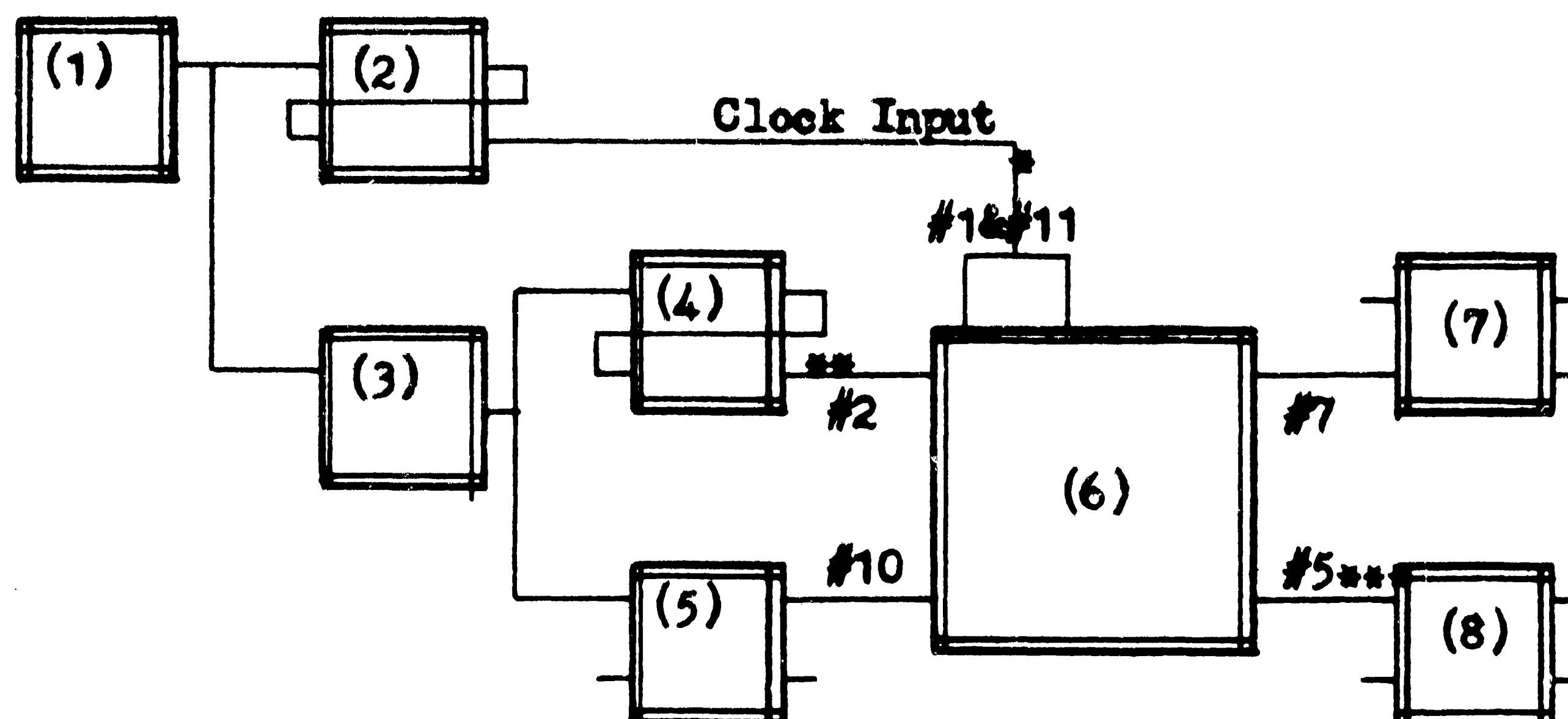
V_{cc} vs. V_{out}

- 1.) $T = 25^{\circ}\text{C}$
- 2.) Pins #1 & #11 at ground for both traces.
- 3.) Top trace with pins #7 & #10 grounded, and bottom trace with pins #2 & #5 grounded.

V_{out} (volts)

4
3
2
1
0





Typical Test Set-up For SFF -3A Flip-Flop

1. Pulse Generator
2. Dual Driver (Clock) SNG-4B
3. Pulse Envelope Generator (Frequency divider)
4. Dual Driver (Input) SNG-4B
5. Driver (Alternate Input) SNG-4B
6. SFF-3A Test Circuit (Flip-Flop)
7. Load = 1 SNG-4B
8. Load = 1 SNG-4B

Clock Frequency = 2 mc.

Logic Inputs = 1 mc.

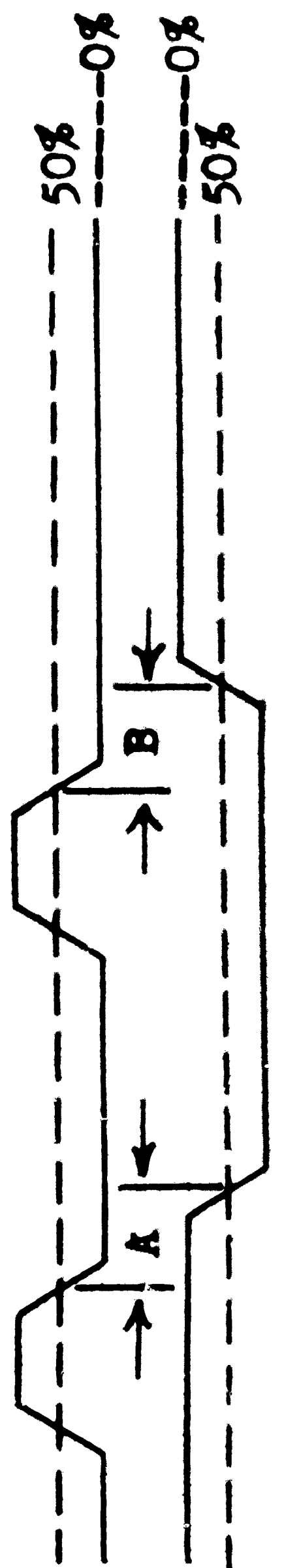
Set-up drawn without V_{cc} and ground for simplicity.

Clock gate, input gate, test circuit, and load circuits were inside of the temperature chamber.

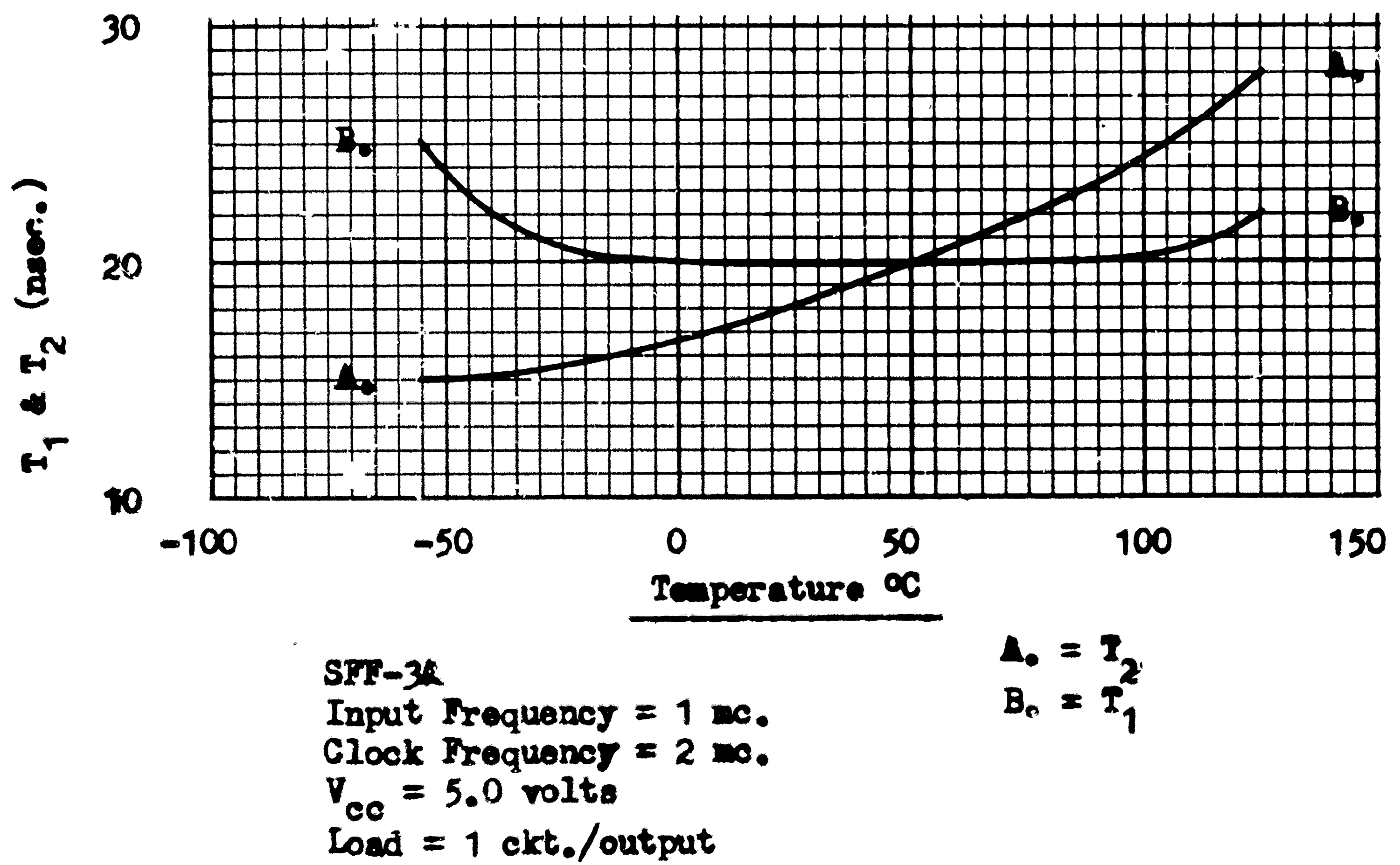
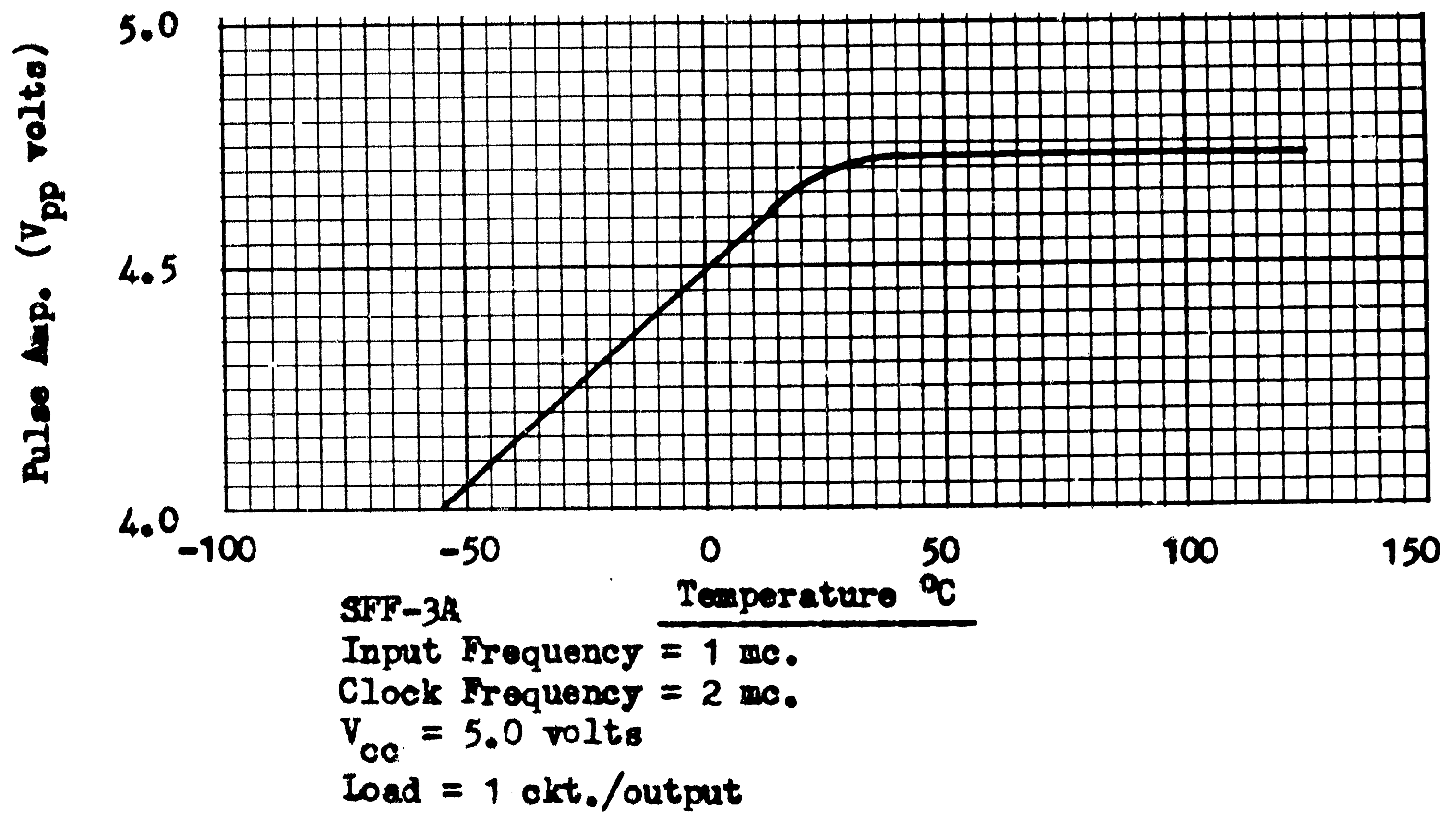
- * Clock Input Monitor
- ** Logic Input Monitor
- *** Logic Output Monitor

SFF 3A Input = 1 mc. Clock = 2 mc. Fan-in = 1 Load = 1 ckt./output

Temperature °C	-55			-40			+25			+85			+125		
V _{cc}	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5
Input #2	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
Pulse Amp.	2.7	3.2	3.7	2.8	3.2	3.8	3.0	3.6	4.1	3.2	3.7	4.3	3.4	3.9	4.5
Pulse Width	506	503	502	506	503	502	503	502	502	502	502	500	500	499	497
T _r	5.0	6.0	7.0	5.5	6.0	7.0	8.0	9.0	11	13	14	16	17	20	21
T _f	9.0	7.0	6.0	9.0	6.0	5.0	6.0	5.0	5.0	6.0	5.0	5.0	6.0	6.0	6.0
Clock	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
Pulse Amp.	2.2	2.7	3.3	2.3	2.8	3.3	2.3	3.1	3.5	2.7	3.2	3.6	2.8	3.2	3.7
Pulse Width	51	49	48	51	49	49	50	50	49	50	50	49	51	49	48
T _r	12	14	17	12	15	17	17	19	22	23	24	28	27	30	32
T _f	8.0	7.0	7.0	8.0	6.0	6.0	6.0	6.0	6.0	7.0	6.0	6.0	6.0	6.0	6.0
Output #5	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
Pulse Amp.	3.3	4.0	4.7	3.5	4.2	4.9	4.2	4.7	5.2	4.2	4.7	5.2	4.2	4.7	5.3
Pulse Width	484	489	492	488	492	494	495	498	501	502	504	507	506	509	511
T _r	14	14	17	15	17	19	23	23	24	28	29	30	34	36	37
T _f	9.0	8.0	8.0	9.0	8.0	7.0	9.0	8.0	7.0	9.0	8.0	8.0	10	9.0	8.0
T ₁	29	25	21	26	22	20	22	20	18	22	20	20	23	22	22
T ₂	15	15	14	14	15	15	17	18	19	22	23	25	28	29	31



Clock Pulse A = T₁
Output Pulse B = T₂

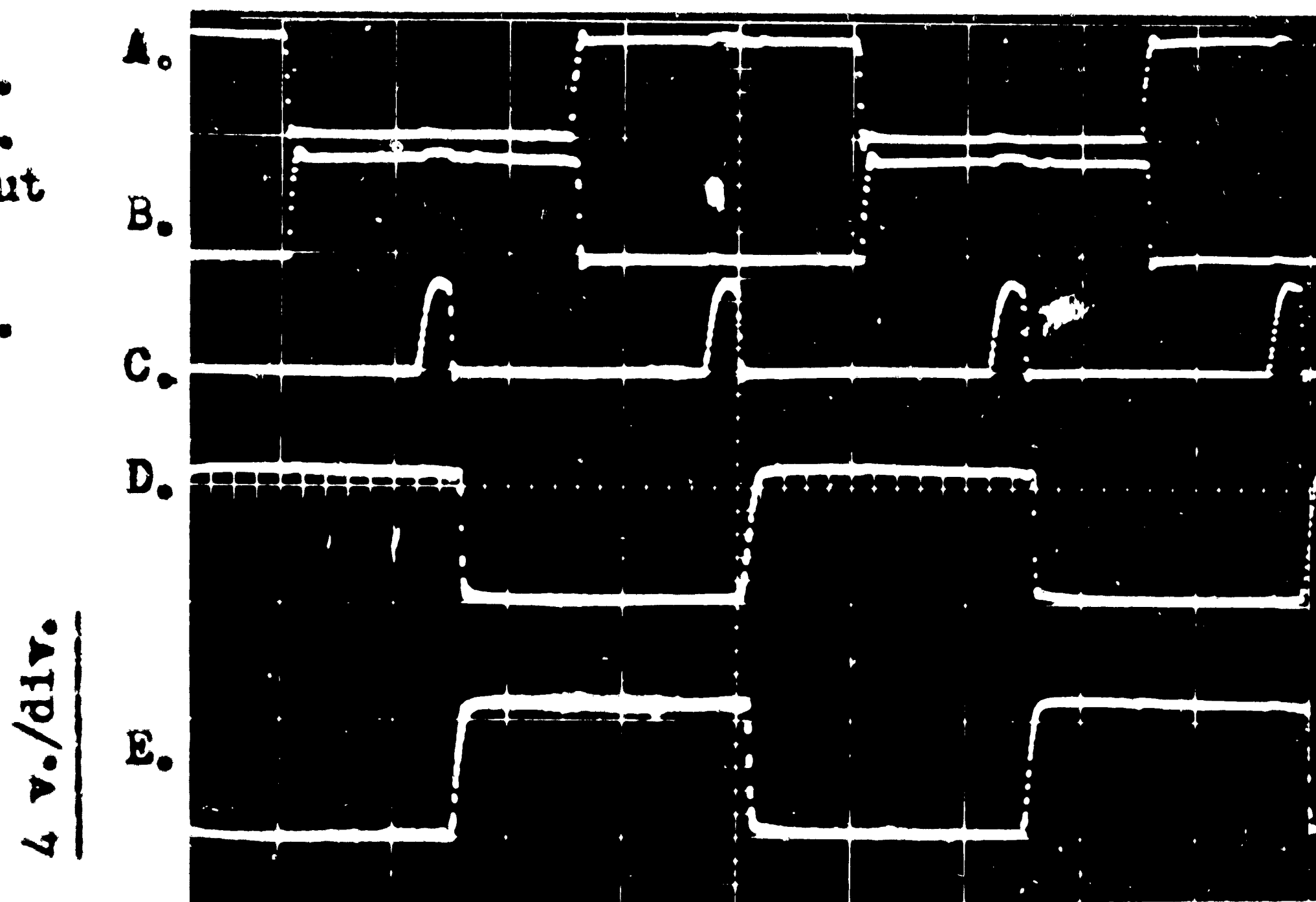


SFF-3A

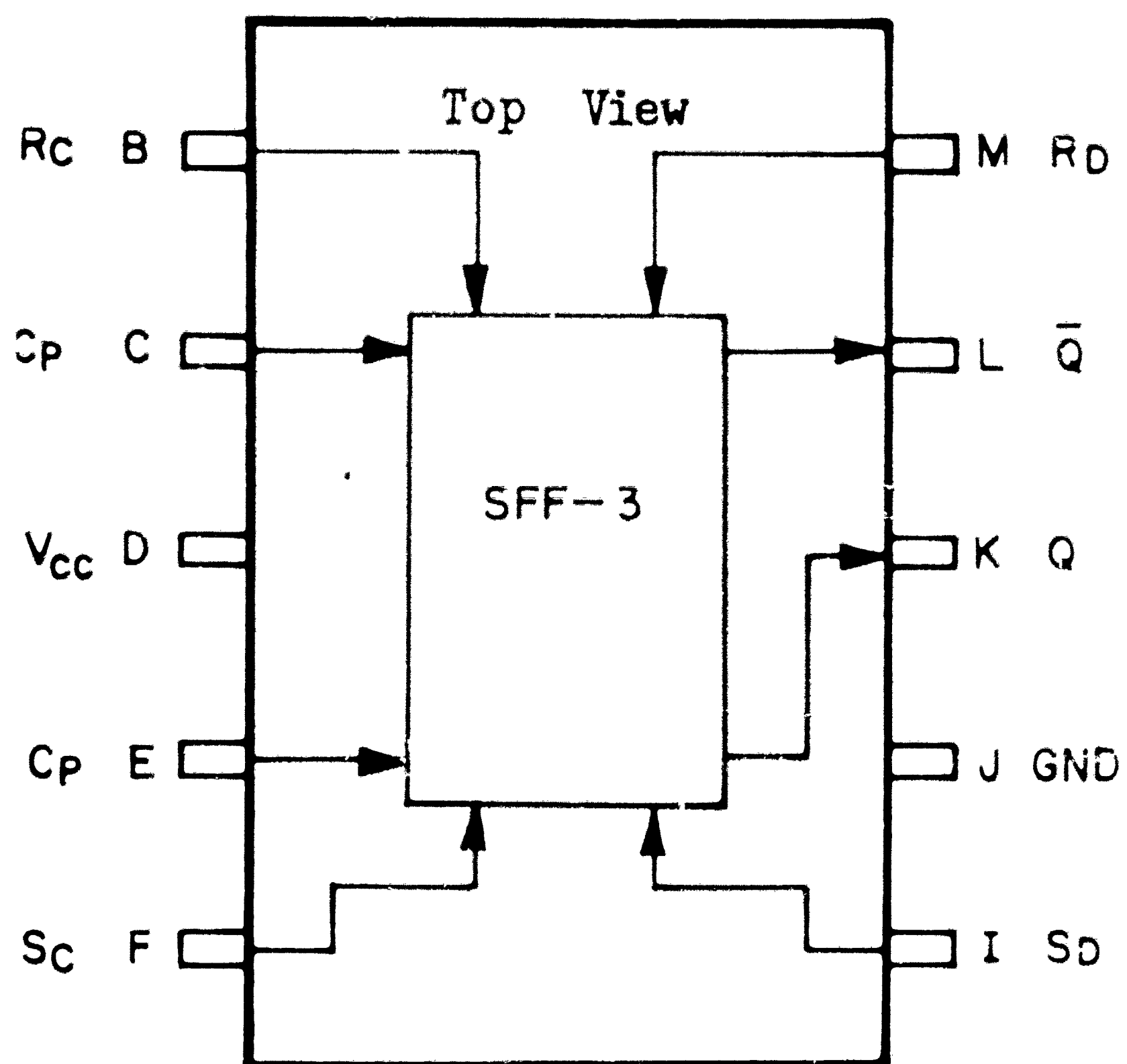
Input Freq. = 1 mc.
 Clock Freq. = 2 mc.
 Load = 1 ckt./output
 $V_{cc} = 5.0$ volts

Temperature = 25°C.

A. = #10 input
 B. = #2 input
 C. = Clock Input
 D. = #5 output
 E. = #7 output



.2 μsec./div.



SECTION 4
APPLICATION

4.0.0

Section 4 - Application

μ-Note 941

Failure Analysis and Reliability Estimates of AN/ASW-25 (XN-) Microelectronic Digital One-Way Data Link

Failure rates and reliability estimates have been completed on a prototype Data Link (one-way) equipment, consisting of Receiver, Digital Logic, D/A Converters, Discrete Indicator and Power Supply. The Receiver and the D/A converters subsystems do not contain microelectronic circuitry. The type of microelectronic circuits contained in the other subsystems are described in μ-Note 613, μ-Note 811 and μ-Note 841.

The failure rate data was extracted from FARADA, Mil-Hdbk-217 and from commercial manufacturers literature and reports for those items not included in the military publications. The estimates were based on the simplifying assumption that any part failure will result in a functional failure. No wear out and drift failures were considered.

The estimated failure rates of the present (XN-1) equipment are shown below:

<u>Functional Block</u>	<u>Rate (ppm)</u>	<u>% of Total</u>
Receiver	211	10
Digital Logic	102	5
D.C. D/A Converter	275	13
A.C. D/A Converter	1003	47
Discrete Indicator	480	23
Power Supply and Misc.	<u>35</u>	<u>2</u>
Total	2106	100%

It can be seen in the above table that the A.C. D/A Converter and the Discrete Indicator contribute 70% of the estimated total failure rate. The A.C. D/A converter has been redesigned to replace 18 relays with solid-state circuitry (one differential amplifier and 18 transistors). The Discrete Indicator has been redesigned to eliminate complexity in the driver amplifiers by utilizing 7 micro-circuit darlington amplifiers.

Preliminary failure rate estimates of a tentative (XN-2A) equipment including the above two redesigned sub-assemblies are shown below:

<u>Functional Block</u>	<u>Rate (ppm)</u>	<u>% of Total</u>
Receiver	211	24
Digital Logic	115	13
D.C. D/A Converter	275	31
A.C. D/A Converter	200	22
Discrete Indicator	50	6
Power Supply and Misc.	<u>35</u>	<u>4</u>
Total	886	100%

It can be seen in the above table that the improvement in reliability or the decrease in the total failure rate of the tentative (XN-2A) equipment is approximately 2.5.

The total failure rate is the maximum that can be expected considering that an internal failure will cause a complete system failure. Such is not the case in this equipment. Various modes of operations are possible and reliability will be different for each operating mode. The resulting effective failure rates and the corresponding

MTBF's for specific operational requirements are tabulated below:

<u>Minimum Acceptable Operating Condition</u>	<u>Present XN-1</u>	<u>Tentative XN-2A</u>
Normal Operation (Visual & Automatic)	2106 ppm 470 hrs.	886 ppm 1130 hrs.
Manual Approach only (no Autopilot input)	1103 ppm 900 hrs.	686 ppm 1470 hrs.
Automatic Approach only (unusable Cross-Pointer)	1831 ppm 540 hrs.	611 ppm 1640 hrs.
Either Manual only or Automatic only	960 ppm 1040 hrs.	475 ppm 2100 hrs.

The above table indicates a reliability improvement of 2 to 1 between the various operating conditions.

SECTION 5
AVAILABILITY

5.0.0

μ -NOTE 951

MICROELECTRONIC DEVICES
EVALUATED FOR μ -NOTES

The table on the following page lists the commercially available microelectronic functional devices which have been evaluated and reported upon in the μ -NOTES. The μ -NOTES issue number in which the evaluation results can be found is at the top of the table. The line below the μ -NOTES issue number identifies the source of the units by manufacturer. The basic description of each circuit type is referenced to each manufacturer by the particular manufacturers model number for the circuit evaluated.

LL-NOTES Issue No.	1	2	3	3	3	3	4	5	6	6	7	7	7	7	8	9	9	9	9	10
Circuit Manufacturer	TI	F	SIG.	PSI	RCA	WHSE.	MOT.	M-H	M-H	M-H	TI	F	F	F	SIG.	SIL.	9	9	9	10
AND Gate									MM4101		SN532				SE105K			264P	OME	SN63B (2) SN620
Dual AND											SN534							264L3		
AND Gate			SE100T SE200T		DMC-100	MM2104			MM43001		SN531	UL907			SE102K	A07A (1) A06A		264L2 (1) 264D2	26538	SN608 (1)
Dual NAND				PCF-101		MM2101					SN533					A07A			26534	SN62AB (1)
NOR Gate	SN512	G										L907			SE102K					
Dual NOR	SN514								MM4101					MM41910						
NOR w/Emitter Follower	SN513																			
OR/NOR Gate							MC306G												54305	
Exclusive OR	SN515		SE140T																	
Buffer		B	SE130T								SN535	UL900		MM41909						
Flip-Flop	SN510	F	SE120T	PCF-101			MC302G	MM43201			SN530	UL916			SE124K			264B		SFT-2B SFT-3A
Flip-Flop w/Emitter Pol.	SN511																			
Half Adder		H		PCF-101			MC303G		MM41301			UL904		MM41912						
Adder									MM41201					MM41908						
Half Shift Register		S										UL905								
Shift Register				PCF-101					MM41501							A03A				
Counter Adapter		C										UL901								
Bus Driver							MC304G													
Power Gate															SE110K			153D3	264P (1)	
Line Driver															SE150K	A05A (1)				
Monostable Multivib.															SE160K	A08A				

*
F-----Fairchild
GE-----General Micro-Electronics
M-H-----Minneapolis-Honeywell
MOT-----Motorola
PSI-----Pacific Semiconductor Inc.
RCA-----Radio Corporation America
SIG-----Signetics
SIL-----Siliconix
SYL-----Sylvania
TI-----Texas Instruments
WHSE-----Westinghouse

- (1) Same circuit performs NAND/NOR operation
(2) Same circuit performs AND/NOR operation

DIGITAL EVALUATIONS